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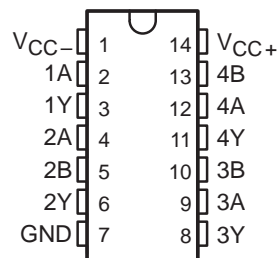
[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

# SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

SLLS033F – JANUARY 1988 – REVISED MARCH 1997

- **Bi-MOS Technology With TTL and CMOS Compatibility**
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Very Low Quiescent Current . . . 95  $\mu$ A Typ**  
 $V_{CC\pm} = \pm 12$  V
- **Current-Limited Outputs . . . 10 mA Typ**
- **CMOS- and TTL-Compatible Inputs**
- **On-Chip Slew Rate Limited to 30 V/ $\mu$ s max**
- **Flexible Supply Voltage Range**
- **Characterized at  $V_{CC\pm}$  of  $\pm 4.5$  V and  $\pm 15$  V**
- **Functionally Interchangeable With Texas Instruments SN75188, Motorola MC1488, and National Semiconductor DS14C88**

**D, DB<sup>†</sup>, OR N PACKAGE  
(TOP VIEW)**



<sup>†</sup> The DB package is only available left-end taped and reeled, i.e., order device SN75C188DBLE.

## description

The SN75C188 is a monolithic, low-power, quadruple line driver that interfaces data terminal equipment with data communications equipment. This device is designed to conform to ANSI Standard EIA/TIA-232-E.

An external diode in series with each supply-voltage terminal is needed to protect the SN75C188 under certain fault conditions to comply with EIA/TIA-232-E.

The SN75C188 is characterized for operation from 0°C to 70°C.

## Function Tables

**DRIVER 1**

B	Y
H	L
L	H

**DRIVERS 2 – 4**

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,  
X = don't care



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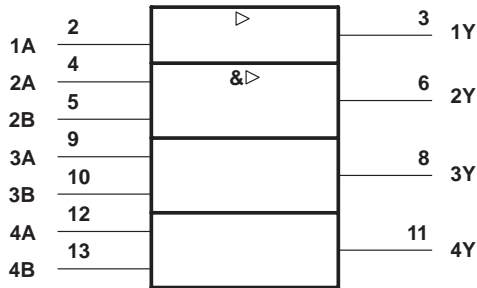
 **TEXAS  
INSTRUMENTS**

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# SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

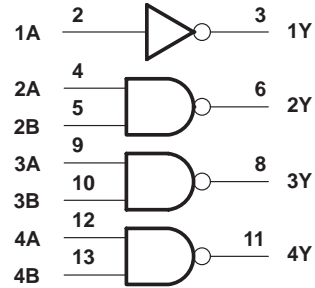
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

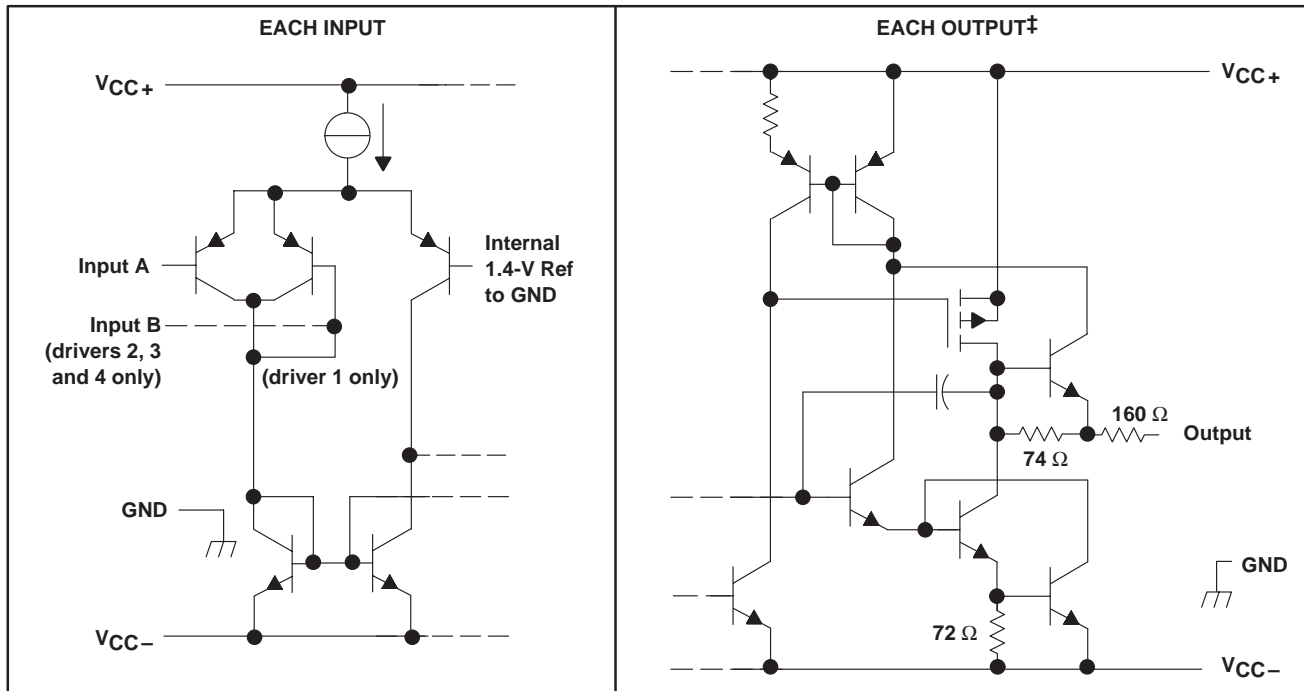


positive logic

$$Y = \bar{A} \text{ (driver 1)}$$

$$Y = \overline{AB} \text{ or } \overline{A + B} \text{ (drivers 2 through 4)}$$

## schematics of inputs and outputs



‡ All resistor values shown are nominal.

## SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+}$ (see Note 1)	15 V
Supply voltage, $V_{CC-}$ (see Note 1)	-15 V
Input voltage range, $V_I$	$V_{CC-}$ to $V_{CC+}$
Output voltage range, $V_O$	$V_{CC-} - 6\text{ V}$ to $V_{CC+} + 6\text{ V}$
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
DB	525 mW	4.2 mW/°C	336 mW
N	1150 mW	9.2 mW/°C	736 mW

### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC+}$	4.5	12	15	V
Supply voltage, $V_{CC-}$	-4.5	-12	-15	V
Input voltage, $V_I$	$V_{CC-} + 2$		$V_{CC+}$	V
High-level Input voltage, $V_{IH}$	2			V
Low-level Input voltage, $V_{IL}$			0.8	V
Operating free-air temperature, $T_A$	0		70	°C

## SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

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electrical characteristics over operating free-air temperature range,  $V_{CC+} = 12\text{ V}$ ,  $V_{CC-} = -12\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{OH}$ High-level output voltage	$V_{IL} = 0.8\text{ V}$ , $R_L = 3\text{ k}\Omega$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$	4			V
		$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$	10			
$V_{OL}$ Low-level output voltage (see Note 2)	$V_{IH} = 2\text{ V}$ , $R_L = 3\text{ k}\Omega$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$	-4			V
		$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$	-10			
$I_{IH}$ High-level input current	$V_I = 5\text{ V}$		10			$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_I = 0$		-10			$\mu\text{A}$
$I_{OS(H)}$ High-level short-circuit output current‡	$V_I = 0.8\text{ V}$ , $V_O = 0$ or $V_{CC-}$		-5.5	-10	-19.5	mA
$I_{OS(L)}$ Low-level short-circuit output current‡	$V_I = 2\text{ V}$ , $V_O = 0$ or $V_{CC+}$		5.5	10	19.5	mA
$r_O$ Output resistance, power off	$V_{CC+} = 0$ , $V_{CC-} = 0$ , $V_I = -2\text{ V}$ to $2\text{ V}$		300			$\Omega$
$I_{CC+}$ Supply current from $V_{CC+}$	$V_{CC+} = 5\text{ V}$ , No load	$V_{CC-} = -5\text{ V}$ , All inputs at $2\text{ V}$ or $0.8\text{ V}$	90			$\mu\text{A}$
	$V_{CC+} = 12\text{ V}$ , No load	$V_{CC-} = -12\text{ V}$ , All inputs at $2\text{ V}$ or $0.8\text{ V}$	95			
$I_{CC-}$ Supply current from $V_{CC-}$	$V_{CC+} = 5\text{ V}$ , No load	$V_{CC-} = -5\text{ V}$ , All inputs at $2\text{ V}$ or $0.8\text{ V}$	-90			$\mu\text{A}$
	$V_{CC+} = 12\text{ V}$ , No load	$V_{CC-} = -12\text{ V}$ , All inputs at $2\text{ V}$ or $0.8\text{ V}$	-95			

† All typical values are at  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only; e.g., if  $-4\text{ V}$  is a maximum, the typical value is a more negative voltage.

### switching characteristics, $V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output§	$R_L = 3\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , See Figure 1	3			$\mu\text{s}$
$t_{PHL}$ Propagation delay time, high- to low-level output§		3.5			$\mu\text{s}$
$t_{TLH}$ Transition time, low- to high-level output¶		0.53		3.2	$\mu\text{s}$
$t_{THL}$ Transition time, high- to low-level output¶		0.53		3.2	$\mu\text{s}$
$t_{TLH}$ Transition time, low- to high-level output#	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $C_L = 2500\text{ pF}$ , See Figure 1	1.5			$\mu\text{s}$
$t_{THL}$ Transition time, high- to low-level output#		1.5			$\mu\text{s}$
SR Output slew rate§	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $C_L = 15\text{ pF}$	6	15	30	$\text{V}/\mu\text{s}$

§ Measured at the 50% level

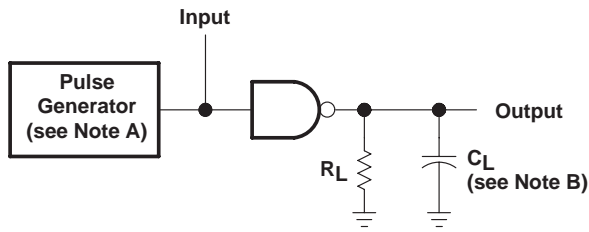
¶ Measured between the 10% and 90% points on the output waveform

# Measured between the  $3\text{-V}$  and  $-3\text{-V}$  points on the output waveform (EIA/TIA-232-E conditions), all unused inputs tied either high or low

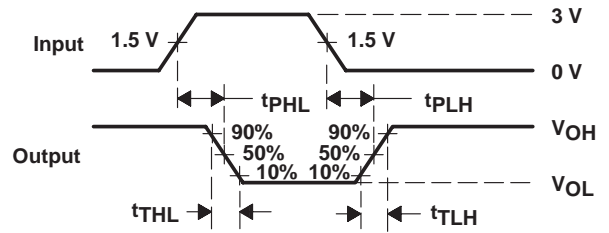
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**PARAMETER MEASUREMENT INFORMATION**



**TEST CIRCUIT**



**VOLTAGE WAVEFORMS**

- NOTES: A. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ ,  $PRR = 20 \text{ kHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = t_f \leq 50 \text{ ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 1. Test Circuit and Voltage Waveforms**

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**TYPICAL CHARACTERISTICS**

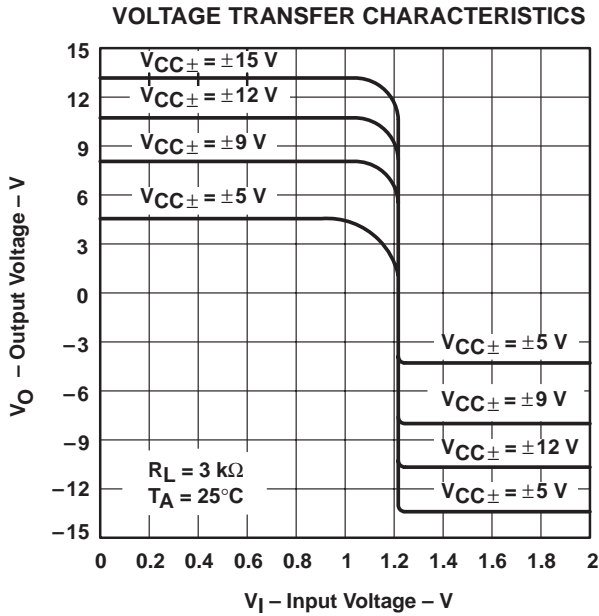


Figure 2

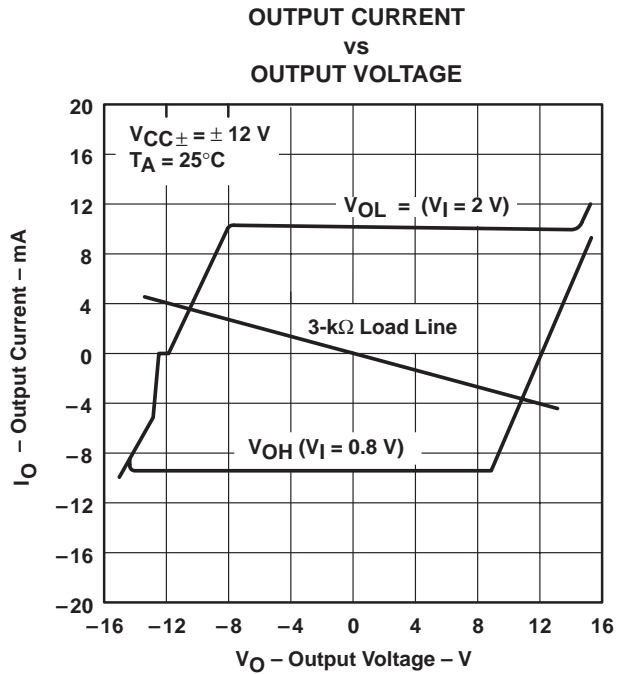


Figure 3

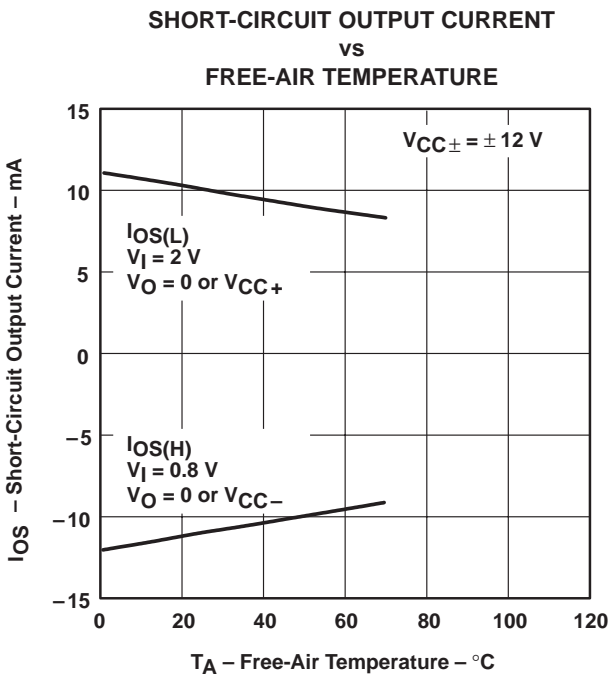


Figure 4

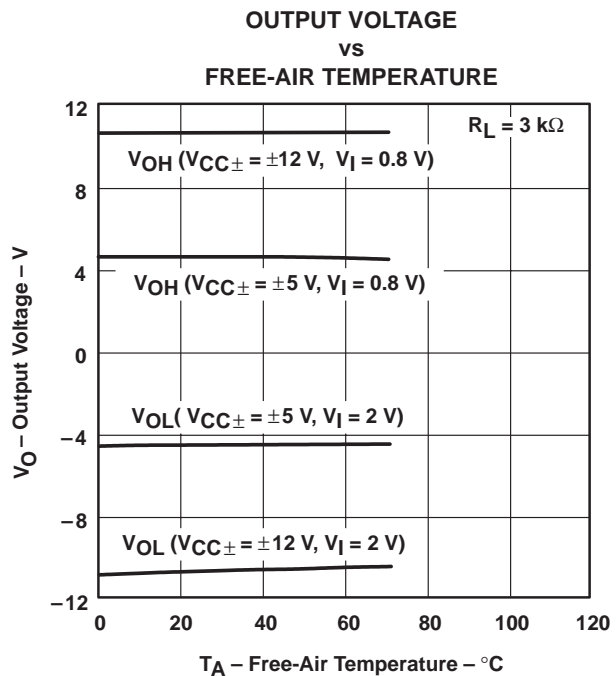


Figure 5

**SN75C188**  
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**TYPICAL CHARACTERISTICS**

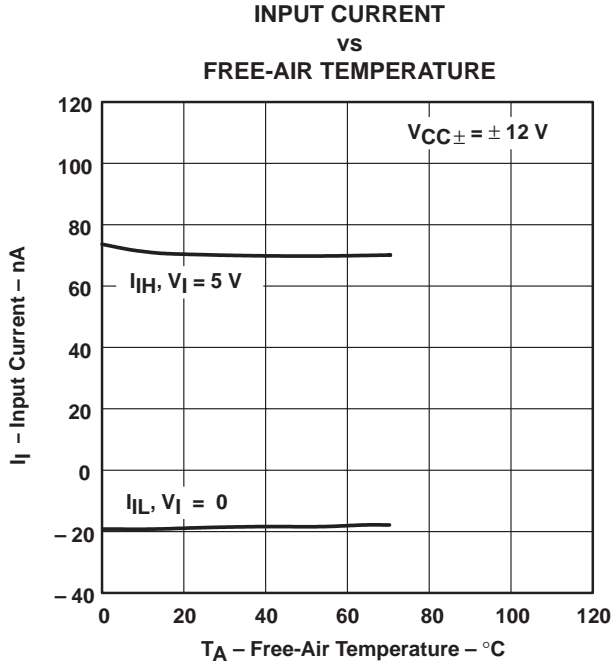


Figure 6

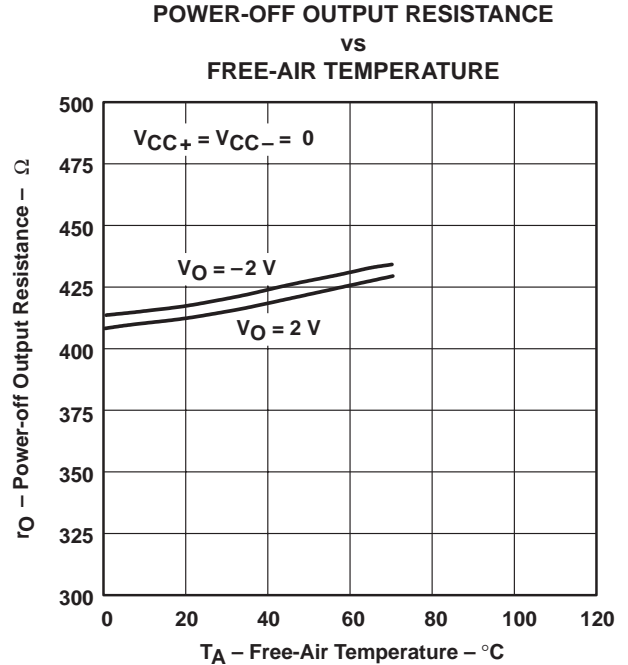


Figure 7

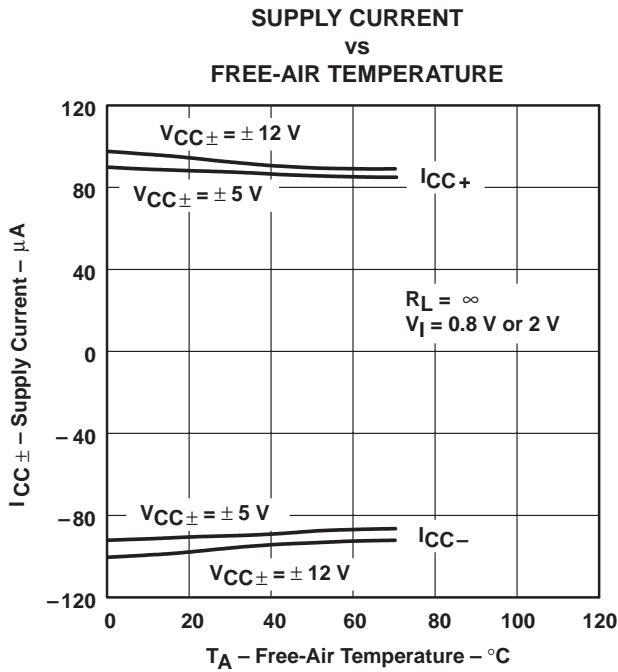


Figure 8

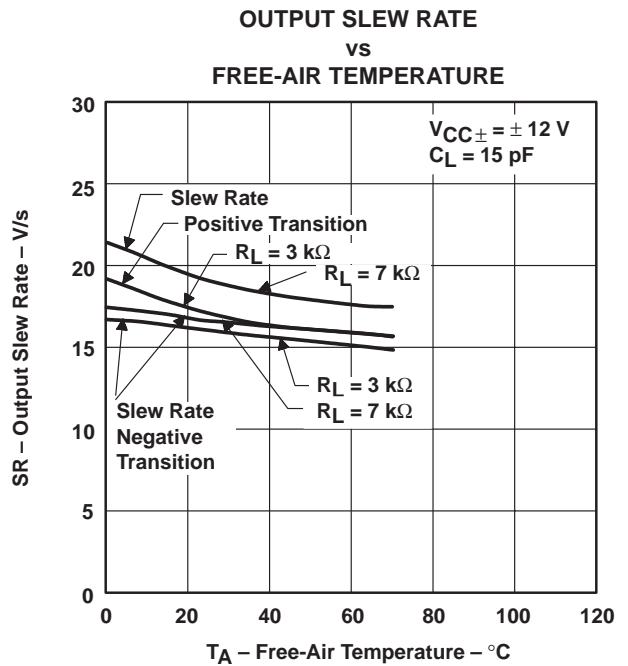


Figure 9



**SN75C188**  
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**TYPICAL CHARACTERISTICS**

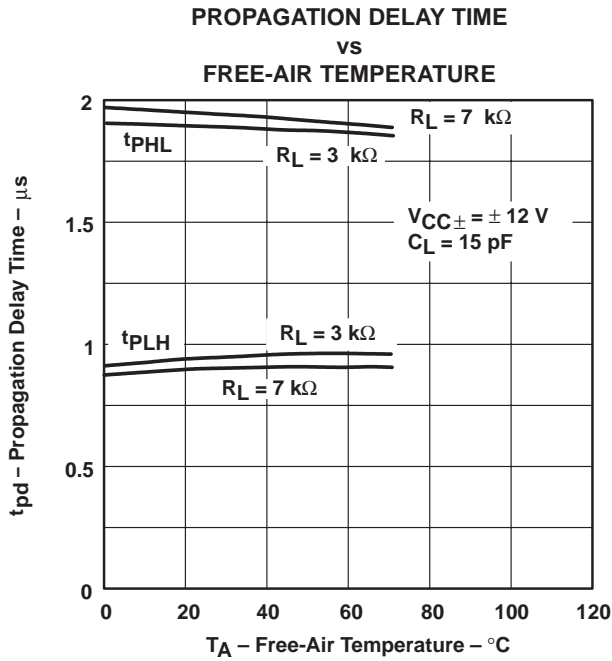


Figure 10

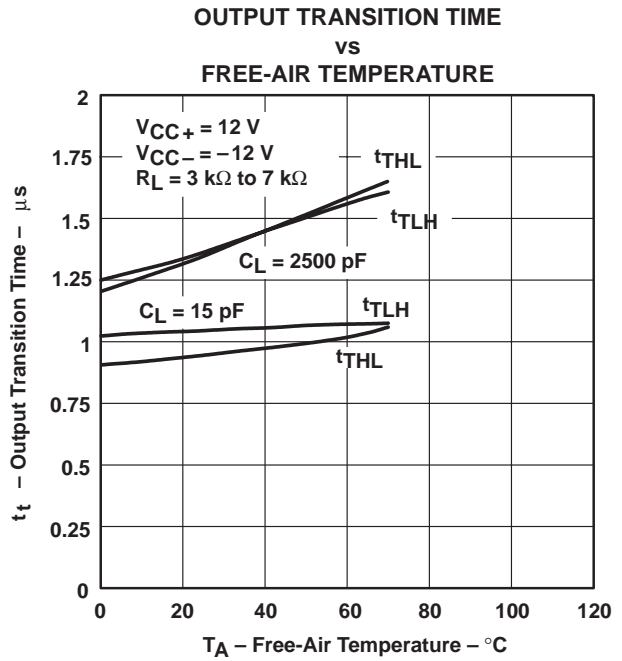


Figure 11

**APPLICATION INFORMATION**

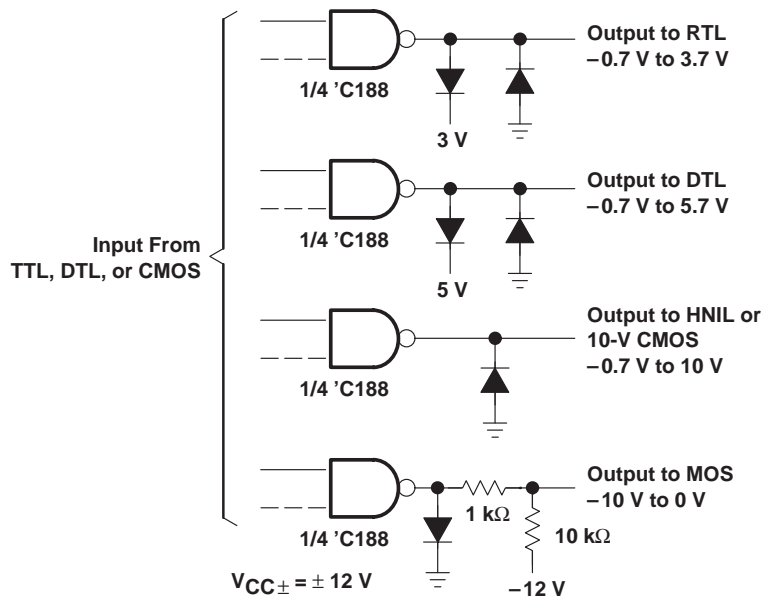
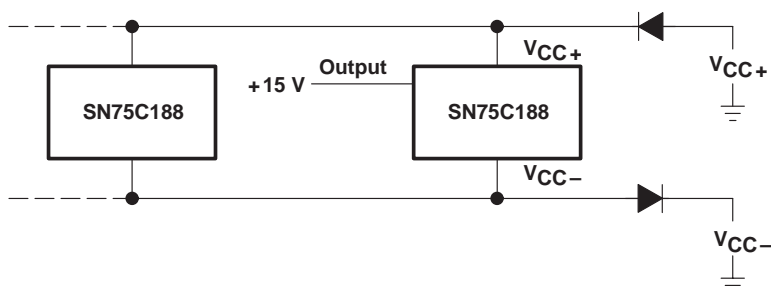


Figure 12. Logic Translator Applications

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**APPLICATION INFORMATION**



NOTE A: External diodes placed in series with the  $V_{CC+}$  and  $V_{CC-}$  leads protect the SN75C188 in the fault condition where the device outputs are shorted to  $\pm 15\text{ V}$  and the power supplies are at low voltage and provide low-impedance paths to GND.

**Figure 13. Power Supply Protection to Meet Power-Off Fault Conditions of Standard EIA/TIA-232-E**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75C188D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188	<a href="#">Samples</a>
SN75C188DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	0 to 70		
SN75C188DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA188	<a href="#">Samples</a>
SN75C188DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188	<a href="#">Samples</a>
SN75C188DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188	<a href="#">Samples</a>
SN75C188DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188	<a href="#">Samples</a>
SN75C188N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75C188N	<a href="#">Samples</a>
SN75C188NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75C188N	<a href="#">Samples</a>
SN75C188NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C188	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

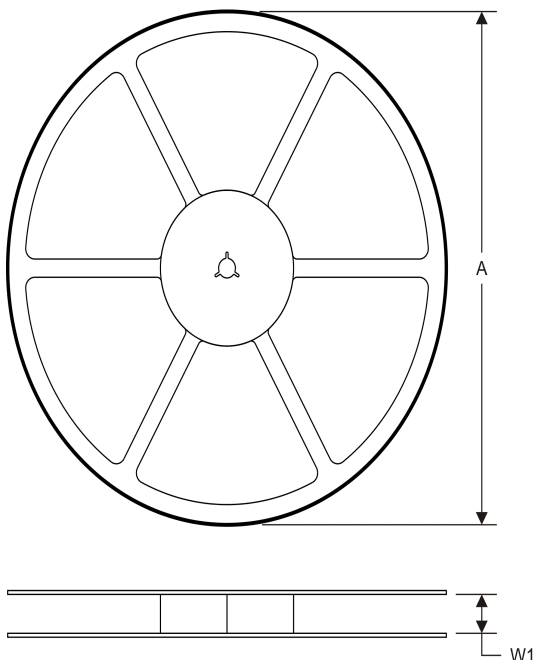
<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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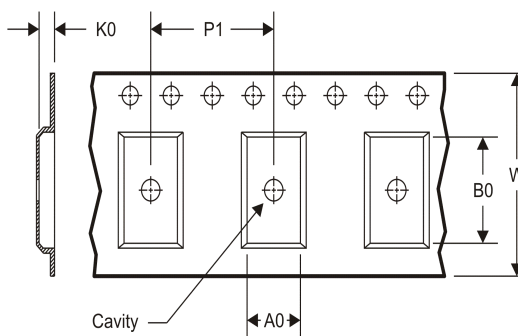
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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



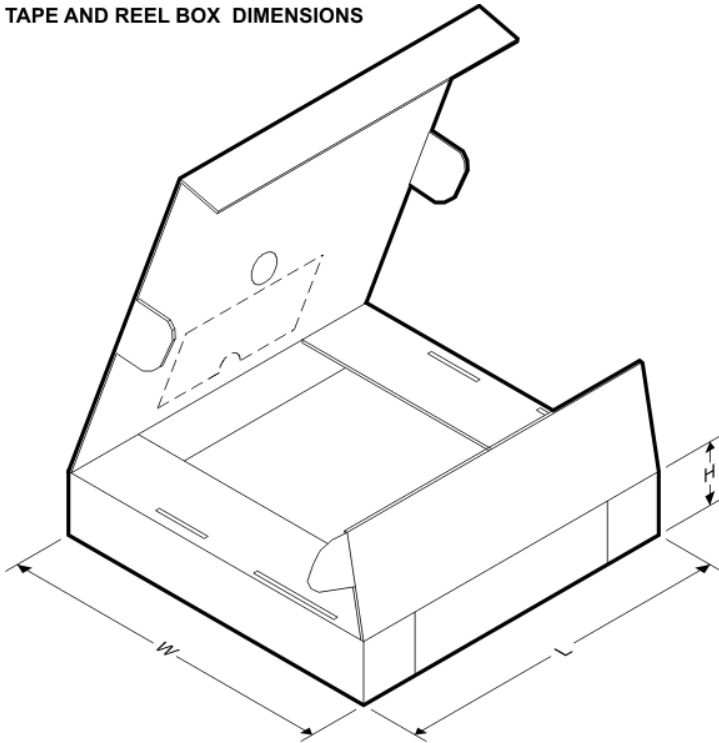
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C188DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75C188DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C188DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C188NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

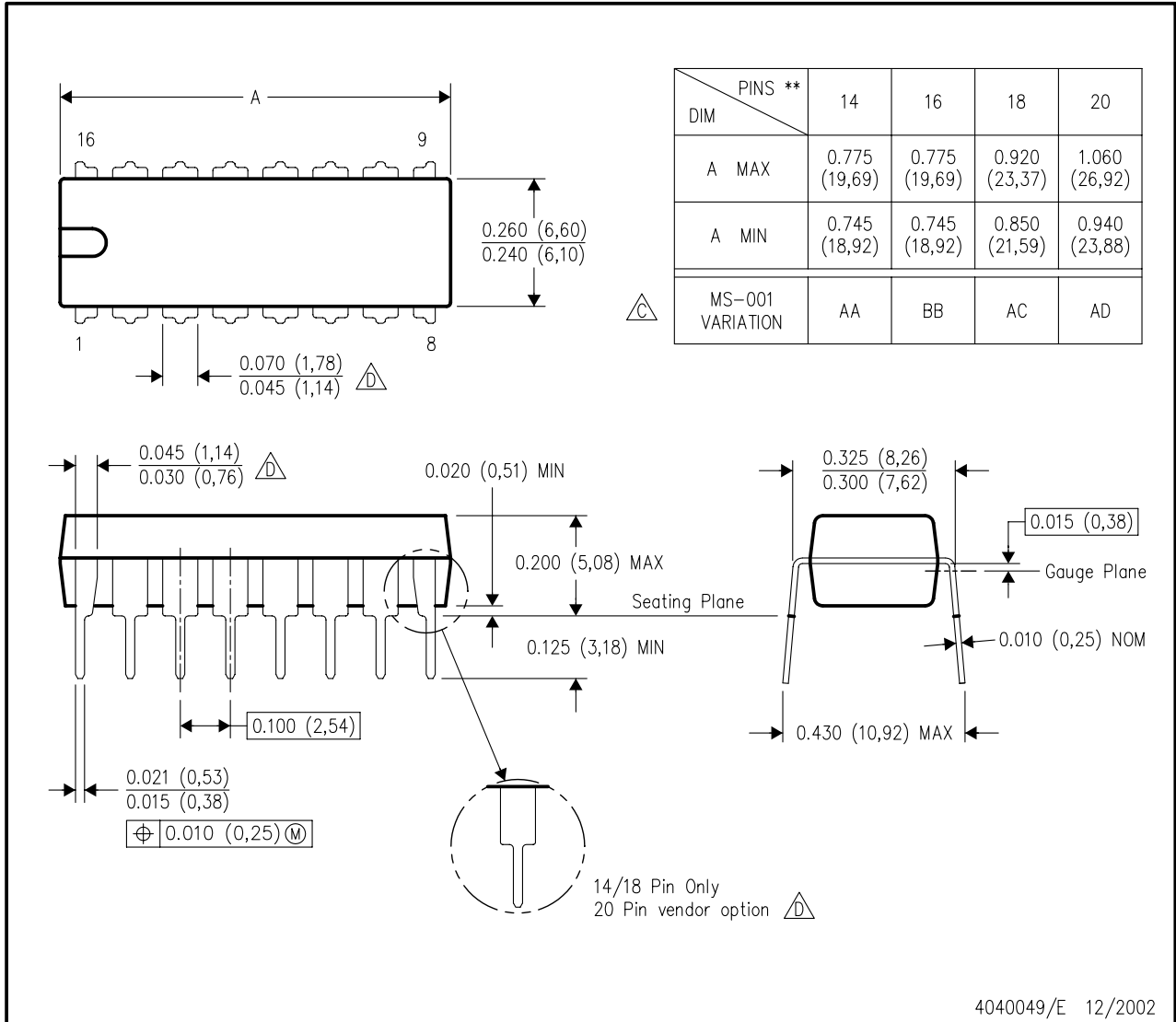
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C188DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN75C188DR	SOIC	D	14	2500	333.2	345.9	28.6
SN75C188DR	SOIC	D	14	2500	367.0	367.0	38.0
SN75C188NSR	SO	NS	14	2000	367.0	367.0	38.0

**MECHANICAL DATA**

**N (R-PDIP-T\*\*)**

16 PINS SHOWN

**PLASTIC DUAL-IN-LINE PACKAGE**



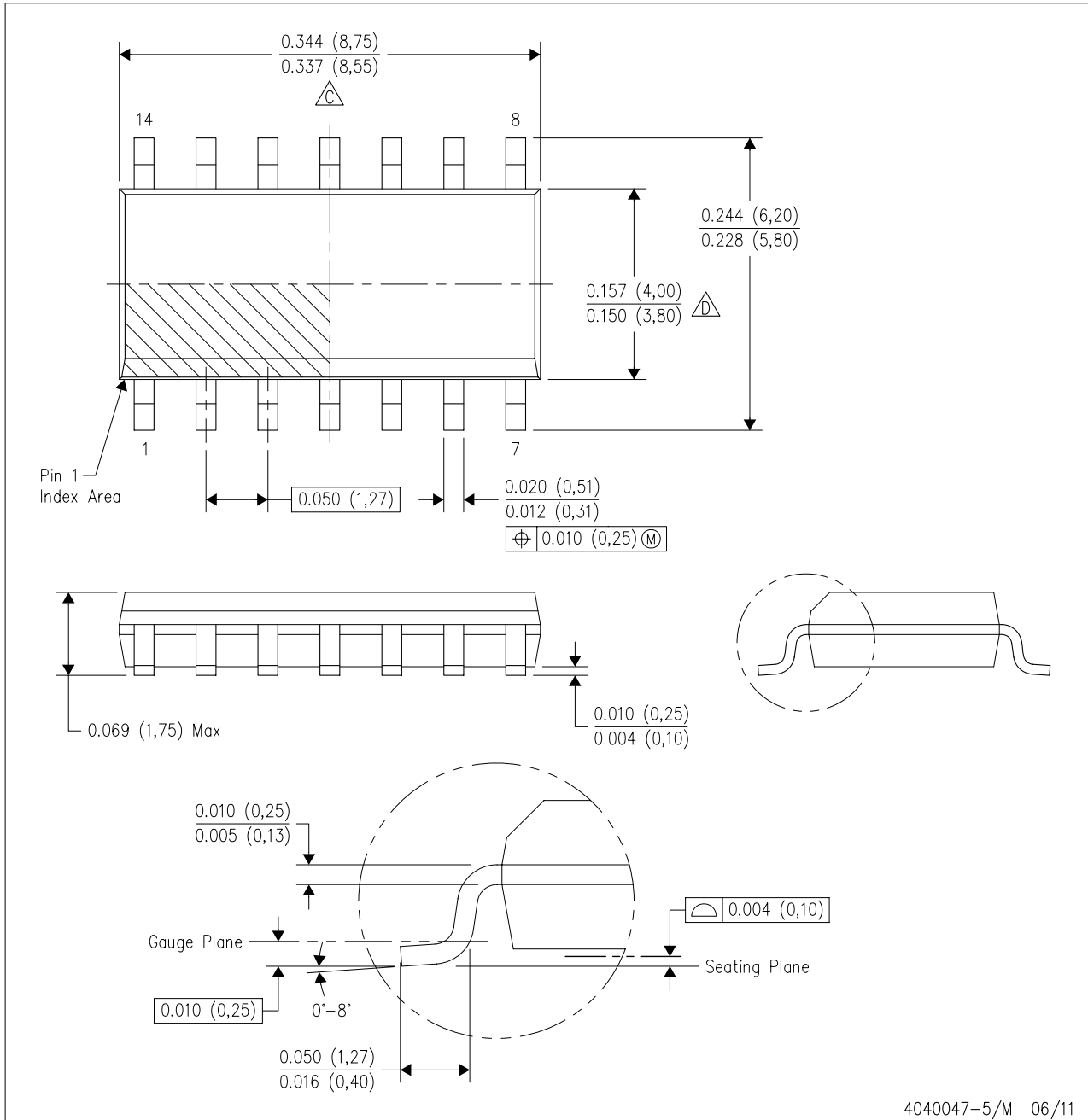
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

**MECHANICAL DATA**

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



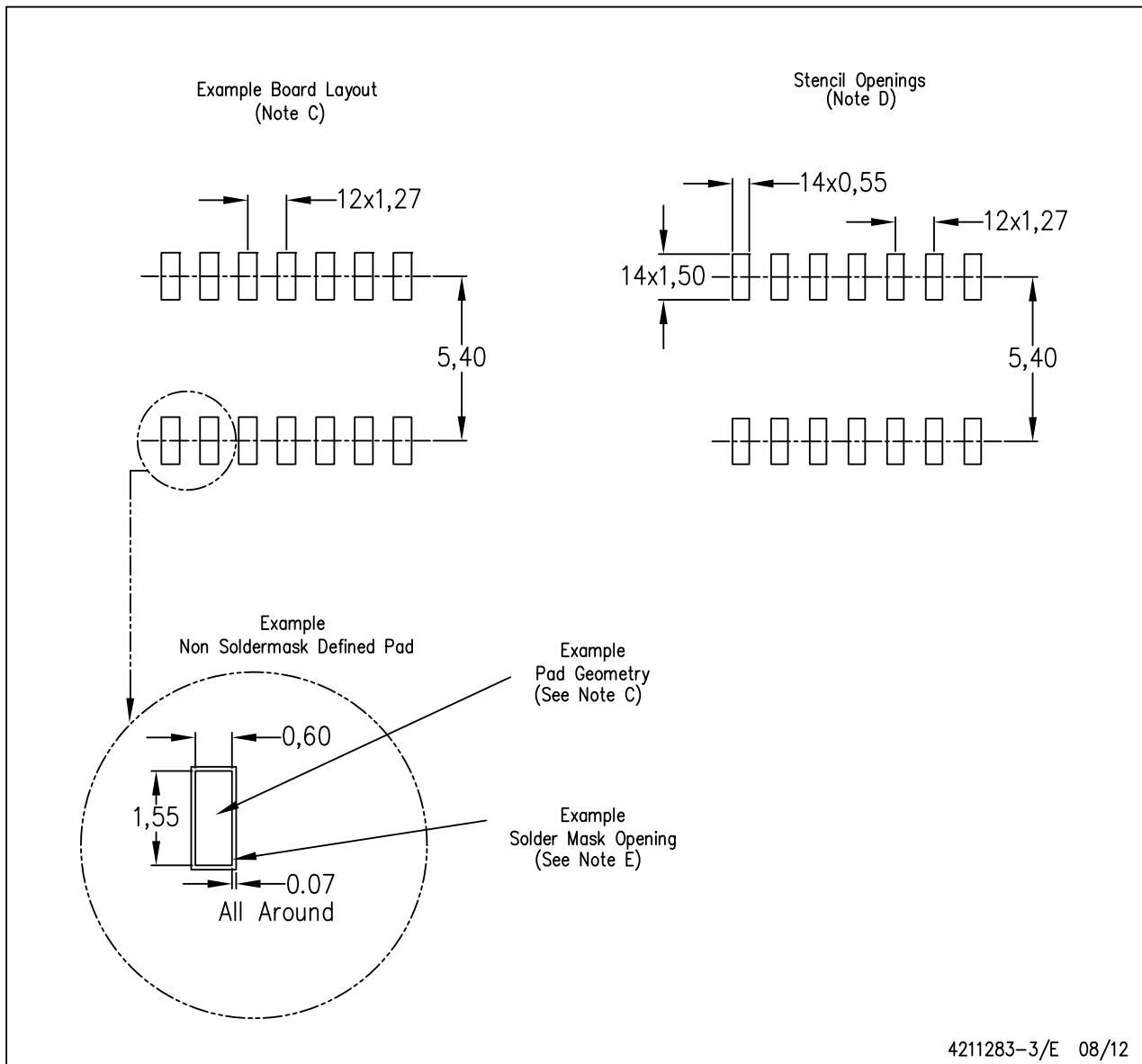
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



**LAND PATTERN DATA**

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

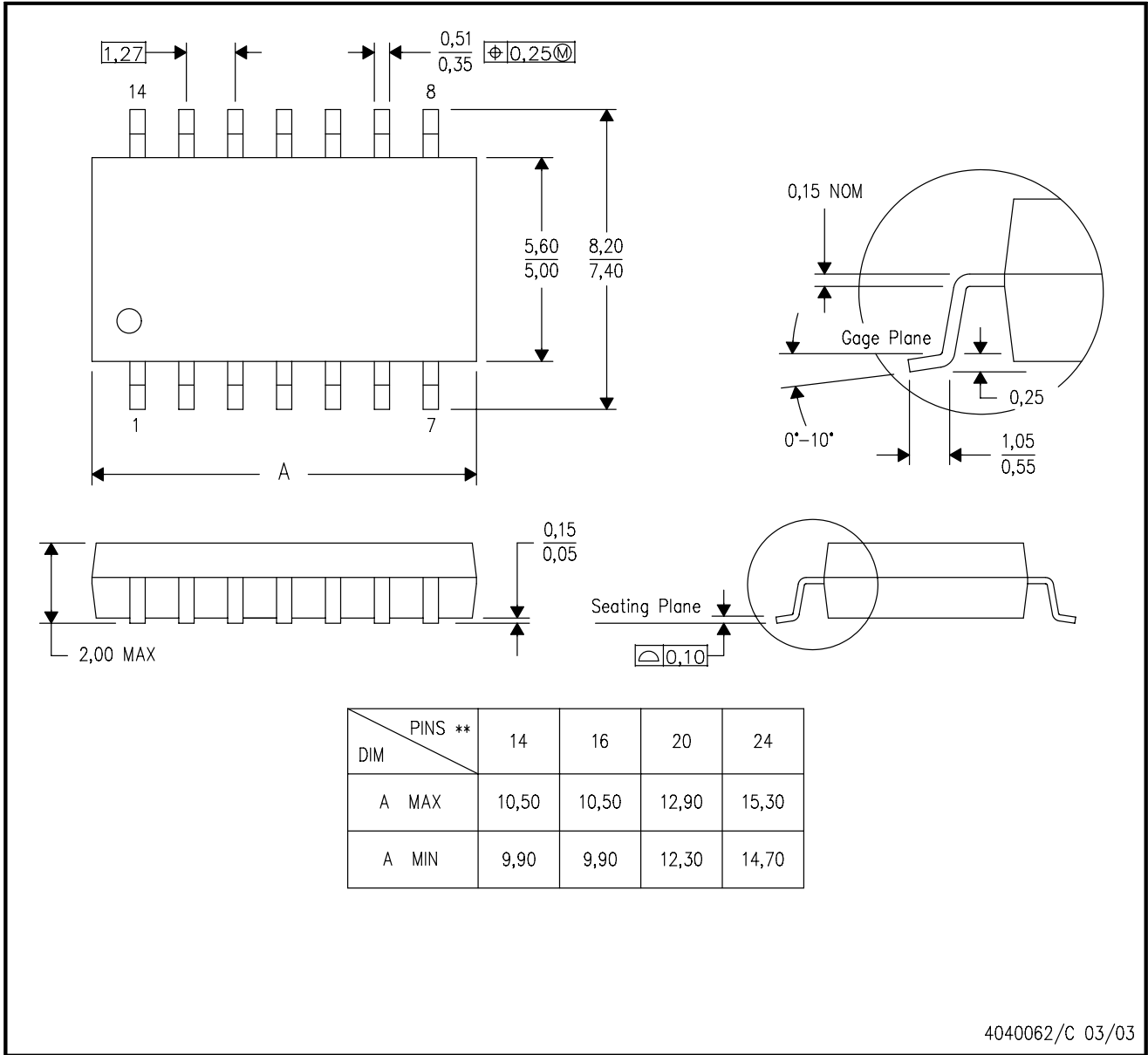
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**MECHANICAL DATA**

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



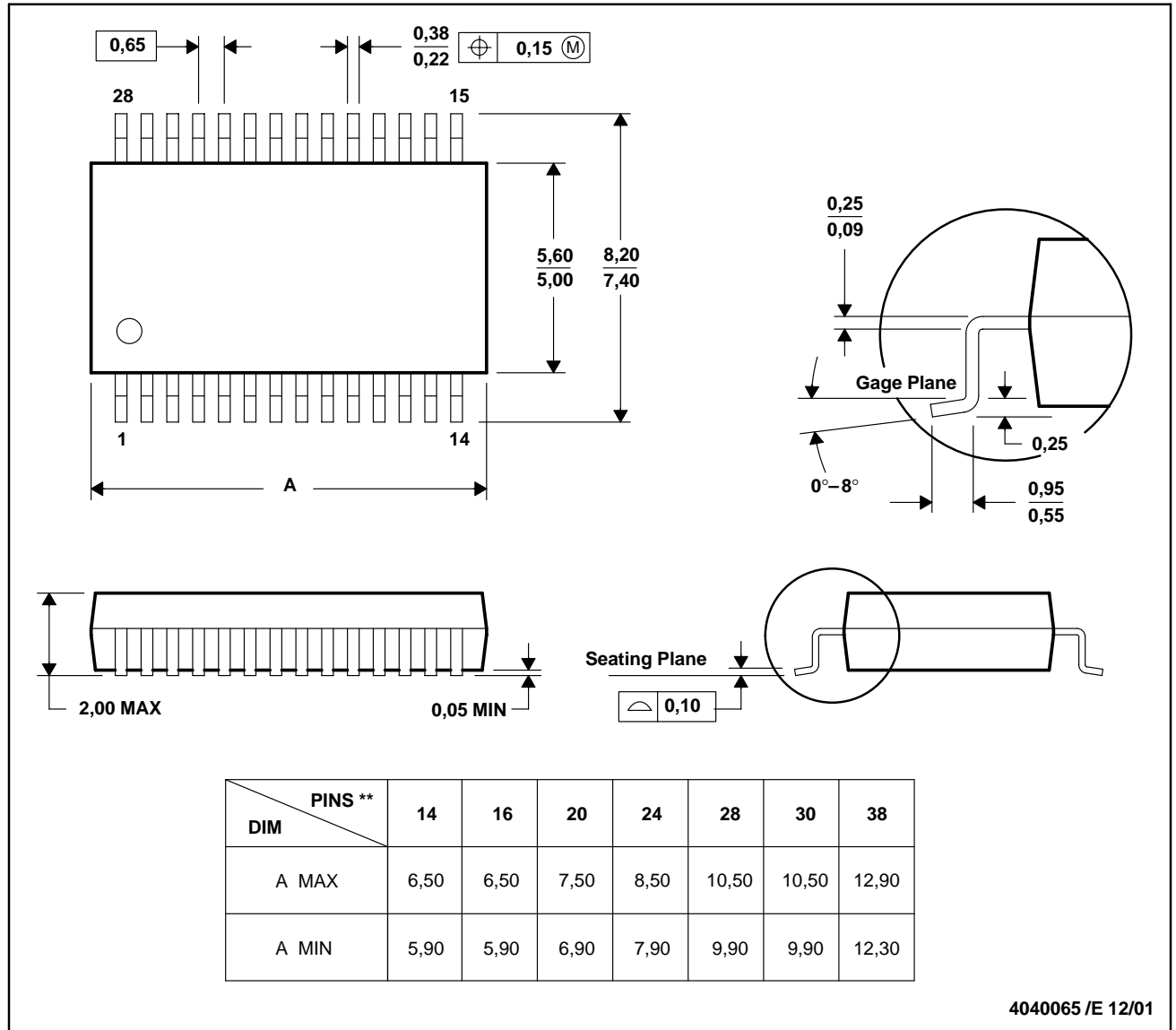
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSS0002E - JANUARY 1995 - REVISED DECEMBER 2001

**DB (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



4040065 / E 12/01

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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