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Z0109NN0

4Q Triac

26 August 2013

Product data sheet

1. General description

Planar passivated sensitive gate four quadrant triac in a SOT223 (SC-73) surface-mountable plastic package intended for applications requiring enhanced immunity to noise and direct interfacing to logic level ICs and low power gate drivers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Enhanced current surge capability
- Enhanced noise immunity
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate in four quadrants
- Surface-mountable package
- Triggering in all four quadrants

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 20 \text{ ms}$; Fig. 4 ; Fig. 5	-	-	12.5	A
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_{sp} \leq 105^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	1	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2+ G+; $T_j = 25^\circ\text{C}$; Fig. 9	0.4	-	10	mA



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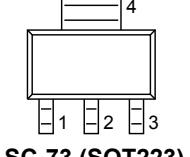
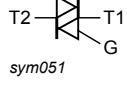
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2+ G-; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 9	0.4	-	10	mA
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2- G-; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 9	0.4	-	10	mA
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2- G+; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 9	0.4	-	10	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 SC-73 (SOT223)	 sym051
2	T2	main terminal 2		
3	G	gate		
4	T2	main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
Z0109NN0	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
Z0109NN0	109NN0

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 105$ °C; Fig. 1 ; Fig. 2 ; Fig. 3		-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4 ; Fig. 5		-	12.5	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	13.8	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	0.78	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 1$ A; $I_G = 20$ mA; $dI_G/dt = 100$ mA/ μs ; T2+ G+		-	50	$A/\mu s$
		$I_T = 1$ A; $I_G = 20$ mA; $dI_G/dt = 100$ mA/ μs ; T2+ G-		-	50	$A/\mu s$
		$I_T = 1$ A; $I_G = 20$ mA; $dI_G/dt = 100$ mA/ μs ; T2- G-		-	50	$A/\mu s$
		$I_T = 1$ A; $I_G = 20$ mA; $dI_G/dt = 100$ mA/ μs ; T2- G+		-	20	$A/\mu s$
I_{GM}	peak gate current			-	1	A
P_{GM}	peak gate power			-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C

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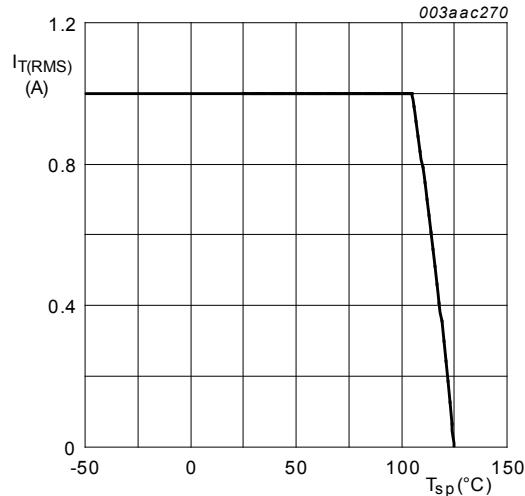
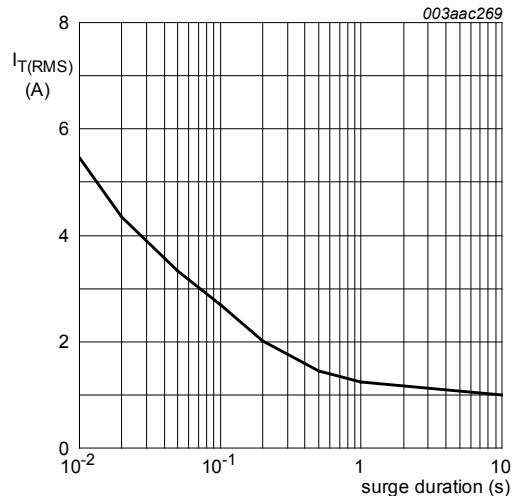


Fig. 1. RMS on-state current as a function of solder point temperature; maximum values



f = 50 Hz; T_{sp} = 105 °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values

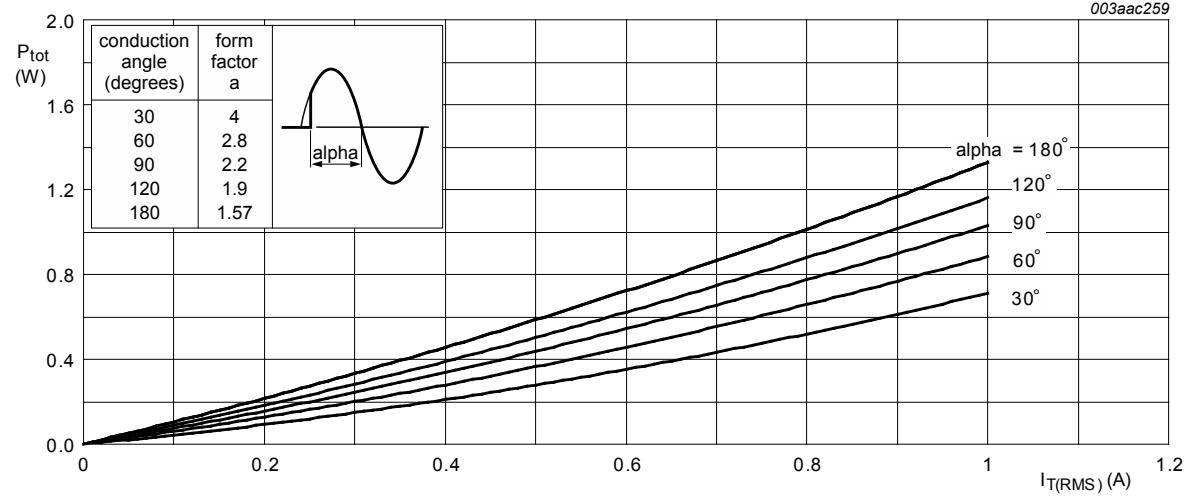


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

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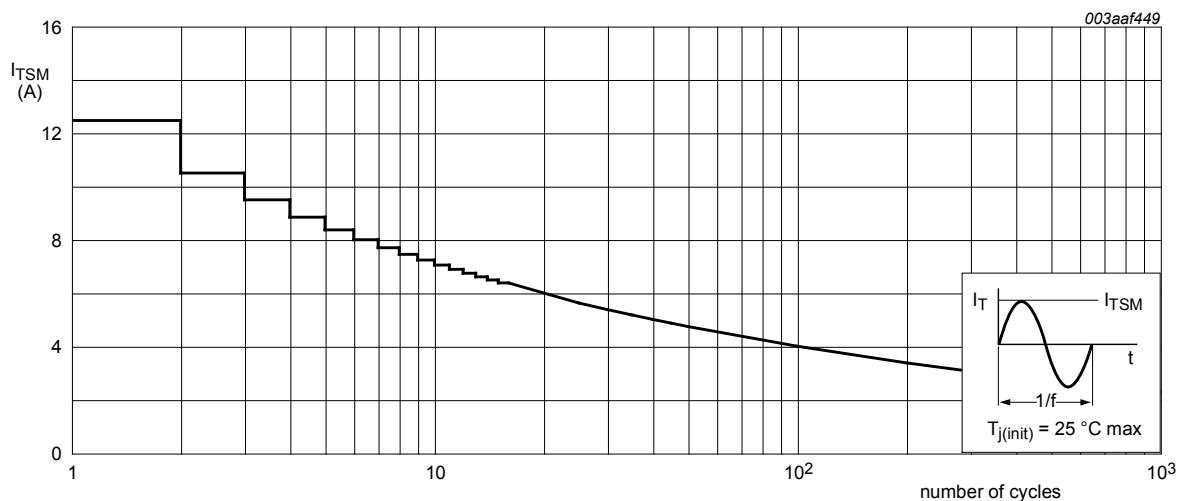


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

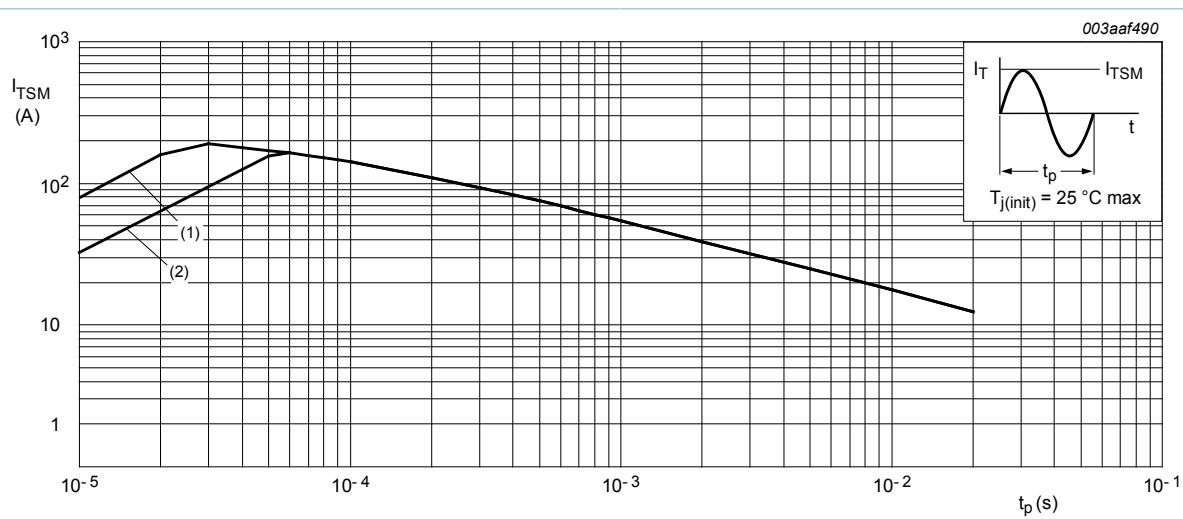


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

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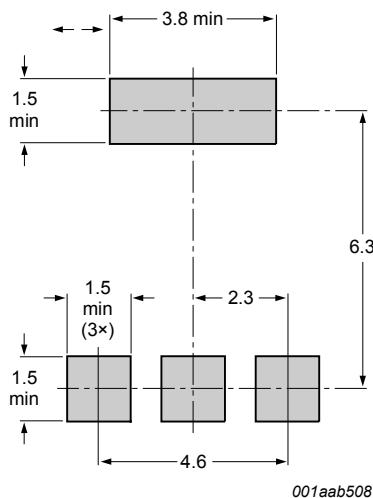
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9. Thermal characteristics

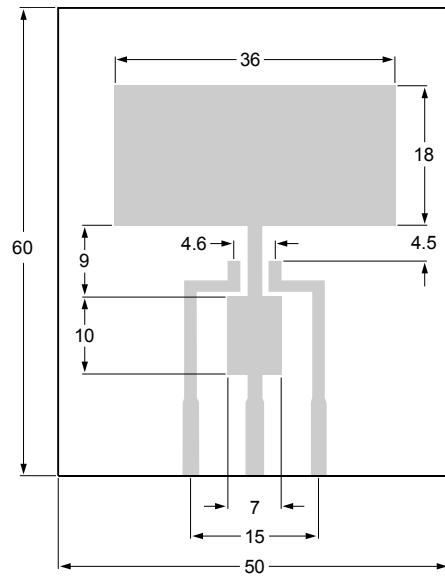
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	full cycle; Fig. 8	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; printed-circuit board mounted: minimum footprint; full cycle; Fig. 6	-	156	-	K/W
		in free air; printed-circuit board mounted: pad area; full cycle; Fig. 7	-	70	-	K/W



All dimensions are in mm

Fig. 6. Minimum footprint SOT223



All dimensions are in mm

Printed circuit board:
 FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick)

Fig. 7. Printed circuit board pad area: SOT223

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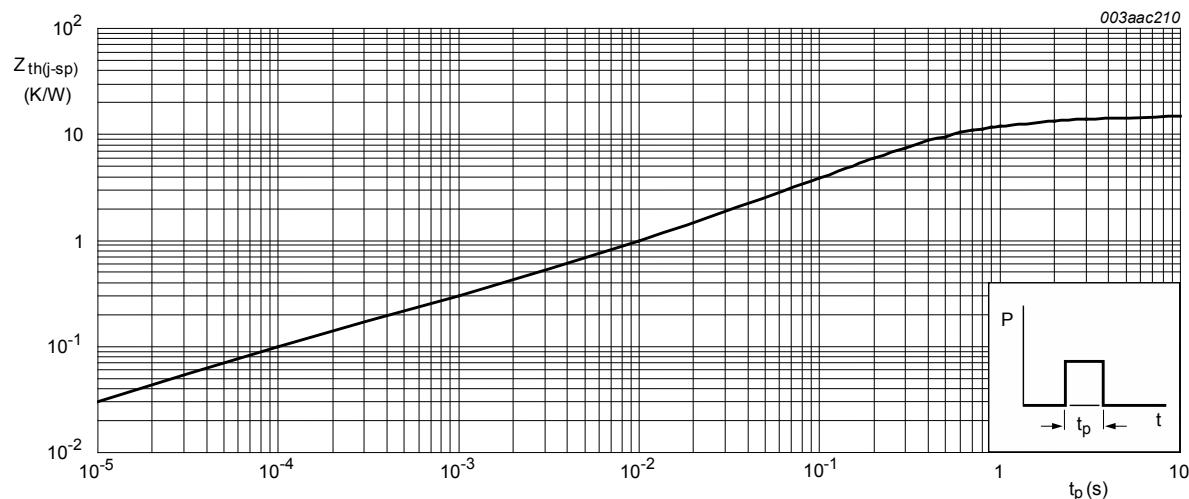


Fig. 8. Transient thermal impedance from junction to solder point as a junction of pulse width

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10. Characteristics

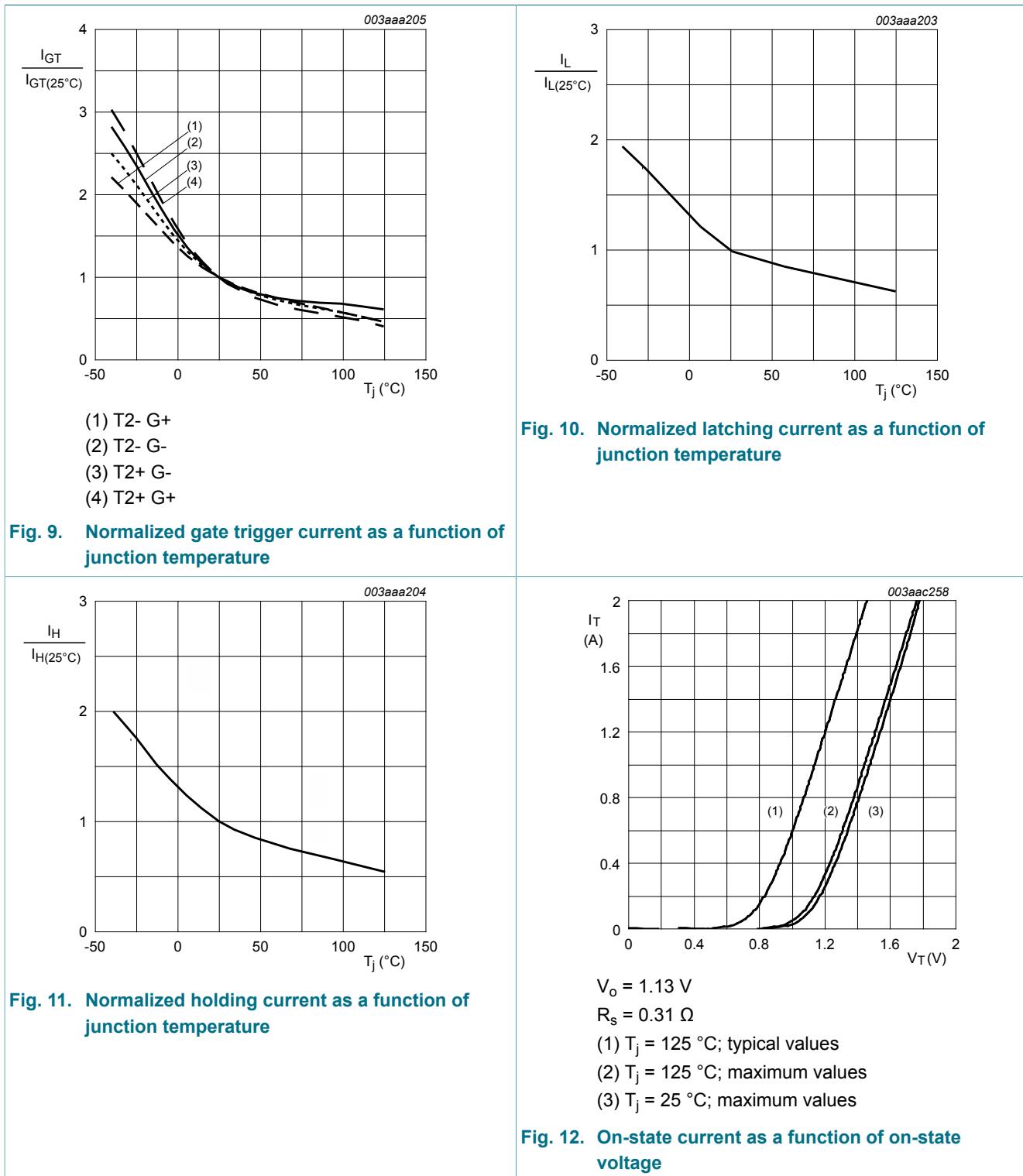
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 9	0.4	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 9	0.4	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 9	0.4	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2- G+; T _j = 25 °C; Fig. 9	0.4	-	10	mA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 10	-	-	15	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 10	-	-	30	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 10	-	-	15	mA
		V _D = 12 V; I _G = 0.1 A; T2- G+; T _j = 25 °C; Fig. 10	-	-	15	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 11	-	-	10	mA
V _T	on-state voltage	I _T = 1.4 A; T _j = 25 °C; Fig. 12	-	1.3	1.6	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 13	-	-	1	V
		V _D = 800 V; I _T = 0.1 A; T _j = 125 °C; Fig. 13	0.2	-	-	V
I _D	off-state current	V _D = 800 V; T _j = 125 °C	-	-	0.5	mA
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 110 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 14	120	-	-	V/μs
dV _{com} /dt	rate of change of commutating voltage	V _D = 400 V; T _j = 110 °C; dI _{com} /dt = 0.44 A/ms; gate open circuit	2	-	-	V/μs

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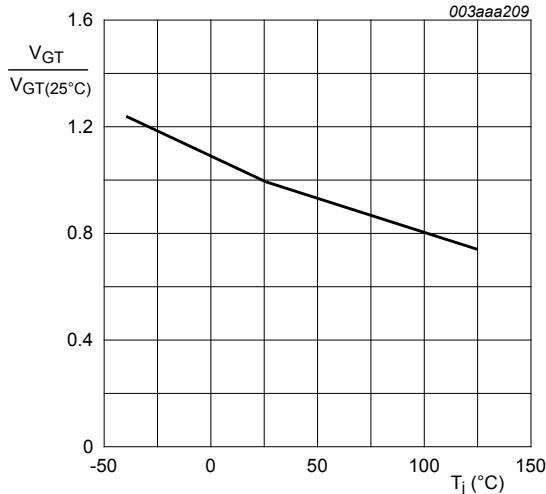


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

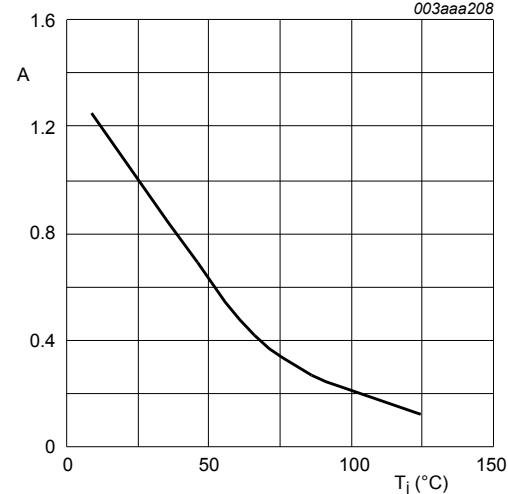


Fig. 14. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

$$A = \frac{dV_{D(T_j)} / dt}{dV_{D(25)} / dt}$$

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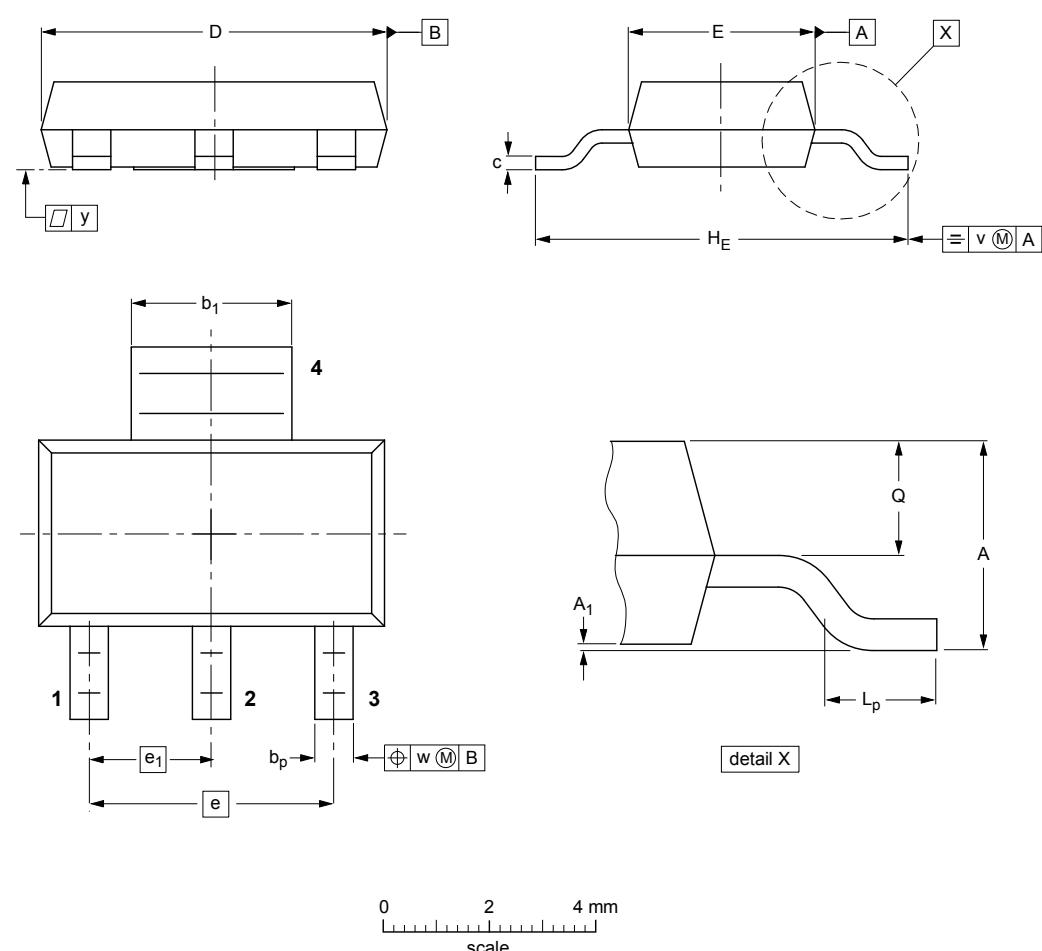
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11. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.8	0.10	0.80	3.1	0.32	6.7	3.7	4.6	2.3	7.3	1.1	0.95	0.2	0.1	0.1
	1.5	0.01	0.60	2.9	0.22	6.3	3.3			6.7	0.7	0.85			

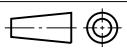
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			04-11-10 06-03-16

Fig. 15. Package outline SC-73 (SOT223)

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12. Soldering

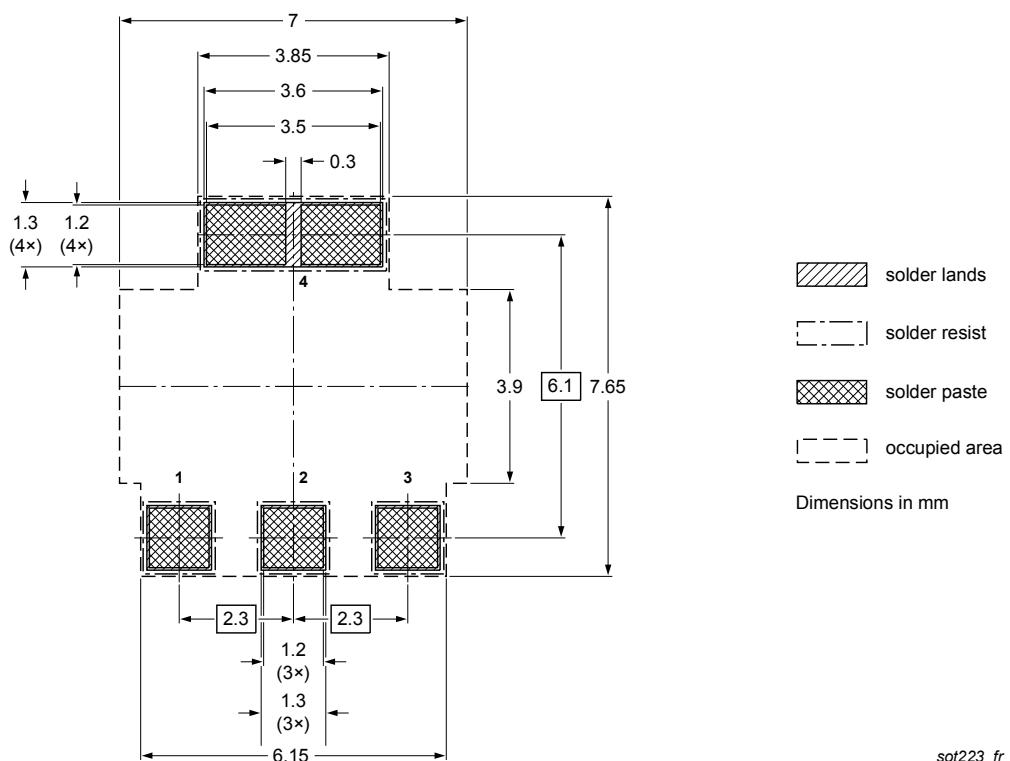


Fig. 16. Reflow soldering footprint for SC-73 (SOT223)

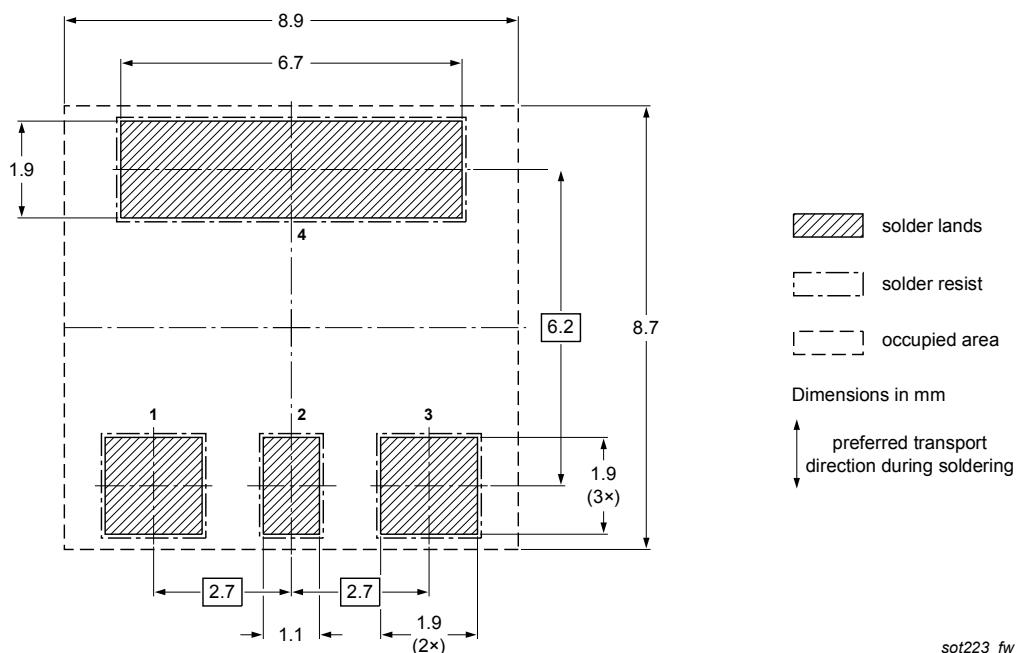


Fig. 17. Wave soldering footprint for SC-73 (SOT223)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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