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[Alpha & Omega Semiconductor Inc.](#)  
[AOD4189](#)

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## AOD4189

### P-Channel Enhancement Mode Field Effect Transistor

#### General Description

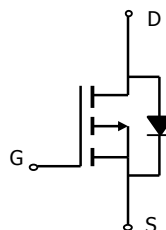
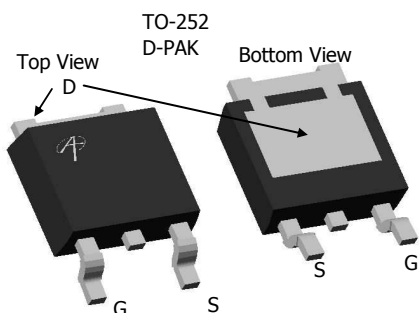
The AOD4189 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications.

- RoHS Compliant
- Halogen Free\*

#### Features

$V_{DS}$  (V) = -40V  
 $I_D$  = -40A ( $V_{GS}$  = -10V)  
 $R_{DS(ON)}$  < 22m $\Omega$  ( $V_{GS}$  = -10V)  
 $R_{DS(ON)}$  < 29m $\Omega$  ( $V_{GS}$  = -4.5V)

**100% UIS Tested!**  
**100% Rg Tested!**



#### Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B,H</sup>	$T_C=25^\circ\text{C}$	-40	A
	$T_C=100^\circ\text{C}$	-28	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-50	
Avalanche Current <sup>C</sup>	$I_{AR}$	-35	
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	61	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ\text{C}$	62.5	W
	$T_C=100^\circ\text{C}$	31	
Power Dissipation <sup>A</sup>	$T_A=25^\circ\text{C}$	2.5	
	$T_A=70^\circ\text{C}$	1.6	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A,G</sup>	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,G</sup>		Steady-State	41	50
Maximum Junction-to-Case <sup>D,F</sup>	$R_{\theta JC}$	2	2.4	$^\circ\text{C/W}$

**AOD4189**
**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =-250μA	-1.7	-1.9	-3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-50			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-12A T <sub>J</sub> =125°C		18 27	22 33	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-8A		23	29	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-12A		35		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.74	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-20	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-20V, f=1MHz		1870		pF
C <sub>oss</sub>	Output Capacitance			185		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			155		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	2.5	4.5	6.5	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (-10V)	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, I <sub>D</sub> =-12A		31.4	41	nC
Q <sub>g</sub> (-4.5V)	Total Gate Charge			7.9	10	
Q <sub>gs</sub>	Gate Source Charge			7.6		nC
Q <sub>gd</sub>	Gate Drain Charge			6.2		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, R <sub>L</sub> =1.6Ω, R <sub>GEN</sub> =3Ω		10		ns
t <sub>r</sub>	Turn-On Rise Time			18		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			38		ns
t <sub>f</sub>	Turn-Off Fall Time			24		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-12A, dI/dt=100A/μs		32	42	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-12A, dI/dt=100A/μs		30		nC

A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C. The power dissipation P<sub>DSM</sub> and current rating I<sub>DSM</sub> are based on T<sub>J(MAX)</sub>=150°C, using steady state junction-to-ambient thermal resistance.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using t ≤ 300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating.

G: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

H: The maximum current rating is limited by bond-wires.

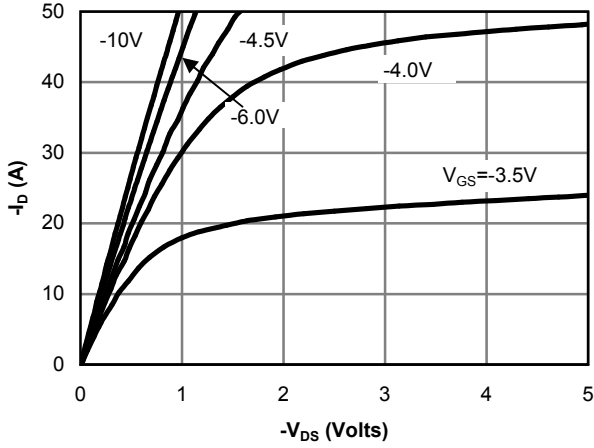
\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

Rev1: Oct 2008

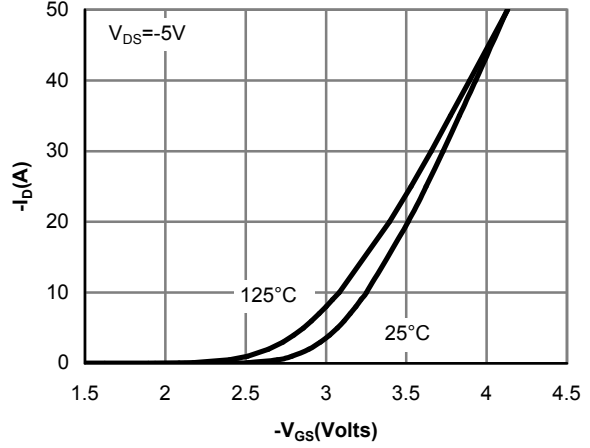
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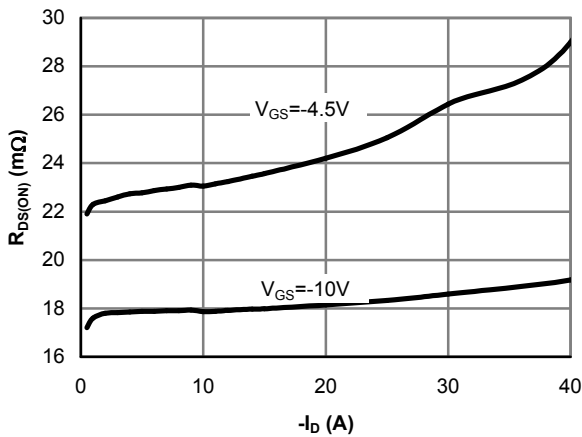
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



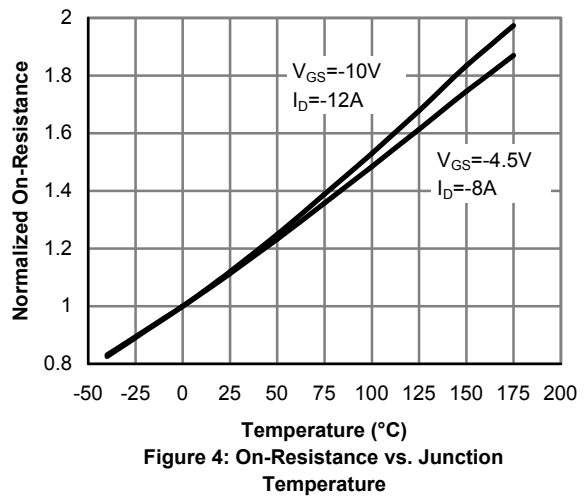
**Figure 1: On-Region Characteristics**



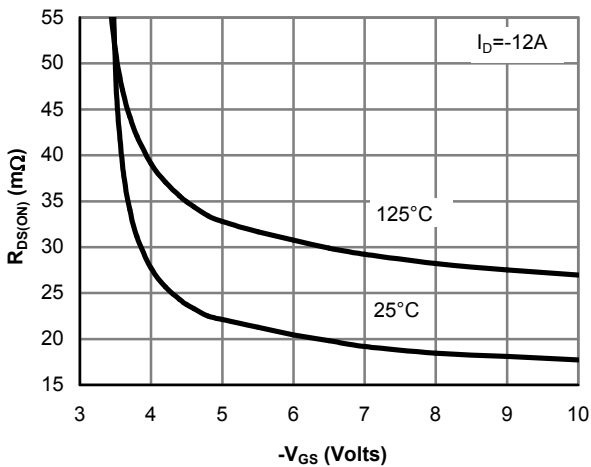
**Figure 2: Transfer Characteristics**



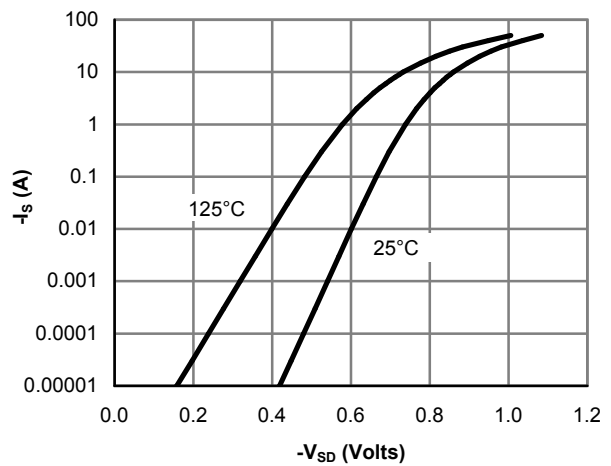
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



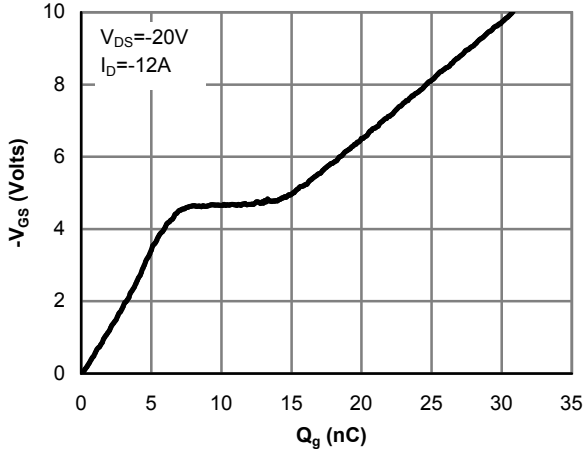
**Figure 5: On-Resistance vs. Gate-Source Voltage**



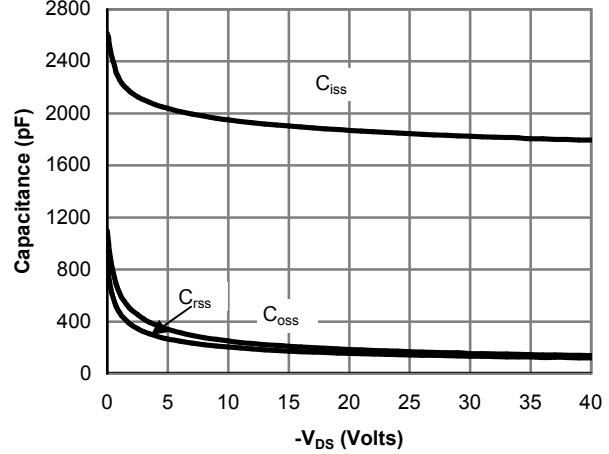
**Figure 6: Body-Diode Characteristics**

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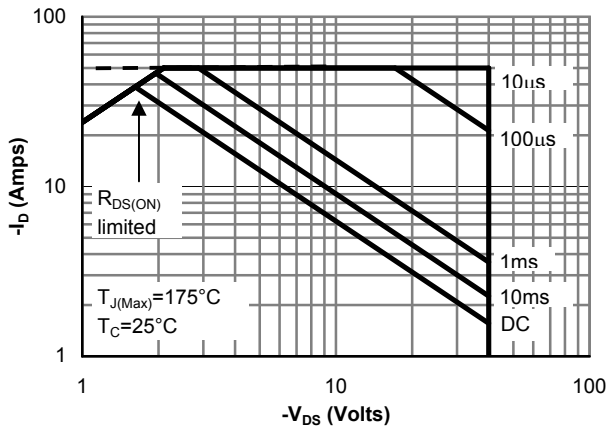
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



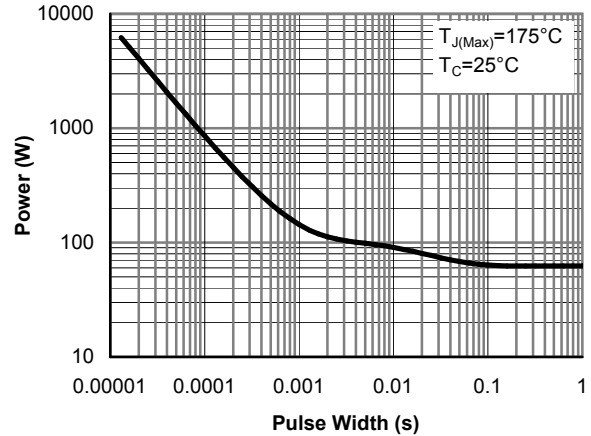
**Figure 7: Gate-Charge Characteristics**



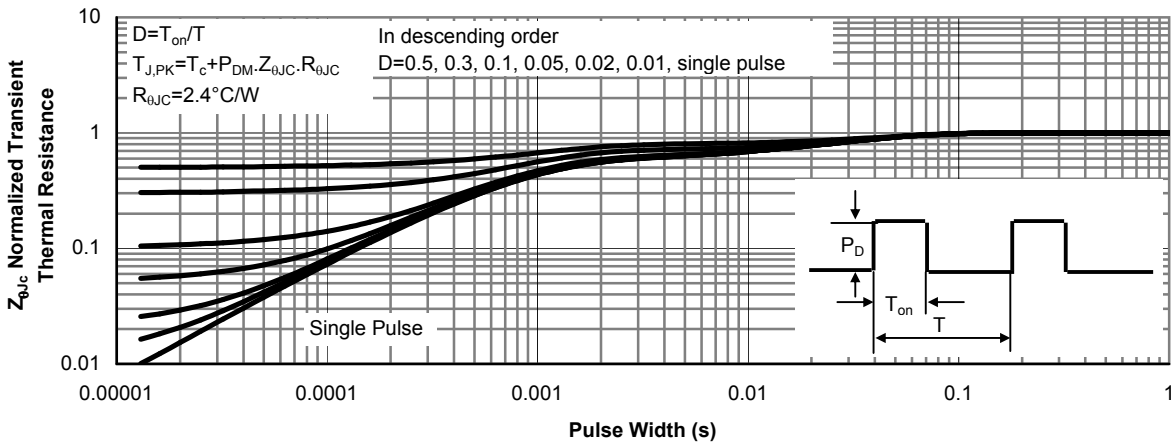
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

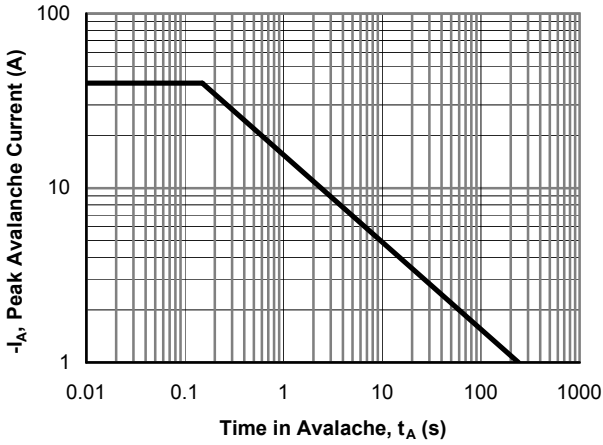


Figure 12: Single Pulse Avalanche Capability

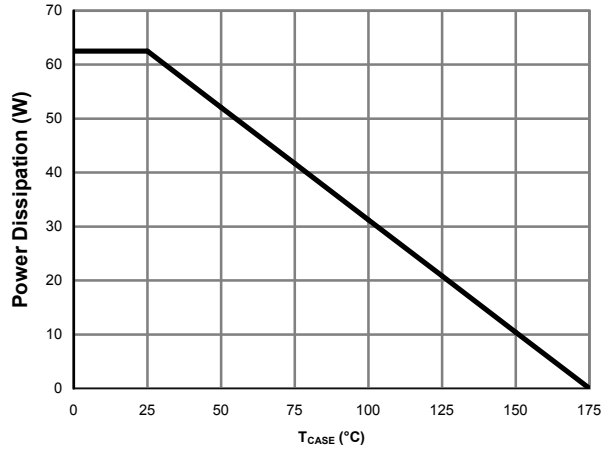


Figure 13: Power De-rating (Note B)

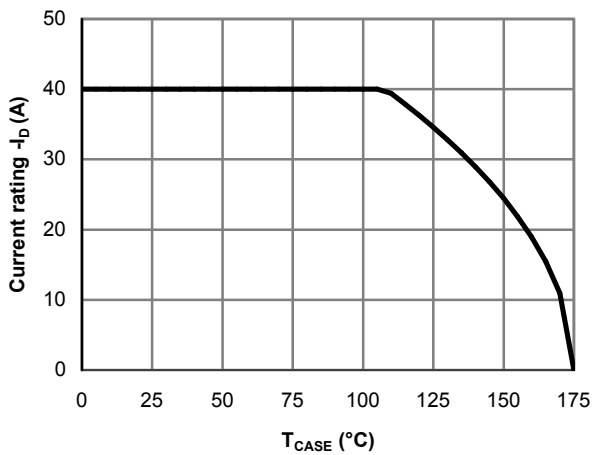


Figure 14: Current De-rating (Note B)

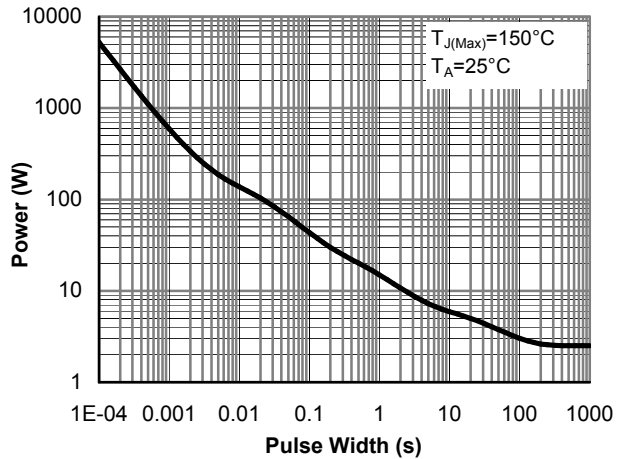


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

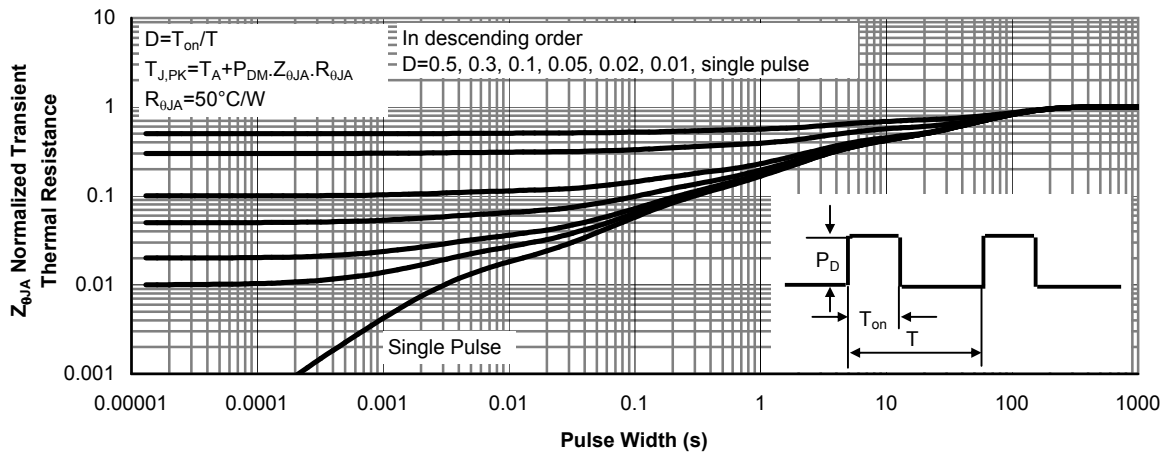
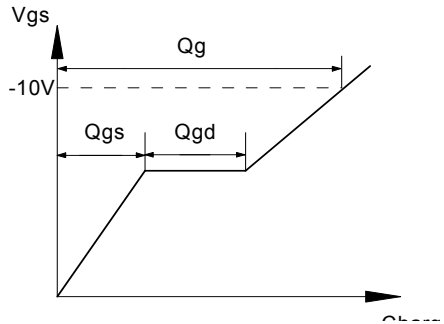
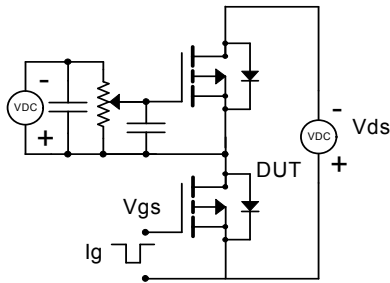


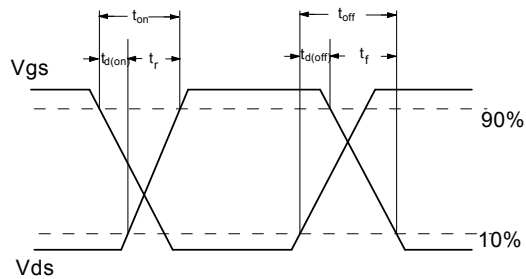
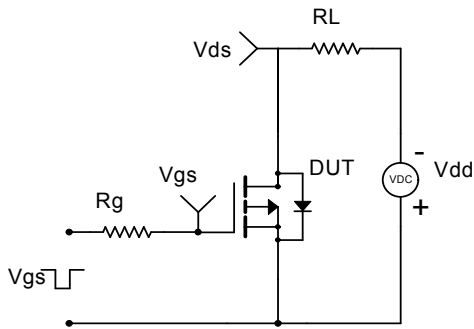
Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

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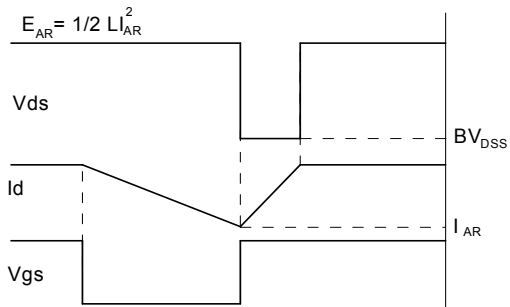
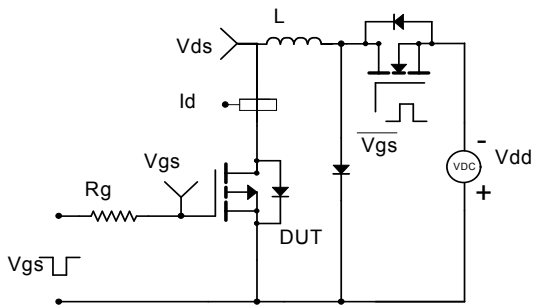
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

