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## TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS084F – APRIL 1994 – REVISED JANUARY 2002

- Complete PWM Power Control
- 3.6-V to 40-V Operation
- Internal Undervoltage-Lockout Circuit
- Internal Short-Circuit Protection
- Oscillator Frequency . . . 20 kHz to 500 kHz
- Variable Dead Time Provides Control Over Total Range
- $\pm 3\%$  Tolerance on Reference Voltage (TL5001A)
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

### description

The TL5001 and TL5001A incorporate on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5001/A contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout (UVLO), short-circuit protection (SCP), and an open-collector output transistor. The TL5001A has a typical reference voltage tolerance of  $\pm 3\%$  compared to  $\pm 5\%$  for the TL5001.

The error-amplifier common-mode voltage ranges from 0 V to 1.5 V. The noninverting input of the error amplifier is connected to a 1-V reference. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low  $V_{CC}$  conditions, the UVLO circuit turns the output off until  $V_{CC}$  recovers to its normal operating range.

The TL5001C and TL5001AC are characterized for operation from  $-20^\circ\text{C}$  to  $85^\circ\text{C}$ . The TL5001I and TL5001AI are characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The TL5001Q and TL5001AQ are characterized for operation from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . The TL5001M and TL5001AM are characterized for operation from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

### AVAILABLE OPTIONS

TA	PACKAGED DEVICES			
	SMALL OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)	CHIP CARRIER (FK)
$-20^\circ\text{C}$ to $85^\circ\text{C}$	TL5001CD	TL5001CP	—	—
	TL5001ACD	TL5001ACP	—	—
$-40^\circ\text{C}$ to $85^\circ\text{C}$	TL5001ID	TL5001IP	—	—
	TL5001AID	TL5001AIP	—	—
$-40^\circ\text{C}$ to $125^\circ\text{C}$	TL5001QD	—	—	—
	TL5001AQD	—	—	—
$-55^\circ\text{C}$ to $125^\circ\text{C}$	—	—	TL5001MJJ	TL5001MFK
	—	—	TL5001AMJJ	TL5001AMFK

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL5001CDR).



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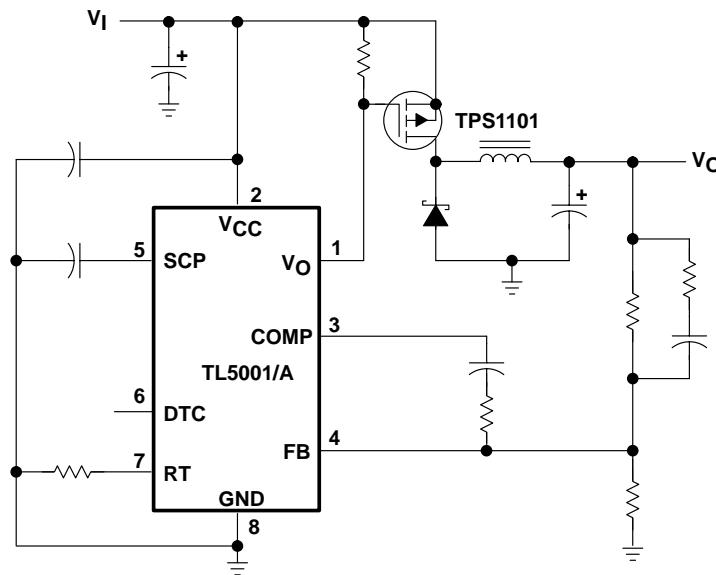


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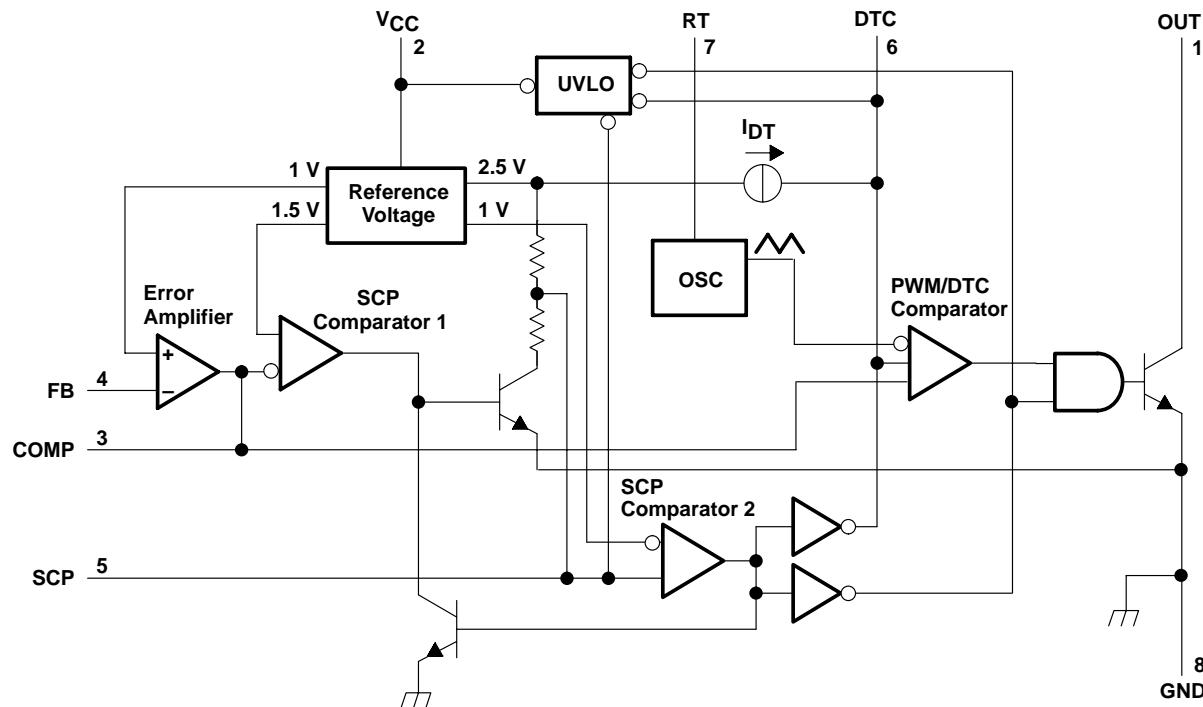
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### schematic for typical application



### functional block diagram



## TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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### detailed description

#### voltage reference

A 2.5-V regulator operating from  $V_{CC}$  is used to power the internal circuitry of the TL5001 and TL5001A and as a reference for the error amplifier and SCP circuits. A resistive divider provides a 1-V reference for the error amplifier noninverting input which typically is within 2% of nominal over the operating temperature range.

#### error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1-V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$$V_O = (1 + R1/R2) (1 \text{ V})$$

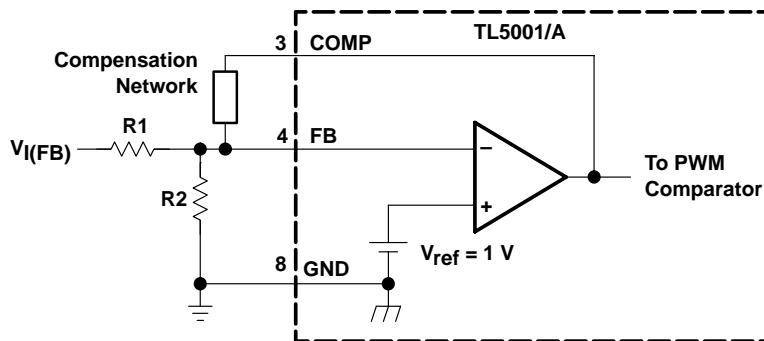


Figure 1. Error-Amplifier Gain Setting

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45  $\mu\text{A}$ , the total dc load resistance should be 100  $\text{k}\Omega$  or more.

#### oscillator/PWM

The oscillator frequency ( $f_{osc}$ ) can be set between 20 kHz and 500 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15  $\text{k}\Omega$  to 250  $\text{k}\Omega$ . The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

#### dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100%, which is critical for boost and flyback converters. A current source generates a reference current ( $I_{DT}$ ) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage ( $V_{DT}$ ), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when  $V_{DT}$  is 0.7 V or less and 100% when  $V_{DT}$  is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250  $\Omega$ ), choosing  $R_{DT}$  for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 ( $V_{oscmax}$  and  $V_{oscmin}$  are the maximum and minimum oscillator levels):

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### dead-time control (DTC) (continued)

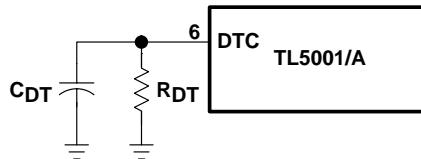
$$R_{DT} = (R_t + 1250) [D(V_{osc}^{max} - V_{osc}^{min}) + V_{osc}^{min}]$$

Where

$R_{DT}$  and  $R_t$  are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor ( $C_{DT}$ ) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT} R_{DT} \left( 1 - e^{-t/R_{DT}C_{DT}} \right)$$



**Figure 2. Soft-Start Circuit**

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant,  $R_{DT}C_{DT}$ , should be  $t_0/3$  to  $t_0/5$ . The TL5001/A remains off until  $V_{DT} \approx 0.7$  V, the minimum ramp value.  $C_{DT}$  is discharged every time UVLO or SCP becomes active.

### undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V at 25°C) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

### short-circuit protection (SCP)

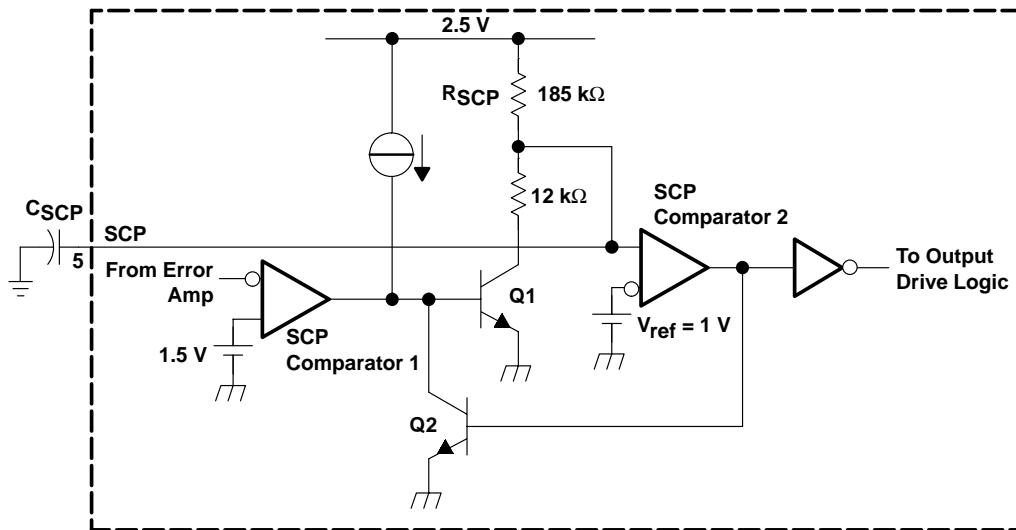
The TL5001/A includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5 V. If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns off the TL5001/A output transistor.

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**short-circuit protection (SCP) (continued)**



**Figure 3. SCP Circuit**

The timer operates by charging an external capacitor ( $C_{SCP}$ ), connected between the SCP terminal and ground, towards 2.5 V through a 185-kΩ resistor ( $R_{SCP}$ ). The circuit begins charging from an initial voltage of approximately 185 mV and times out when the capacitor voltage reaches 1 V. The output of SCP comparator 2 then goes high, turns on  $Q_2$ , and latches the timer circuit. The expression for setting the SCP time period is derived from the following equation:

$$V_{SCP} = (2.5 - 0.185)(1 - e^{-t/\tau}) + 0.185$$

Where

$$\tau = R_{SCP}C_{SCP}$$

The end of the time-out period,  $t_{SCP}$ , occurs when  $V_{SCP} = 1$  V. Solving for  $C_{SCP}$  yields:

$$C_{SCP} = 12.46 \times t_{SCP}$$

Where

$t$  is in seconds,  $C$  in  $\mu\text{F}$ .

$t_{SCP}$  must be much longer (generally 10 to 15 times) than the converter start-up period or the converter will not start.

**output transistor**

The output of the TL5001/A is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$ (see Note 1) .....	41 V
Amplifier input voltage, $V_{I(FB)}$ .....	20 V
Output voltage, $V_O$ , OUT .....	51 V
Output current, $I_O$ , OUT .....	21 mA
Output peak current, $I_{O(peak)}$ , OUT .....	100 mA
Continuous total power dissipation .....	See Dissipation Rating Table
Operating ambient temperature range, $T_A$ : TL5001C, TL5001AC .....	–20°C to 85°C
TL5001I, TL5001AI .....	–40°C to 85°C
TL5001Q, TL5001AQ .....	–40°C to 125°C
TL5001M, TL5001AM .....	–55°C to 125°C
Storage temperature range, $T_{Stg}$ .....	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds .....	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

## recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$		3.6	40	V
Amplifier input voltage, $V_{I(FB)}$		0	1.5	V
Output voltage, $V_O$ , OUT			50	V
Output current, $I_O$ , OUT			20	mA
COMP source current			45	µA
COMP dc load resistance		100		kΩ
Oscillator timing resistor, $R_t$		15	250	kΩ
Oscillator frequency, $f_{osc}$		20	500	kHz
Operating ambient temperature, $T_A$	TL5001C, TL5001AC	–20	85	°C
	TL5001I, TL5001AI	–40	85	
	TL5001Q, TL5001AQ	–40	125	
	TL5001M, TL5001AM	–55	125	

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**electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6$  V,  
 $f_{osc} = 100$  kHz (unless otherwise noted)**

**reference**

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output voltage	COMP connected to FB	0.95	1	1.05	0.97	1	1.03	V
Input regulation	$V_{CC} = 3.6$ V to 40 V		2	12.5		2	12.5	mV
Output voltage change with temperature	$T_A = -20^\circ\text{C}$ to $25^\circ\text{C}$ (C suffix)	-10	-1	10	-10	-1	10	mV/V
	$T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$ (I suffix)	-10	-1	10	-10	-1	10	
	$T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$	-10	-2	10	-10	-2	10	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

**undervoltage lockout**

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Upper threshold voltage	$T_A = 25^\circ\text{C}$		3			3		V
Lower threshold voltage	$T_A = 25^\circ\text{C}$		2.8			2.8		V
Hysteresis	$T_A = 25^\circ\text{C}$	100	200		100	200		mV
Reset threshold voltage	$T_A = 25^\circ\text{C}$	2.1	2.55		2.1	2.55		V

† All typical values are at  $T_A = 25^\circ\text{C}$ .

**short-circuit protection**

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
SCP threshold voltage	$T_A = 25^\circ\text{C}$	0.95	1.00	1.05	0.97	1.00	1.03	V
SCP voltage, latched	No pullup	140	185	230	140	185	230	mV
SCP voltage, UVLO standby	No pullup		60	120		60	120	mV
Input source current	$T_A = 25^\circ\text{C}$	-10	-15	-20	-10	-15	-20	$\mu\text{A}$
SCP comparator 1 threshold voltage			1.5			1.5		V

† All typical values are at  $T_A = 25^\circ\text{C}$ .

**oscillator**

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Frequency	$R_t = 100$ k $\Omega$		100			100		kHz
Standard deviation of frequency			15			15		kHz
Frequency change with voltage	$V_{CC} = 3.6$ V to 40 V		1			1		kHz
Frequency change with temperature	$T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	-4	-0.4	4	-4	-0.4	4	kHz
	$T_A = -20^\circ\text{C}$ to $25^\circ\text{C}$	-4	-0.4	4	-4	-0.4	4	kHz
	$T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$	-4	-0.2	4	-4	-0.2	4	kHz
Voltage at RT			1			1		V

† All typical values are at  $T_A = 25^\circ\text{C}$ .



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## TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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**electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6$  V,  $f_{osc} = 100$  kHz (unless otherwise noted) (continued)**

### dead-time control

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output (source) current	TL5001C	$V_{(DT)} = 1.5$ V	$0.9 \times I_{RT}^{\ddagger}$	$1.1 \times I_{RT}$	$0.9 \times I_{RT}^{\ddagger}$	$1.1 \times I_{RT}$		µA
	TL5001I	$V_{(DT)} = 1.5$ V	$0.9 \times I_{RT}^{\ddagger}$	$1.2 \times I_{RT}$	$0.9 \times I_{RT}^{\ddagger}$	$1.2 \times I_{RT}$		
Input threshold voltage		Duty cycle = 0%	0.5	0.7	0.5	0.7		V
		Duty cycle = 100%		1.3	1.5		1.3	1.5

† All typical values are at  $T_A = 25$ °C.

‡ Output source current at RT

### error amplifier

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Input voltage	$V_{CC} = 3.6$ V to 40 V	0	1.5		0	1.5		V
Input bias current			-160	-500		-160	-500	nA
Output voltage swing	Positive		1.5	2.3		1.5	2.3	V
	Negative		0.3	0.4		0.3	0.4	
Open-loop voltage amplification			80			80		dB
Unity-gain bandwidth			1.5			1.5		MHz
Output (sink) current	$V_{I(FB)} = 1.2$ V, COMP = 1 V	100	600		100	600		µA
Output (source) current	$V_{I(FB)} = 0.8$ V, COMP = 1 V	-45	-70		-45	-70		µA

† All typical values are at  $T_A = 25$ °C.

### output

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output saturation voltage	$I_O = 10$ mA		1.5	2		1.5	2	V
Off-state current	$V_O = 50$ V, $V_{CC} = 0$			10			10	µA
	$V_O = 50$ V			10			10	
Short-circuit output current	$V_O = 6$ V		40			40		mA

† All typical values are at  $T_A = 25$ °C.

### total device

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Standby supply current	Off state		1	1.5		1	1.5	mA
Average supply current	$R_t = 100$ kΩ		1.4	2.1		1.4	2.1	mA

† All typical values are at  $T_A = 25$ °C.

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**electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6$  V,  
 $f_{osc} = 100$  kHz (unless otherwise noted)**

**reference**

PARAMETER	TEST CONDITIONS	TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output voltage	$T_A = 25^\circ C$	COMP connected to FB	0.95	1.00	1.05	0.97	1.00	1.03
	$T_A = \text{MIN to MAX}$		0.93	0.98	1.07	0.94	0.98	1.06
Input regulation	$T_A = \text{MIN to MAX}$	$V_{CC} = 3.6$ V to 40 V		2	12.5	2	12.5	mV
Output voltage change with temperature	$T_A = \text{MIN to MAX}$			*-6	2	*6	*-6	%

† All typical values are at  $T_A = 25^\circ C$ .

\*Not production tested.

**undervoltage lockout**

PARAMETER	TEST CONDITIONS	TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Upper threshold voltage	$T_A = \text{MIN, } 25^\circ C$	3.00	3.00	2.55	2.55	2.55	2.55	V
	$T_A = \text{MAX}$							
Lower threshold voltage	$T_A = \text{MIN, } 25^\circ C$	2.8	2.8	2.0	2.0	2.0	2.0	V
	$T_A = \text{MAX}$							
Hysteresis	$T_A = \text{MIN to MAX}$	100	200	100	200	100	200	mV
Reset threshold voltage	$T_A = \text{MIN, } 25^\circ C$	2.10	2.55	2.10	2.55	2.10	2.55	V
	$T_A = \text{MAX}$	0.35	0.63	0.35	0.63	0.35	0.63	

† All typical values are at  $T_A = 25^\circ C$ .

**short-circuit protection**

PARAMETER	TEST CONDITIONS	TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
SCP threshold voltage	$T_A = \text{MIN, } 25^\circ C$	0.95	1.00	1.05	0.97	1.00	1.03	V
	$T_A = \text{MAX}$	0.93	0.98	1.07	0.94	0.98	1.06	
SCP voltage, latched	$T_A = \text{MIN to MAX}$	No pullup		140	185	230	140	185
SCP voltage, UVLO standby	$T_A = \text{MIN to MAX}$	No pullup		60	120	60	120	mV
Equivalent timing resistance	$T_A = \text{MIN to MAX}$			185			185	kΩ
SCP comparator 1 threshold voltage	$T_A = \text{MIN to MAX}$			1.5			1.5	V

† All typical values are at  $T_A = 25^\circ C$ .

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**electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6$  V,  $f_{osc} = 100$  kHz (unless otherwise noted) (continued)**

### oscillator

PARAMETER	TEST CONDITIONS	TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Frequency	$T_A = \text{MIN to MAX}$ $R_t = 100$ k $\Omega$	100			100			kHz
Standard deviation of frequency	$T_A = \text{MIN to MAX}$		2			2		kHz
Frequency change with voltage	$T_A = \text{MIN to MAX}$ $V_{CC} = 3.6$ V to 40 V		1			1		kHz
Frequency change with temperature	$T_A = \text{MIN to MAX}$	Q suffix	*-6	3	*6	*-6	3	*6
		M suffix	*-9	5	*9	*-9	5	*9
Voltage at RT	$T_A = \text{MIN to MAX}$		1			1		V

† All typical values are at  $T_A = 25^\circ\text{C}$ .

\*Not production tested.

### dead-time control

PARAMETER	TEST CONDITIONS	TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output (source) current	$T_A = \text{MIN to MAX}$ $V_{(DT)} = 1.5$ V	$0.9 \times I_{RT}^\ddagger$		$1.1 \times I_{RT}$	$0.9 \times I_{RT}^\ddagger$		$1.1 \times I_{RT}$	$\mu\text{A}$
Input threshold voltage	$T_A = 25^\circ\text{C}$	Duty cycle = 0%	0.5	0.7	0.5	0.7		V
		Duty cycle = 100%	1.3	1.5		1.3	1.5	
	$T_A = \text{MIN to MAX}$	Duty cycle = 0%	0.4	0.7	0.4	0.7		
		Duty cycle = 100%	1.3	1.7		1.3	1.7	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

‡ Output source current at RT

### error amplifier

PARAMETER	TEST CONDITIONS	TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Input bias current	$T_A = \text{MIN to MAX}$		-160	-500		-160	-500	nA
Output voltage swing	$T_A = \text{MIN to MAX}$		1.5	2.3	1.5	2.3		V
			0.3	0.4		0.3	0.4	V
Open-loop voltage amplification	$T_A = \text{MIN to MAX}$		80			80		dB
Unity-gain bandwidth	$T_A = \text{MIN to MAX}$		1.5			1.5		MHz
Output (sink) current	$T_A = \text{MIN to MAX}$ $V_{I(FB)} = 1.2$ V, COMP = 1 V	100	600		100	600		$\mu\text{A}$
Output (source) current	$T_A = \text{MIN, } 25^\circ\text{C}$ $V_{I(FB)} = 0.8$ V, COMP = 1 V	-45	-70		-45	-70		$\mu\text{A}$
		-30	-45		-30	-45		

† All typical values are at  $T_A = 25^\circ\text{C}$ .



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**TL5001, TL5001A**  
**PULSE-WIDTH-MODULATION CONTROL CIRCUITS**

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**electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6$  V,  
 $f_{osc} = 100$  kHz (unless otherwise noted) (continued)**

**output**

PARAMETER	TEST CONDITIONS			TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Output saturation voltage	$T_A = \text{MIN to MAX}$	$I_O = 10$ mA		1.5	2		1.5	2		V
Off-state current	$T_A = \text{MIN to MAX}$	$V_O = 50$ V, $V_{CC} = 0$			10			10		$\mu\text{A}$
		$V_O = 50$ V			10			10		
Short-circuit output current	$T_A = \text{MIN to MAX}$	$V_O = 6$ V			40			40		mA

† All typical values are at  $T_A = 25^\circ\text{C}$ .

**total device**

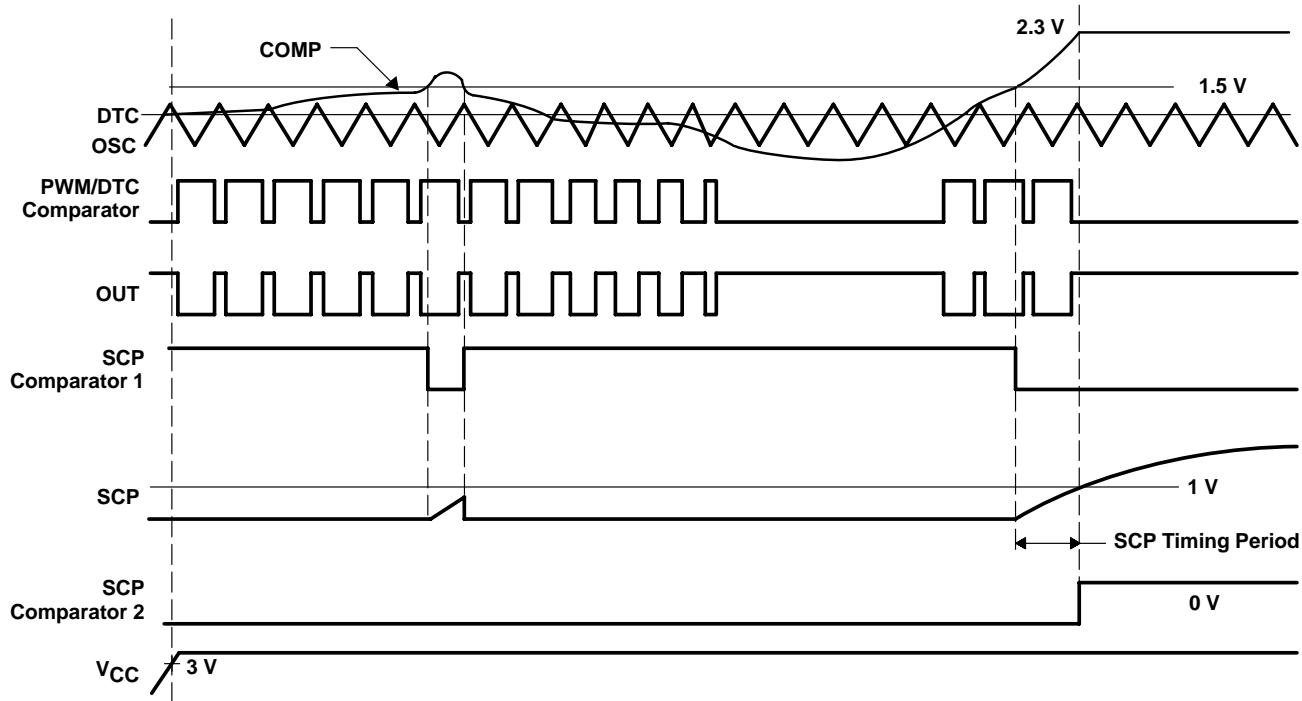
PARAMETER	TEST CONDITIONS			TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
Standby supply current	Off state	$T_A = \text{MIN to MAX}$		1	1.5		1	1.5		mA
Average supply current		$T_A = \text{MIN to MAX}$	$R_t = 100$ k $\Omega$	1.4	2.1		1.4	2.1		mA

† All typical values are at  $T_A = 25^\circ\text{C}$ .

**TL5001, TL5001A**  
**PULSE-WIDTH-MODULATION CONTROL CIRCUITS**

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**PARAMETER MEASUREMENT INFORMATION**



NOTE A: The waveforms show timing characteristics for an intermittent short circuit and a longer short circuit that is sufficient to activate SCP.

**Figure 4. PWM Timing Diagram**

**TL5001, TL5001A**  
**PULSE-WIDTH-MODULATION CONTROL CIRCUITS**

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**TYPICAL CHARACTERISTICS**

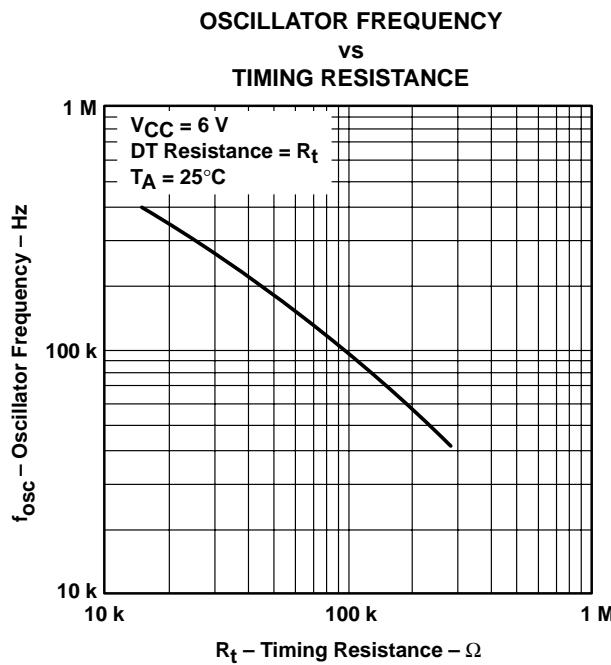


Figure 5

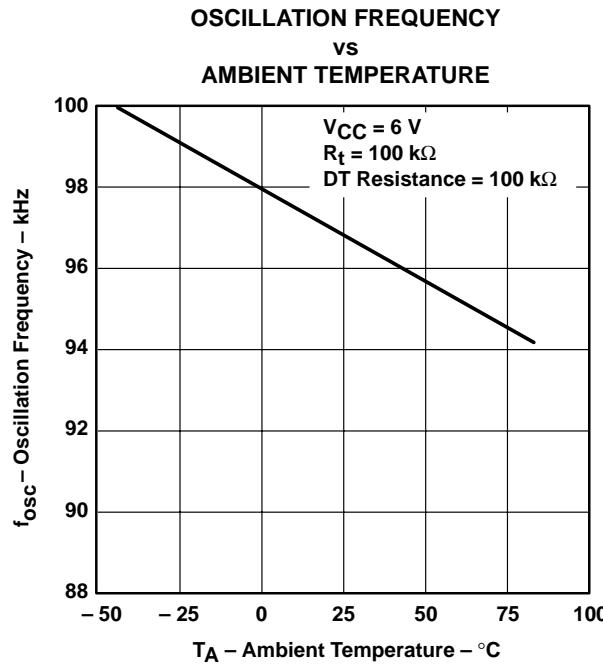


Figure 6

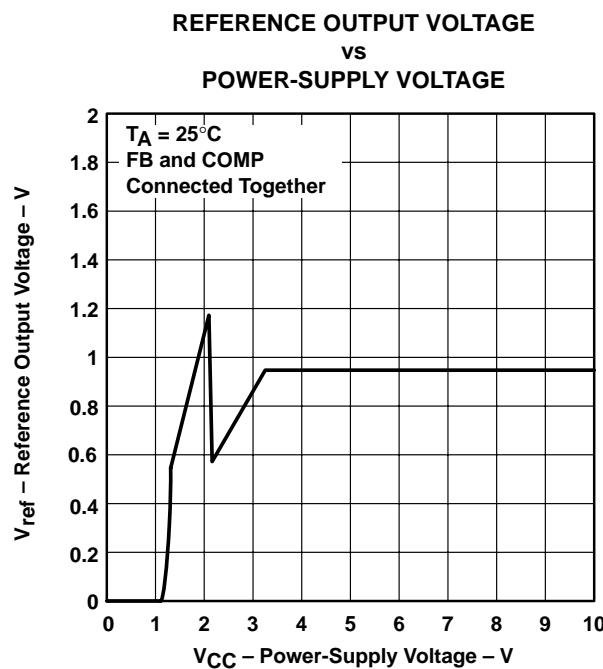


Figure 7

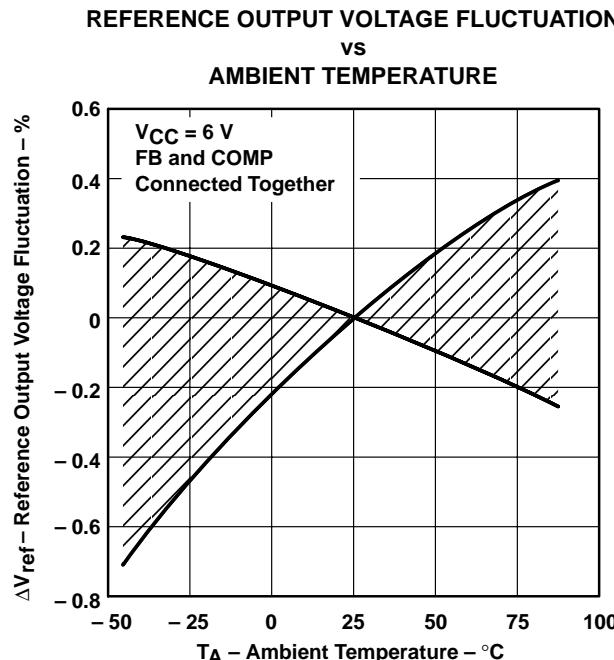


Figure 8

# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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## TYPICAL CHARACTERISTICS

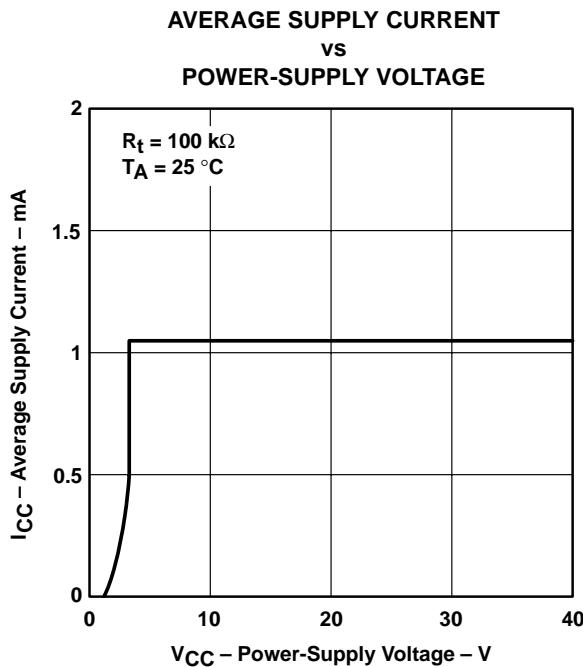


Figure 9

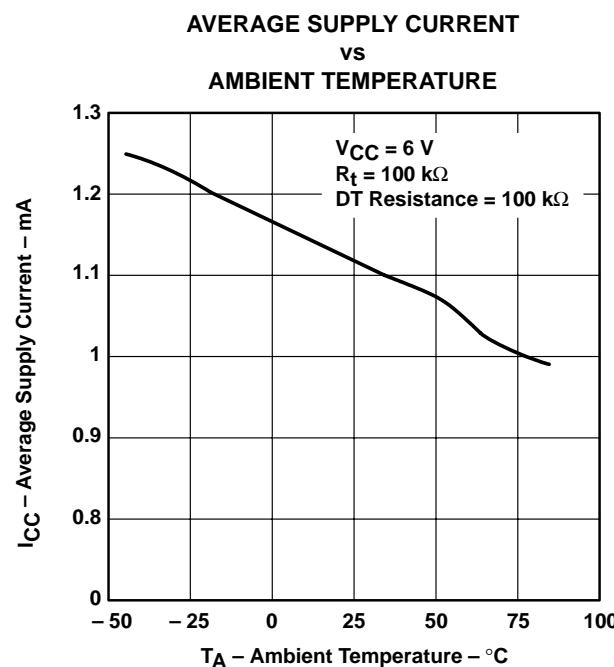


Figure 10

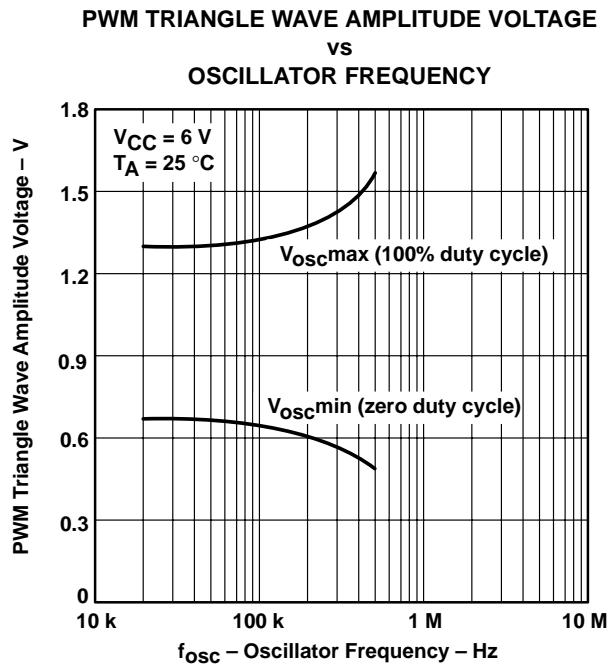


Figure 11

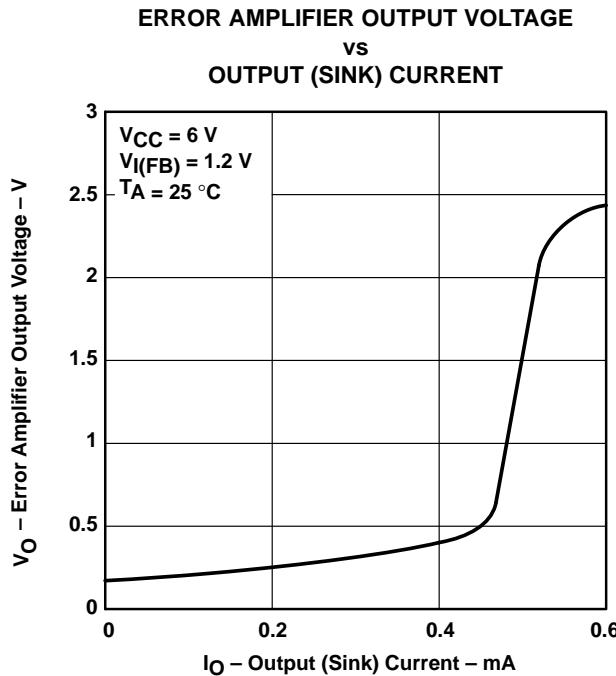


Figure 12

**TL5001, TL5001A**  
**PULSE-WIDTH-MODULATION CONTROL CIRCUITS**

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**TYPICAL CHARACTERISTICS**

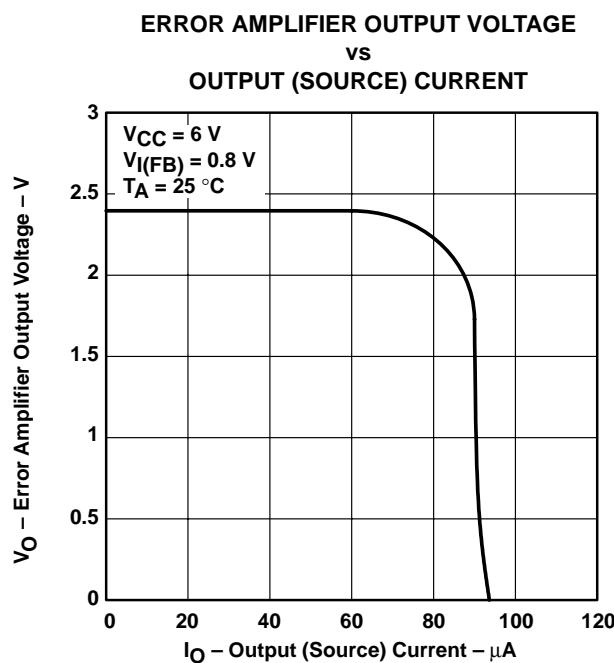


Figure 13

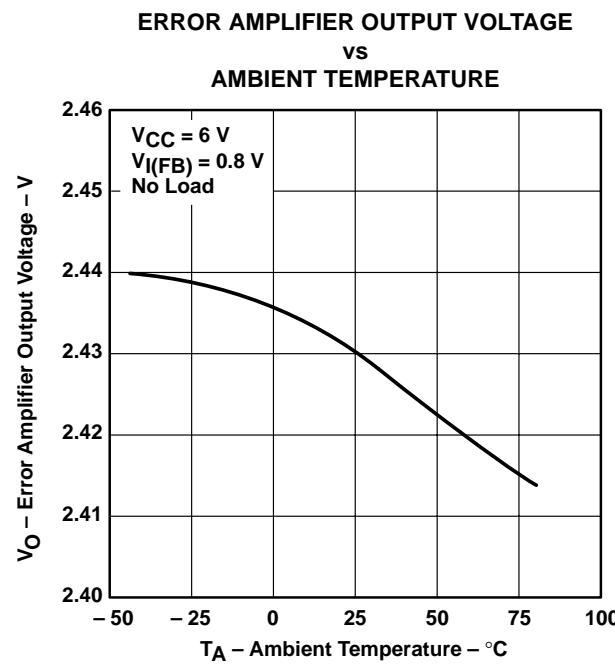


Figure 14

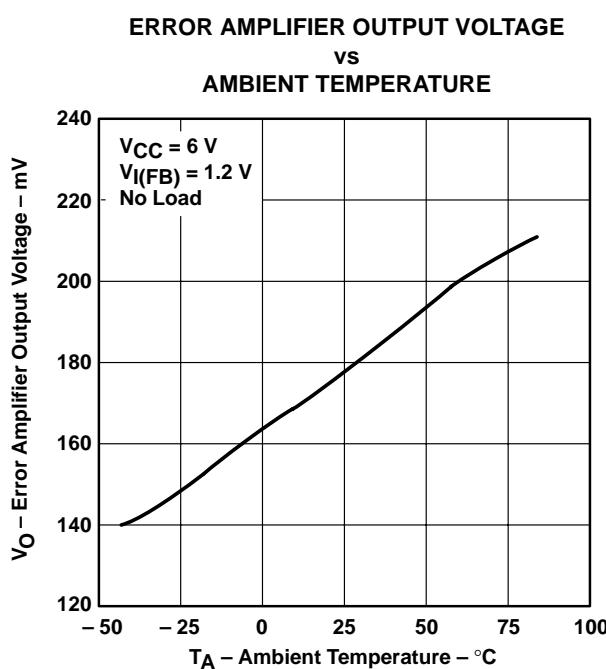


Figure 15

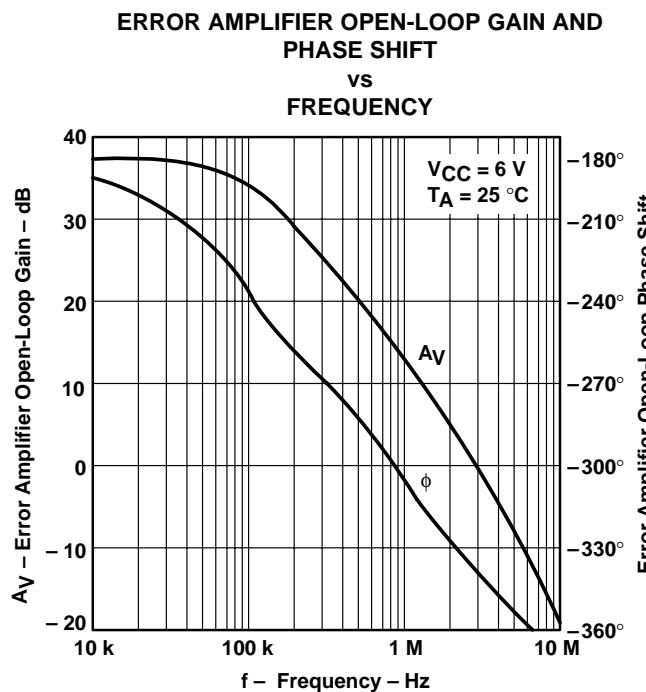


Figure 16

# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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## TYPICAL CHARACTERISTICS

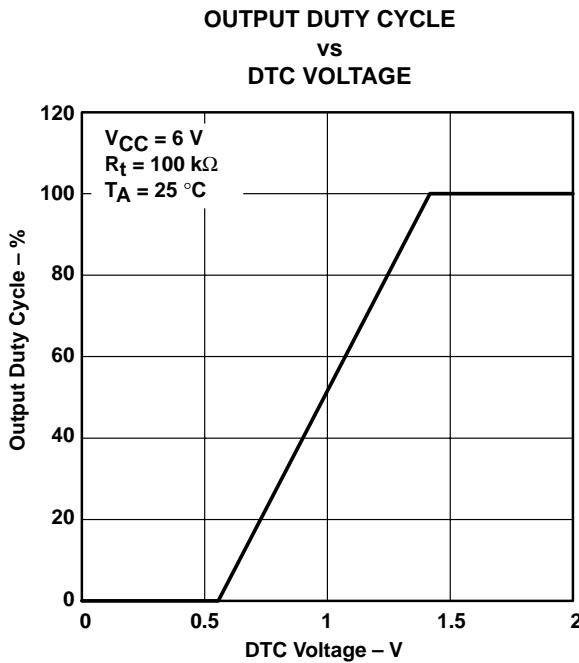


Figure 17

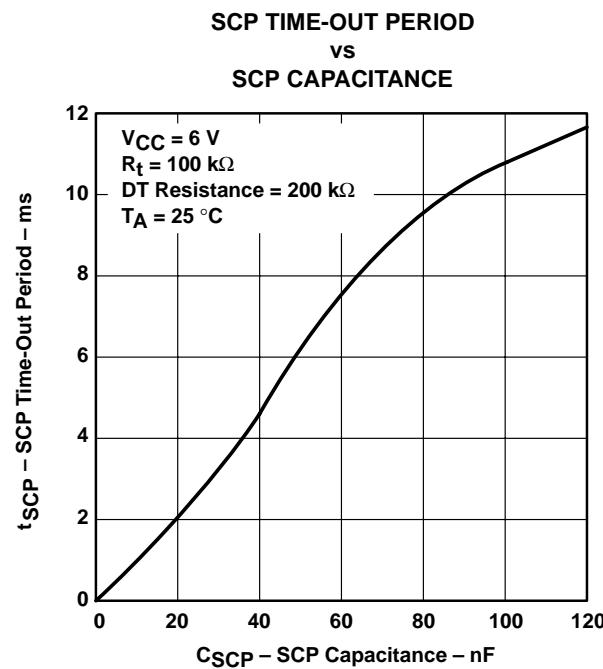


Figure 18

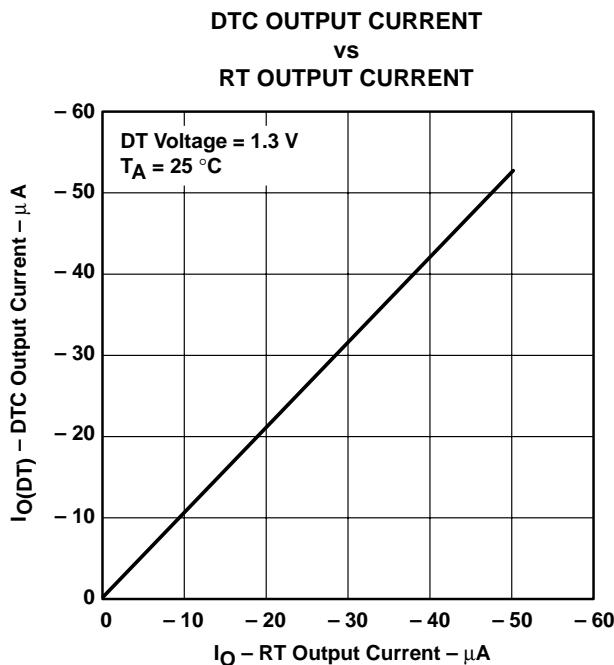


Figure 19

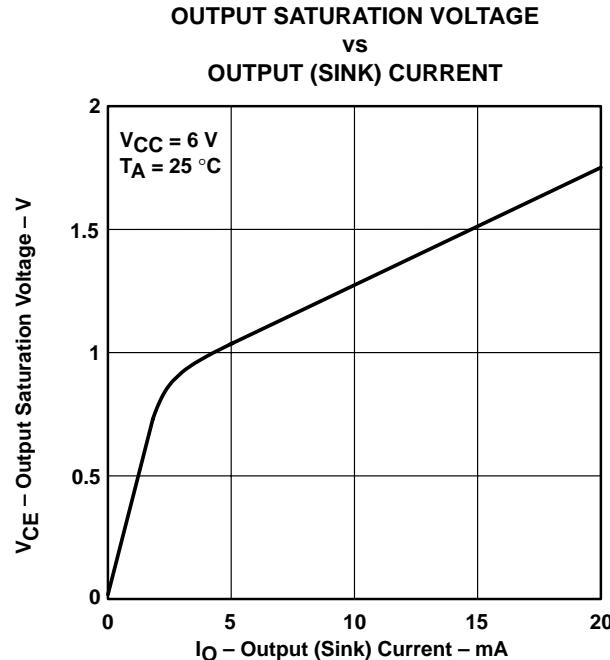
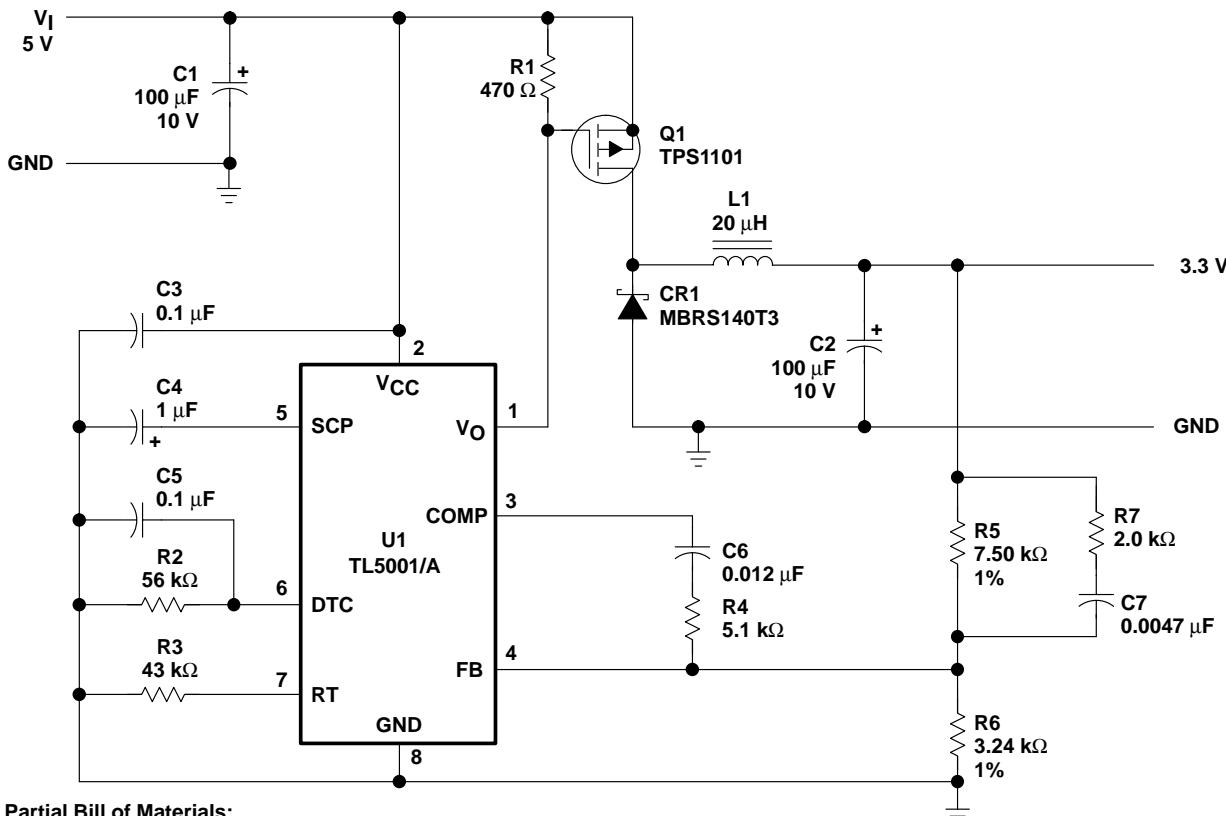


Figure 20

**TL5001, TL5001A**  
**PULSE-WIDTH-MODULATION CONTROL CIRCUITS**

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**APPLICATION INFORMATION**



**Partial Bill of Materials:**

U1	TL5001/A	Texas Instruments
Q1	TPS1101	Texas Instruments
LI	CTX20-1 or 23 turns of #28 wire on Micrometals No. T50-26B core	Coiltronics
C1	TPSD107M010R0100	AVX
C2	TPSD107M010R0100	AVX
CR1	MBRS140T3	Motorola

NOTES: A. Frequency = 200 kHz  
B. Duty cycle = 90% max  
C. Soft-start time constant (TC) = 5.6 ms  
D. SCP TC = 70 msA

**Figure 21. Step-Down Converter**

**TL5001, TL5001A**  
**PULSE-WIDTH-MODULATION CONTROL CIRCUITS**

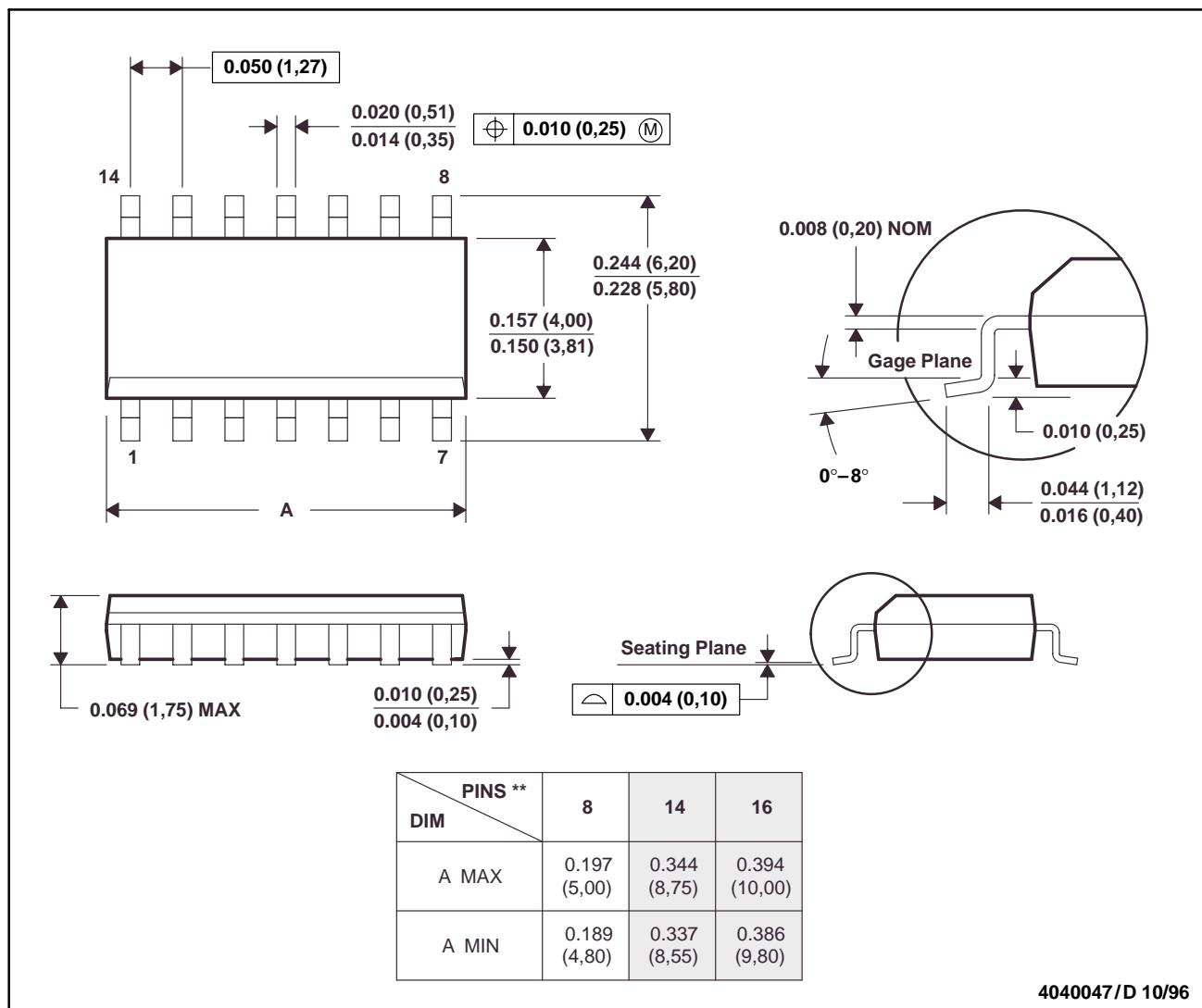
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**MECHANICAL DATA**

**D (R-PDSO-G\*\*)**

14 PIN SHOWN

**PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:

- B. All linear dimensions are in inches (millimeters).
- C. This drawing is subject to change without notice.
- D. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0.15).
- E. Falls within JEDEC MS-012

**TL5001, TL5001A**  
**PULSE-WIDTH-MODULATION CONTROL CIRCUITS**

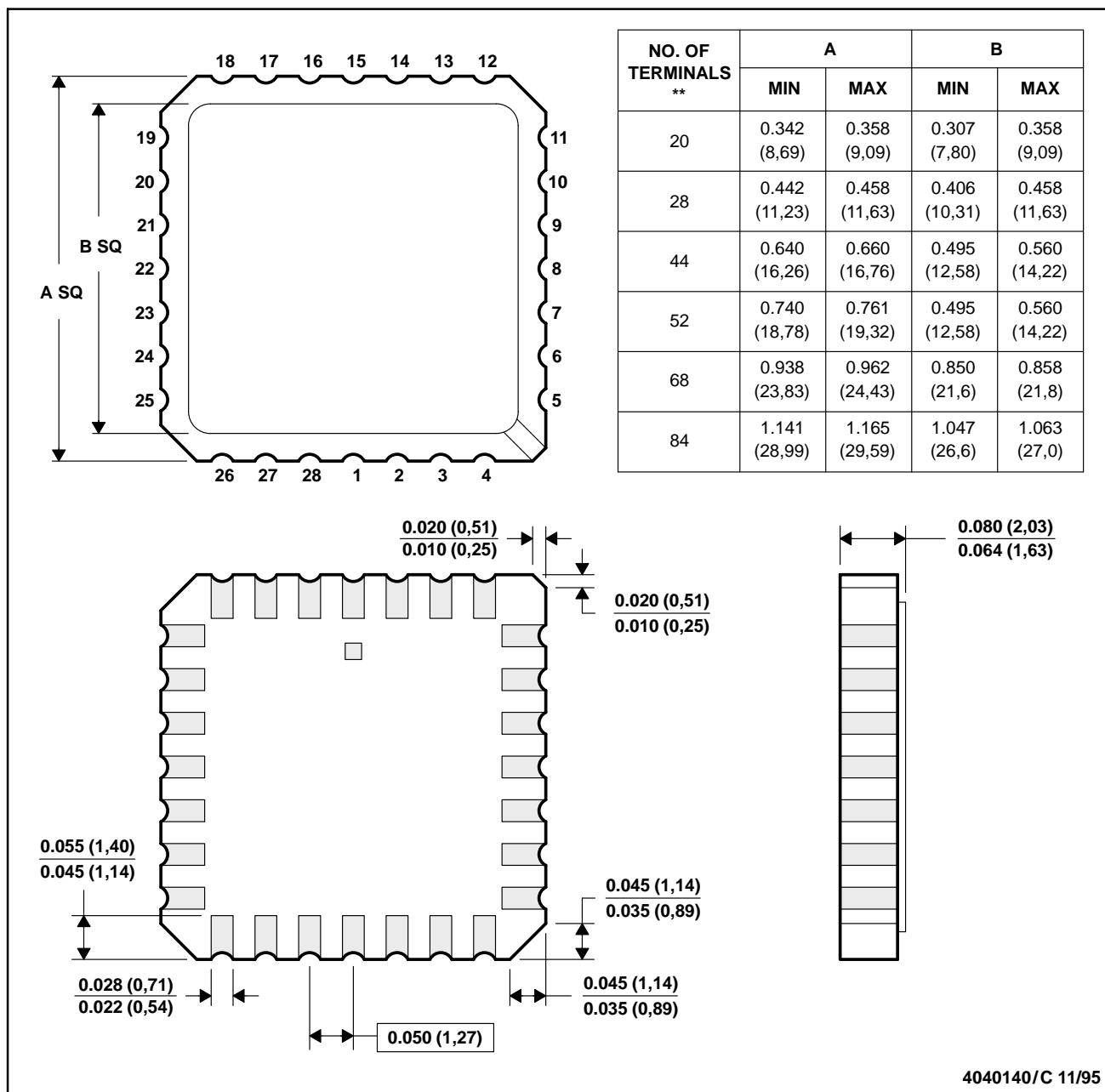
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**MECHANICAL DATA**

**FK (S-CQCC-N\*\*)**

28 TERMINALS SHOWN

**LEADLESS CERAMIC CHIP CARRIER**



4040140/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a metal lid.  
 D. The terminals are gold-plated.  
 E. Falls within JEDEC MS-004

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9958301QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9958301QPA TL5001M	<a href="#">Samples</a>
5962-9958302Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9958302Q2A TL5001 AMFKB	<a href="#">Samples</a>
5962-9958302QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9958302QPA TL5001AM	<a href="#">Samples</a>
TL5001ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	<a href="#">Samples</a>
TL5001ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	<a href="#">Samples</a>
TL5001ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	<a href="#">Samples</a>
TL5001ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	<a href="#">Samples</a>
TL5001AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	<a href="#">Samples</a>
TL5001AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	<a href="#">Samples</a>
TL5001AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	<a href="#">Samples</a>
TL5001AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	<a href="#">Samples</a>
TL5001AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5001AIP	<a href="#">Samples</a>
TL5001AIP4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5001AIP	<a href="#">Samples</a>
TL5001AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9958302Q2A TL5001 AMFKB	<a href="#">Samples</a>
TL5001AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9958302QPA TL5001AM	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL5001AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001AQ	<a href="#">Samples</a>
TL5001AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		5001AQ	<a href="#">Samples</a>
TL5001AQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001AQ	<a href="#">Samples</a>
TL5001AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		5001AQ	<a href="#">Samples</a>
TL5001CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	<a href="#">Samples</a>
TL5001CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	<a href="#">Samples</a>
TL5001CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	<a href="#">Samples</a>
TL5001CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	<a href="#">Samples</a>
TL5001CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	TL5001CP	<a href="#">Samples</a>
TL5001CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	TL5001CP	<a href="#">Samples</a>
TL5001CPS	ACTIVE	SO	PS	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		T5001	<a href="#">Samples</a>
TL5001CPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI			
TL5001CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	T5001	<a href="#">Samples</a>
TL5001CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	T5001	<a href="#">Samples</a>
TL5001ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001I	<a href="#">Samples</a>
TL5001IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001I	<a href="#">Samples</a>
TL5001IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001I	<a href="#">Samples</a>
TL5001IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL5001IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5001IP	<a href="#">Samples</a>
TL5001IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL5001IP	<a href="#">Samples</a>
TL5001IPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Z5001	<a href="#">Samples</a>
TL5001MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL5001MJG	<a href="#">Samples</a>
TL5001MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9958301QPA TL5001M	<a href="#">Samples</a>
TL5001QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001Q	<a href="#">Samples</a>
TL5001QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		5001Q	<a href="#">Samples</a>
TL5001QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001Q	<a href="#">Samples</a>
TL5001QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		5001Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL5001, TL5001A, TL5001AM, TL5001M :**

• Catalog: [TL5001A](#), [TL5001](#)

• Automotive: [TL5001A-Q1](#), [TL5001A-Q1](#)

• Military: [TL5001M](#), [TL5001AM](#)

**NOTE: Qualified Version Definitions:**

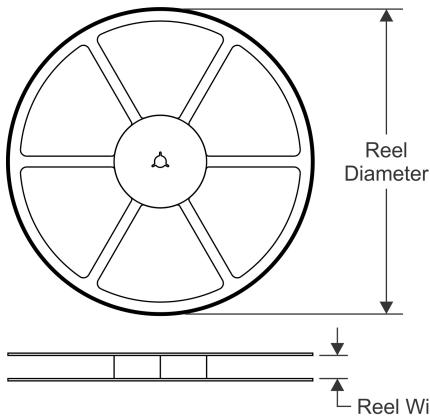
• Catalog - TI's standard catalog product

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

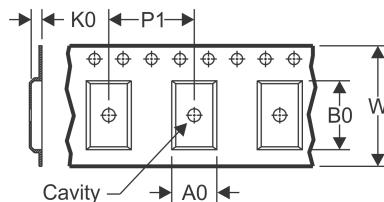
• Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

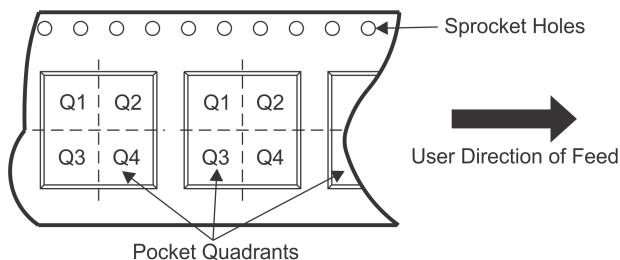


**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

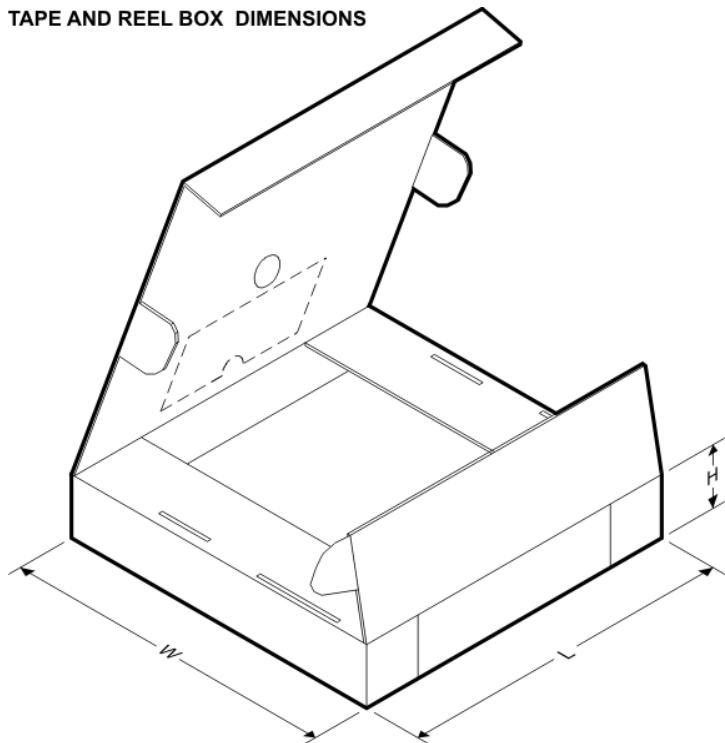
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL5001ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001AQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001AQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL5001IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001IPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL5001QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



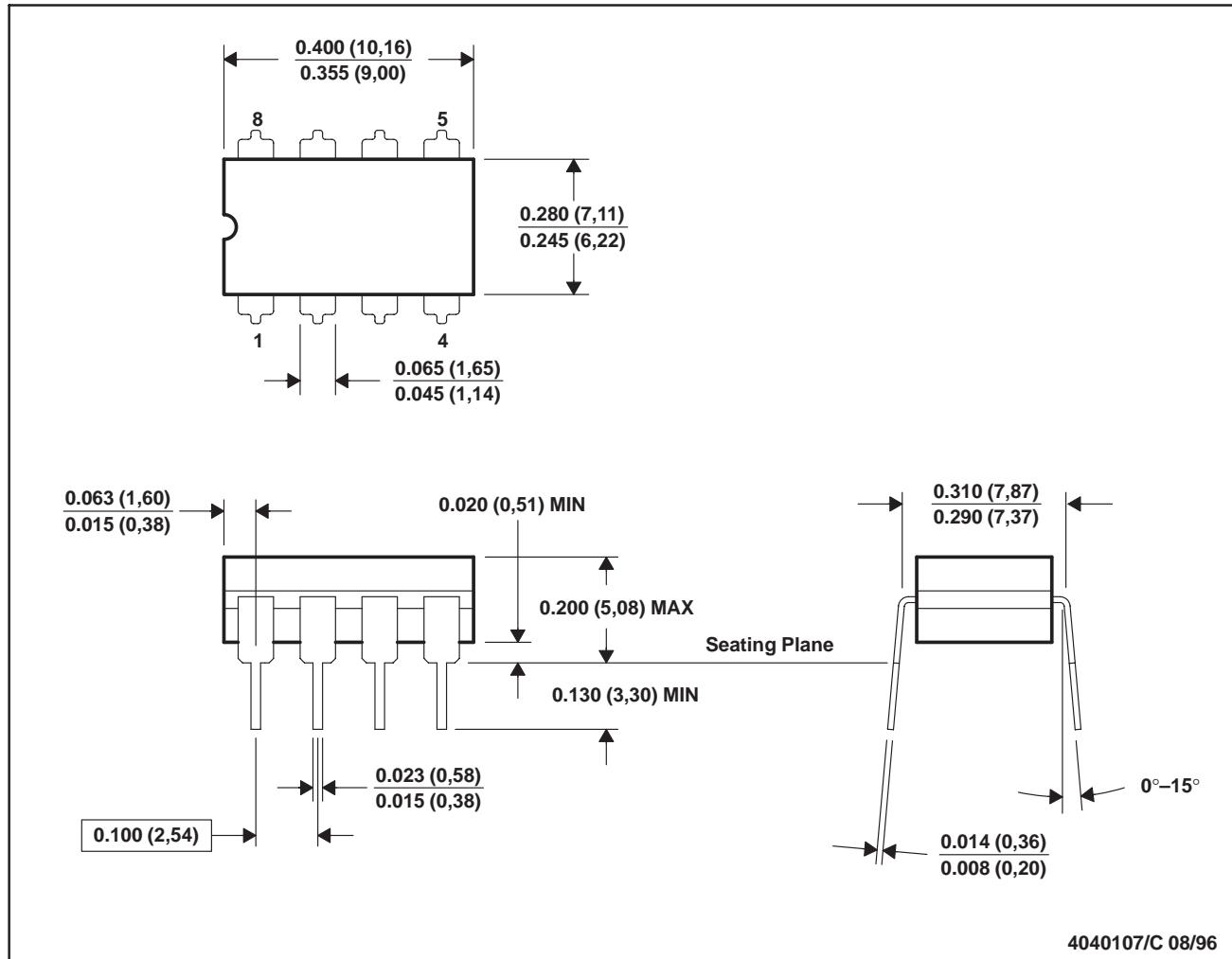
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL5001ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001AQDR	SOIC	D	8	2500	367.0	367.0	38.0
TL5001AQDRG4	SOIC	D	8	2500	367.0	367.0	38.0
TL5001CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL5001IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001IPSR	SO	PS	8	2000	367.0	367.0	38.0
TL5001QDR	SOIC	D	8	2500	367.0	367.0	38.0
TL5001QDRG4	SOIC	D	8	2500	367.0	367.0	38.0

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

**JG (R-GDIP-T8)**

**CERAMIC DUAL-IN-LINE**



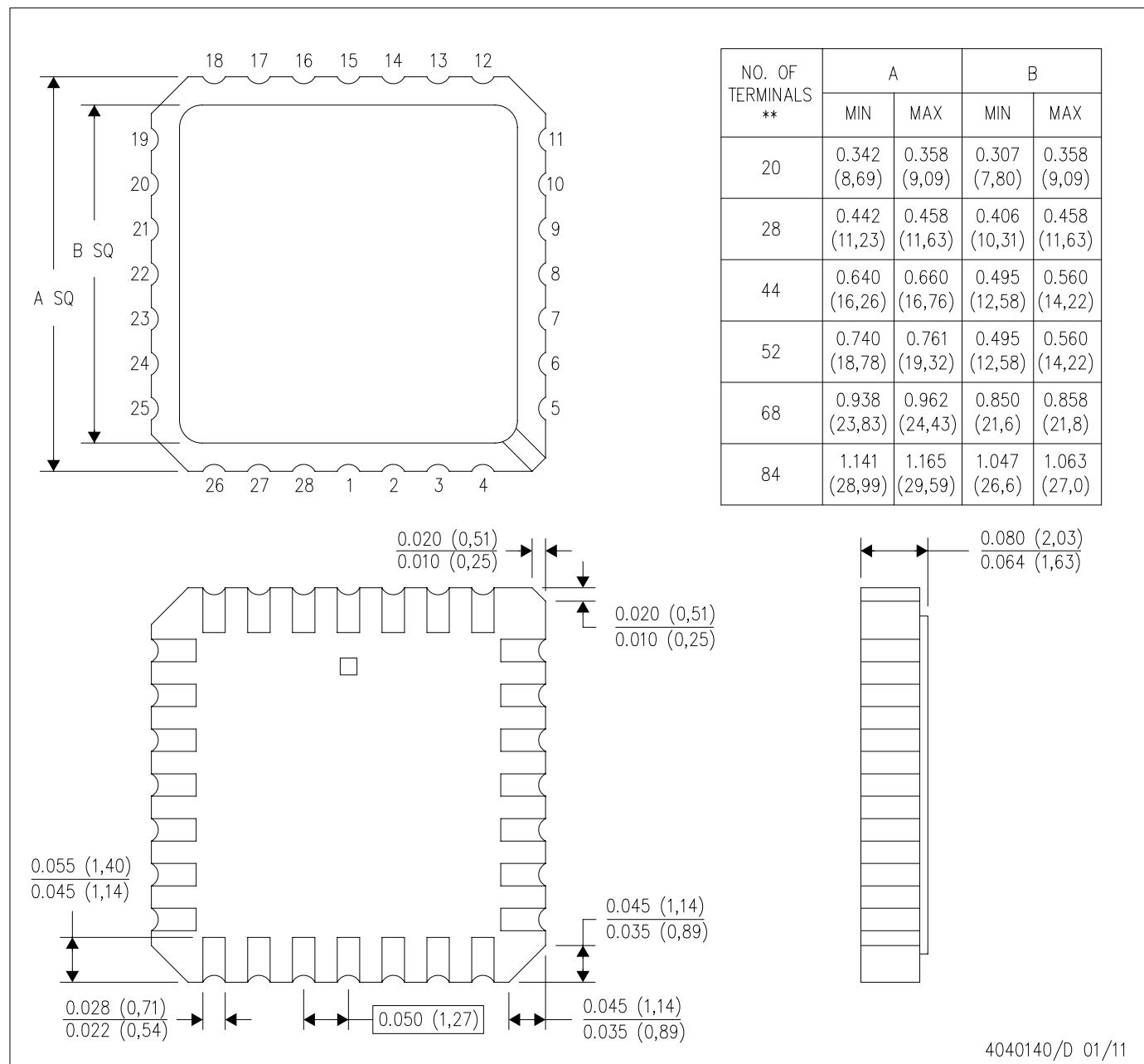
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification.
- Falls within MIL STD 1835 GDIP1-T8

**FK (S-CQCC-N\*\*)**

28 TERMINAL SHOWN

**LEADLESS CERAMIC CHIP CARRIER**



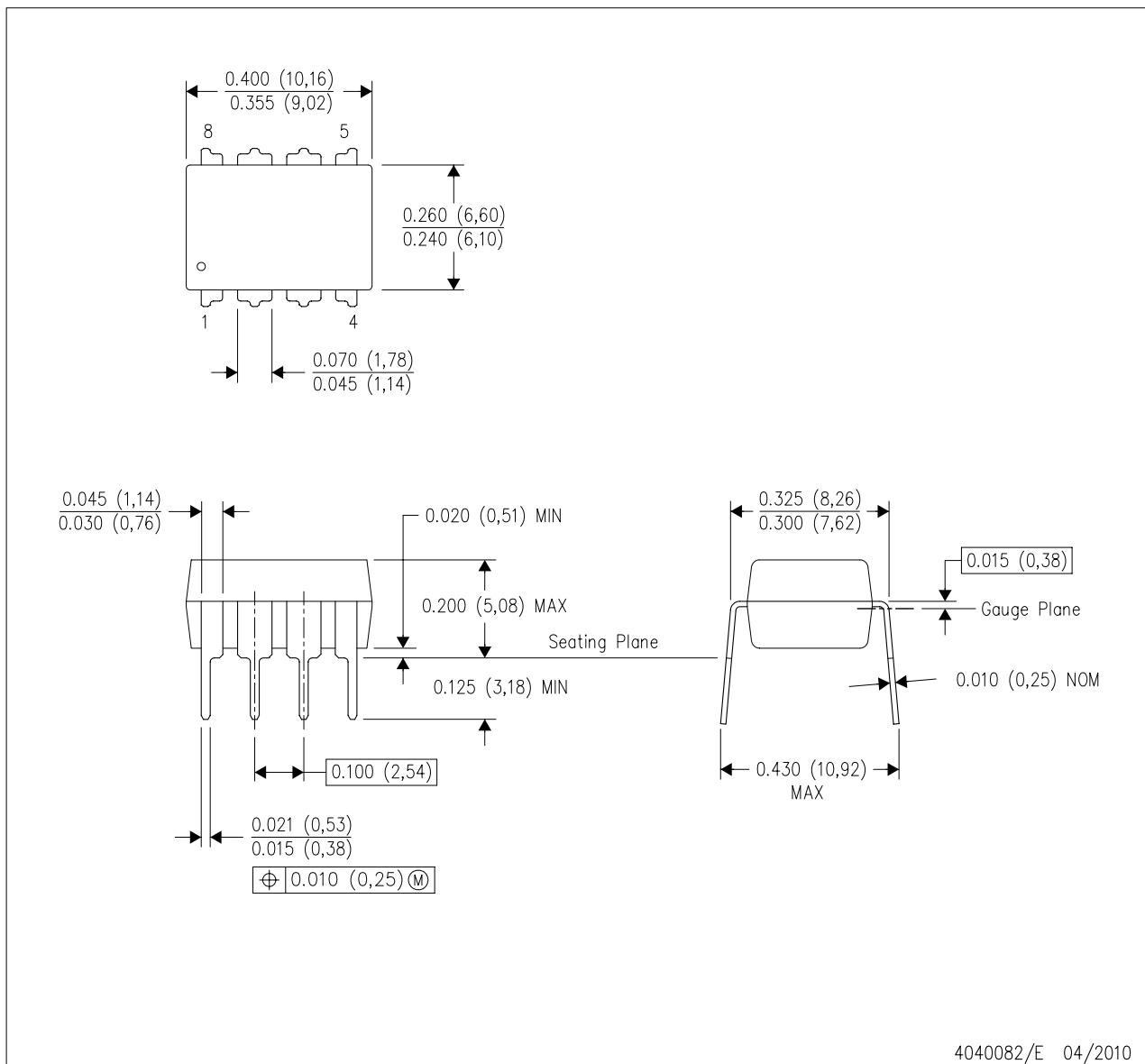
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a metal lid.  
 D. Falls within JEDEC MS-004

4040140/D 01/11

## MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

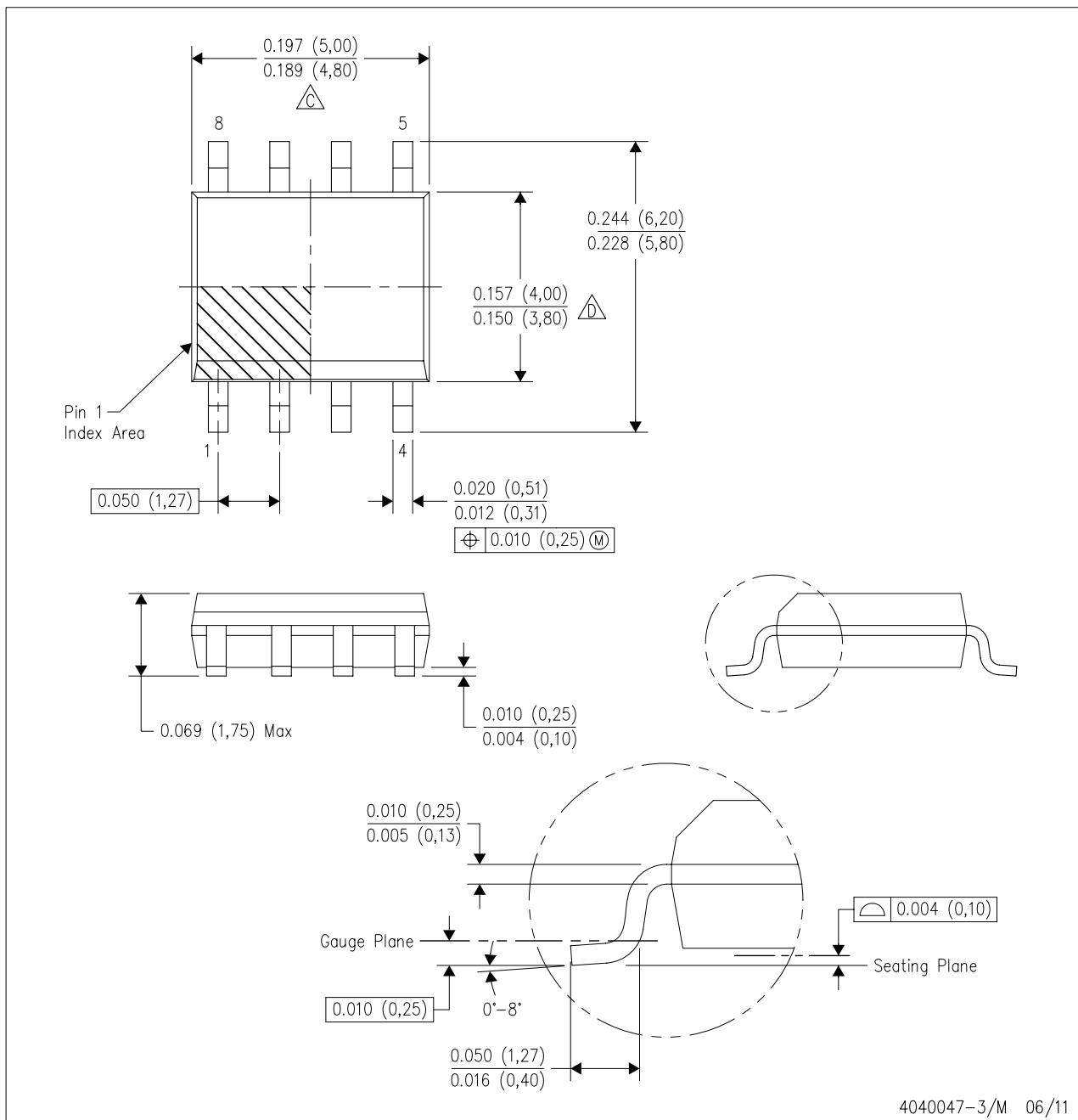
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.

## MECHANICAL DATA

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

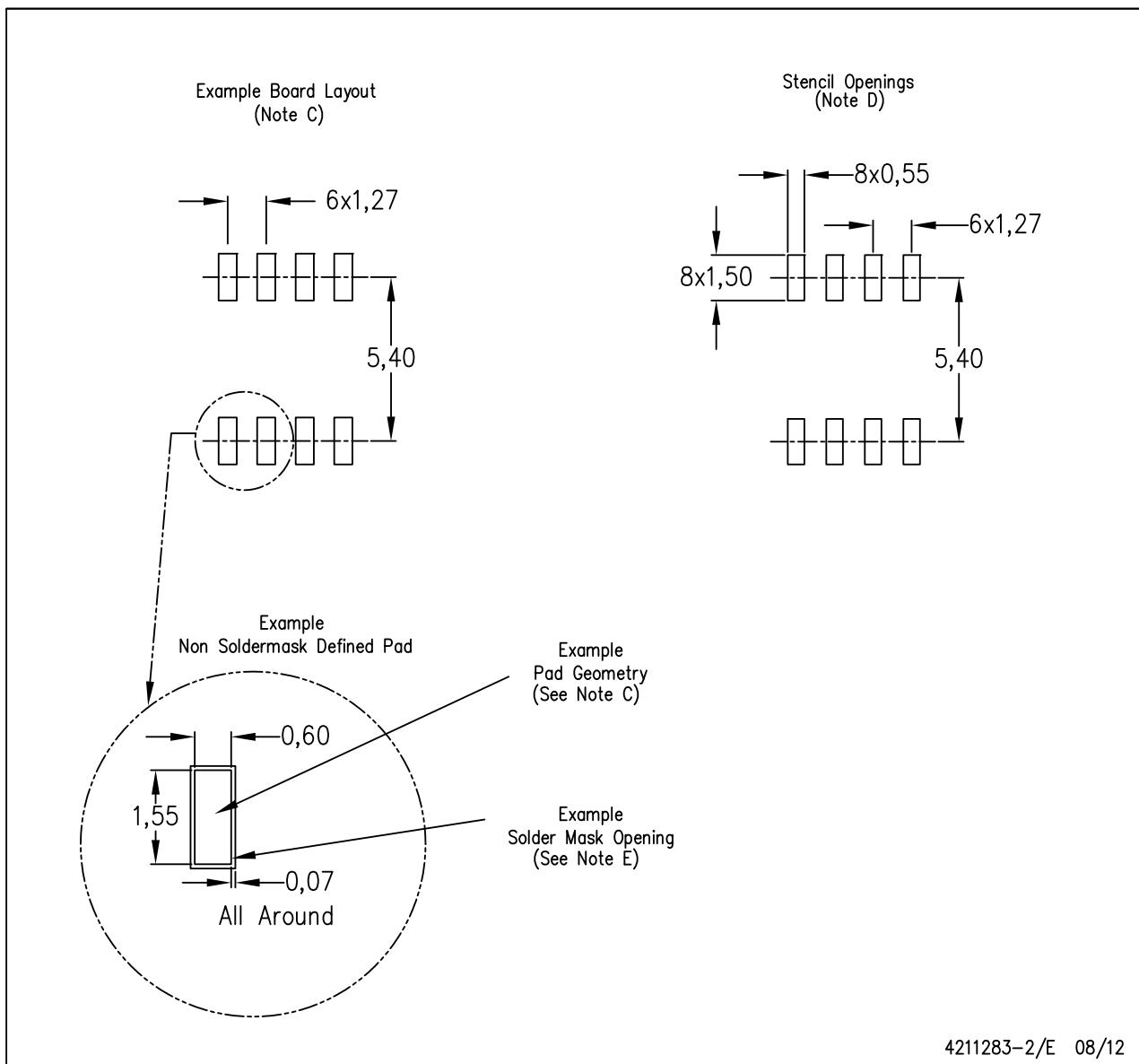
D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AA.

## LAND PATTERN DATA

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

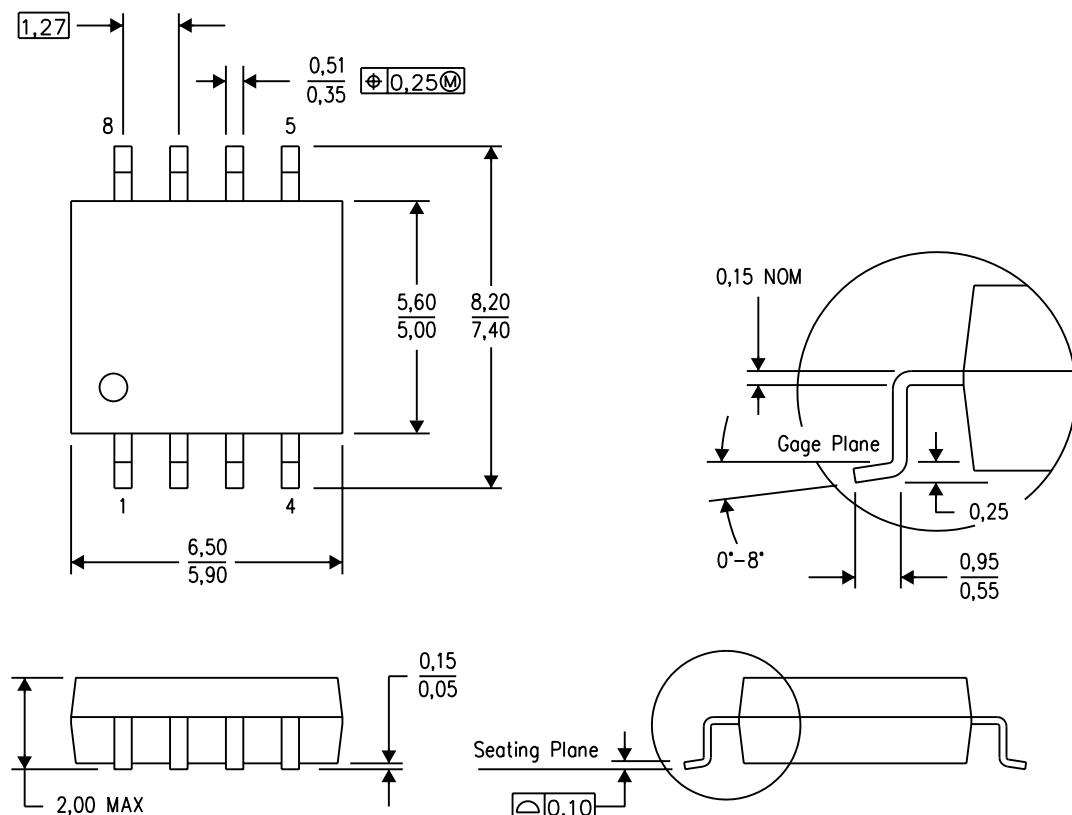
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4040063/C 03/03

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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