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DLP-2232H-PSOC5

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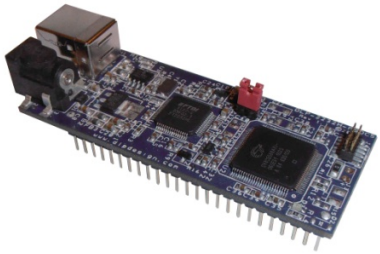
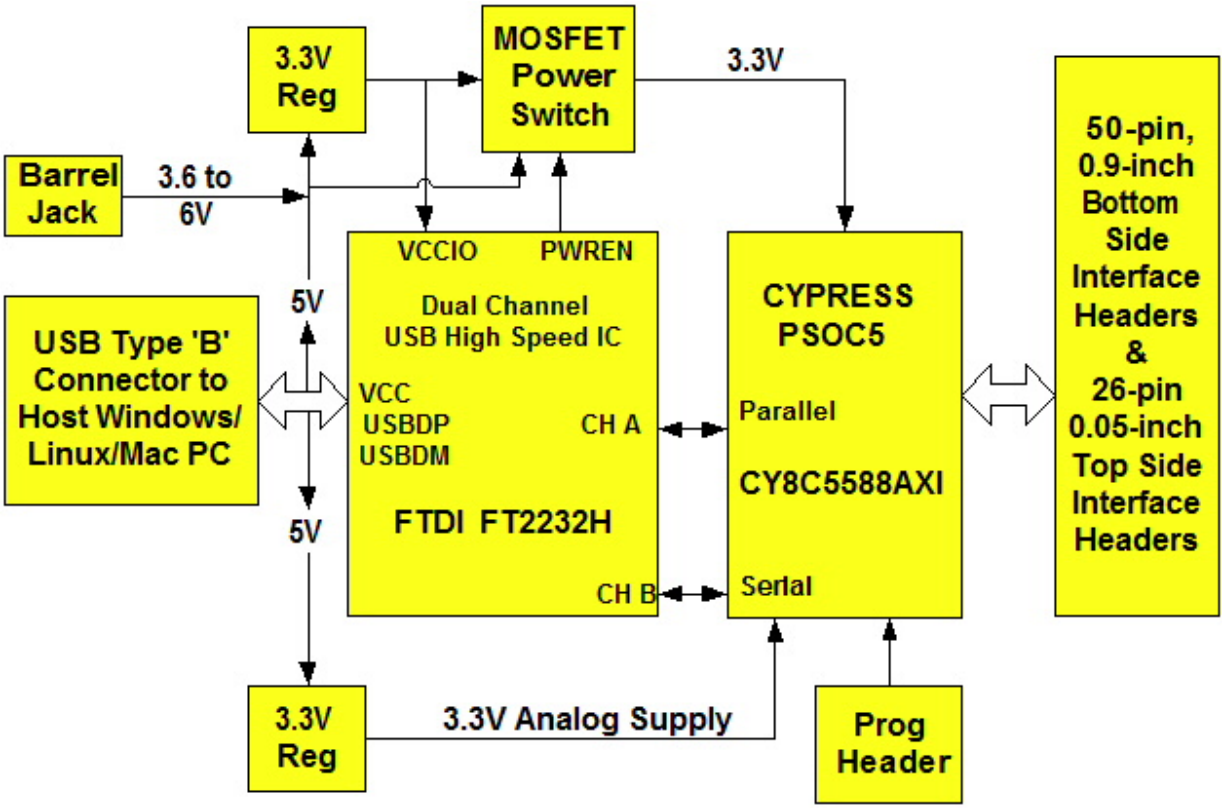


DLP-2232H-PSOC5

LEAD FREE

USB - PSOC5 MODULE



FEATURES:

- Cypress CY8C5588 Programmable System-on-Chip (PSoC®) 5 containing:
  - 32-bit ARM Cortex-M3 CPU Core
  - Up to 67MHz Operation
  - 256 KBytes Flash Program Memory
  - 64 KBytes SRAM Memory
  - Internal Non-Volatile Configuration Memory for All Programmable Features
  - One Configurable Delta-Sigma ADC with 8- to 20-Bit Resolution
  - Two Configurable SAR ADC's with 8- to 12-Bit Resolution
  - Four 8-bit DAC's Configurable for Current or Voltage Mode Operation
  - Four Comparators and Four OpAmps
  - Four Configurable Multifunction Analog Blocks
  - 24 Programmable Logic Device (PLD-Based) Universal Digital Blocks (UDB)

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  - Four Configurable Timers/Counters/PWM Blocks
  - Library of Standard Peripherals including SPI, UART and I2C
- High-Speed USB 2.0 Interface Featuring FTDI FT2232H Silicon—Both Parallel and Serial Interfaces are Supported
- 40 User I/O Channels plus 2 Output/Dedicated Peripheral Usage Pins
  - Any User I/O Can Route to Either Digital or Analog Peripheral
  - All User I/O are Configurable as Open Drain High/Low, Pull-Up/Pull-Down, High-Z or Strong Output
  - Any User I/O Can Support CapSense® Technology
  - Any User I/O Can Support LCD Direct Drive
  - All User I/O Can Support Configurable Pin State at Power-On Reset
- USB Port Powered or 5V External Power Barrel Jack
- USB 1.1- and 2.0-Compatible Interface
- Small Footprint: 3.0 x 1.2-Inch PCB and Standard 50-Pin, 0.9-Inch DIP Interface

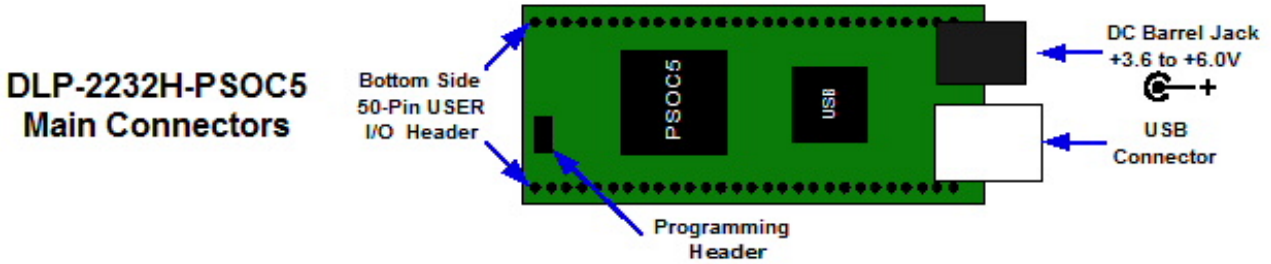
APPLICATIONS:

- Rapid Prototyping
- Educational Tool
- Industrial/Process Control
- Data Acquisition/Processing
- Embedded Processor

1.0 INTRODUCTION

The DLP-2232H-PSOC5 module is a low-cost, compact prototyping tool that can be used for rapid proof of concept, OEM solutions or within educational environments. The module is based on Cypress Semiconductor's Programmable System-on-Chip (PSoC®) 5 and Future Technology Devices International's FT2232H Dual-Channel High-Speed USB IC. The DLP-2232H-PSOC5 provides both the beginner as well as the experienced engineer with a rapid path to developing PSoC-based designs. When combined with the free PSoC® software development tools (PSoC Creator™ and PSoC Programmer™) from Cypress, this module is more than sufficient for creating anything from basic microcontroller with embedded analog and digital functions to a highly complex system controller. Both the hardware system architecture and the software are supported by the PSoC® software tools.

The DLP-2232H-PSOC5 has on-board voltage regulators that generate all required power supply voltages from a single 5-volt source. Power for the module can be taken from either the host USB port or from a user-supplied, external 5-volt power supply via an onboard standard barrel connector:



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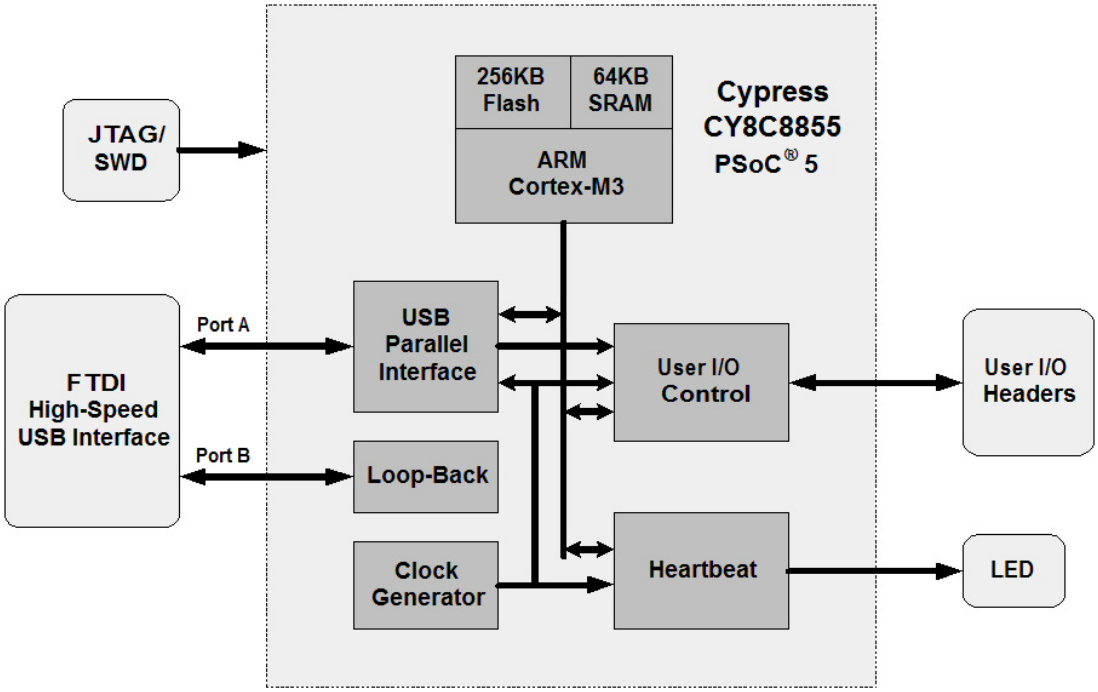
Connection to user electronics is made via a 50-pin, 0.9-inch wide, industry-standard 0.025-square inch post DIP header on the bottom of the board. The bottom side 50-pin header provides access to the user input/output pins as well as the USB port power output and the module's power input. The bottom side header mates with a user-supplied, standard, 50-pin, 0.9-inch spaced DIP socket.

Other on-board features include a GPIO-driven LED, SMT footprints for optional external KHz and MHz crystals and a JTAG/SWD port for connection to Cypress programming and debug tools.

2.0 REFERENCE DESIGN

A reference design comes pre-loaded in the Cypress PSoC® 5 on the DLP-2232H-PSOC5, and this is available for download to those who purchase the module. The design was created and compiled using the free Cypress PSoC Creator™ tools. The reference design consists of the following blocks:



It contains the ARM Cortex M-3 CPU along with its internal memory, a USB Interface Block, a User I/0 Block, a Heartbeat Pulse Generator and a Clock Generator. The JTAG Port is used to program and debug the PSoC® 5. The ARM core source code is written in C, and uses the compiler included with the PSoC Creator™ tool. The hardware implemented in the PLD blocks was created using the Cypress Component Catalog and compiled using the synthesis tool also included in the PSoC Creator™ tool.

The USB interface captures, interprets and returns command and data information sent from the host PC through the FTDI USB interface to the PSoC® 5. Commands include Ping, Flash LED, Set a User I/O Pin High or Low or Read a User I/O Pin (Section 10 explains these in detail).

The User I/O Block controls access to the 40 user I/O pins accessible through the bottom-side headers. The User I/O Block can configure these pins as inputs and read their state or as outputs and drive them high or low.

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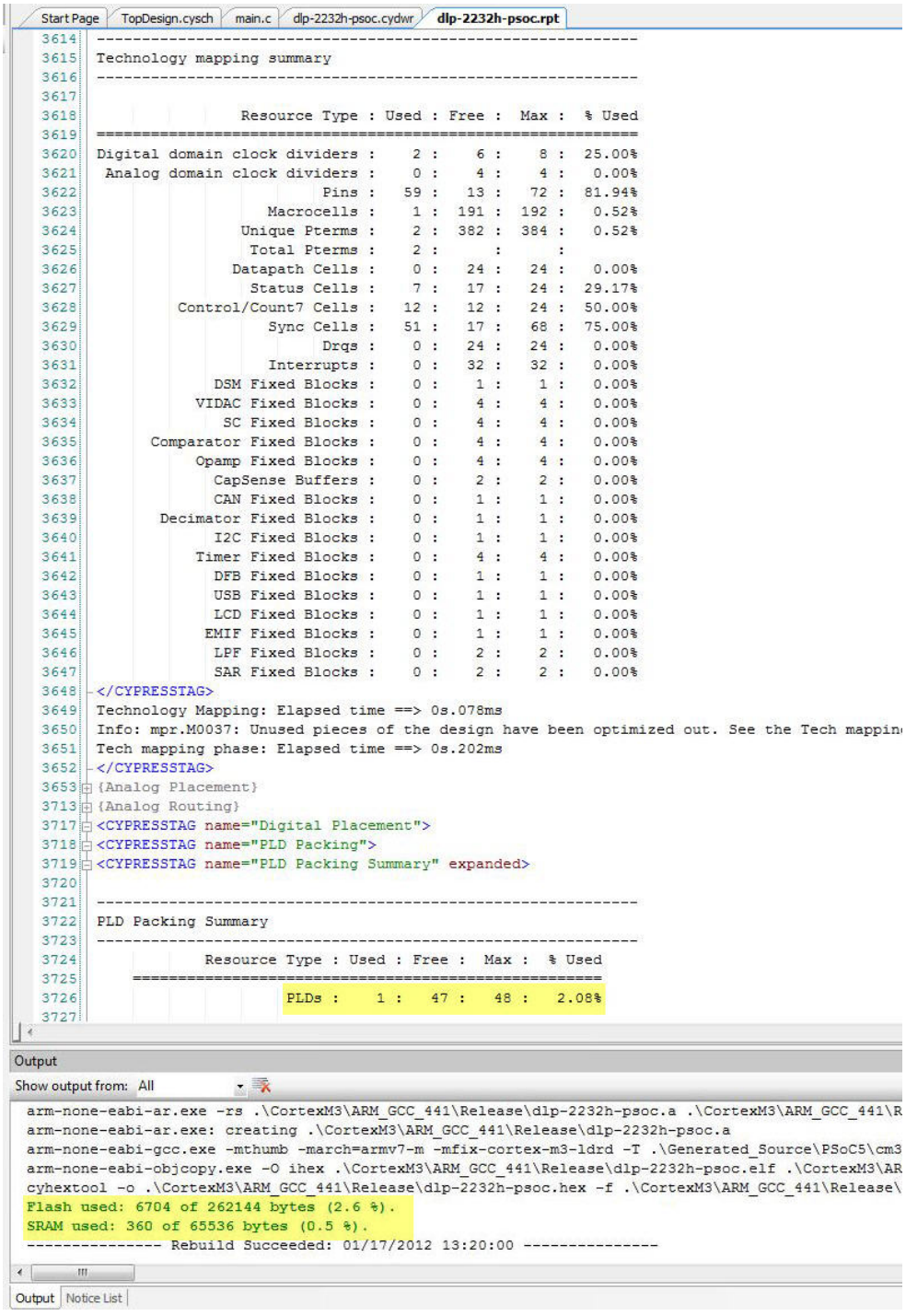
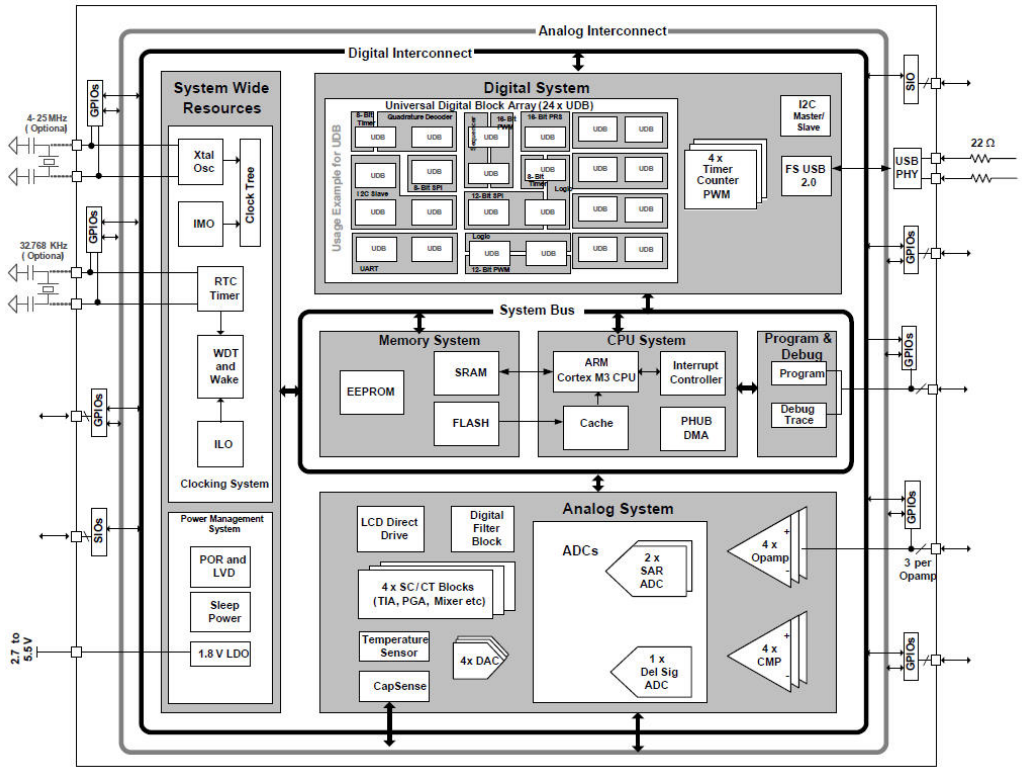
The Clock Generator Block creates the ARM CPU core clock and the 10-Hz clock for the Heartbeat Pulse Generator. The Heartbeat Pulse Generator gates the 10-Hz clock to flash the LED based on the status of the control bits from the ARM CPU.

The design occupies the following resources on the DLP-2232H-PSOC5 module's CY8C5588: Approximately 3% of the flash program memory, <1% of the SRAM data memory and 2% of logic resources.



More reference designs are planned. Please contact DLP Design with any specific requests.

3.0 PSoC® 5 SPECIFICATIONS



The device used on the DLP-2232H-PSOC5 is the Cypress PSoC® 5 CY8C5588AXI-060. It contains the following:

- Processor System:

CPU Core:	32-Bit ARM Cortex-M3
CPU Speed:	67MHz, 1.25 DMIPS/MHz, 80+ DMIP's Performance
Architecture:	Harvard, 3-Stage Pipeline
Instruction Set:	Thumb®-2 (includes 16-Bit and 32-Bit Instructions)
Memory:	256-KB Flash, 64 Kbytes SRAM, 2-KB EEPROM (4 GB Address Space)
Cache:	128 Byte with Internal Controller
Interrupts:	Nested Vectored Interrupt Controller Supports 16 System Exceptions and 32 Peripheral Interrupts (48 total)
DMA:	24 Channels with 8 Levels of Priority; up to 127 Transaction Descriptors
Clocking:	3- to 48-MHz Internal Main Oscillator; PLL Output of 24-67 MHz

- Analog System:

A/D Convertors:	One 8- to 20-bit Delta-Sigma ADC; Two 8- to 12-bit SAR ADC's
D/A Convertors:	Four 8-bit DAC's Configurable for Voltage or Current
Reference:	Internal Precision Reference Included
Comparators:	Four Factory Trimmed to 15 mV with Two Optional Low-Pass Filters
OpAmps:	Four Configurable as Gain Stage or Voltage Follower
Other:	Four Configurable Switched Capacitance/Continuous Time Blocks for use as OpAmps, Unity Gain Buffer, PGA, TIA, Mixer, etc. CapSense, Digital Filter Block andTemperature Sensor.

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- Digital System:

Universal Digital Blocks:	24 UDB's; Each Consisting of 2 Programmable Logic Devices (PLD), 1 Datapath ALU, Status Register and Control Register
PLD:	12V4 PAL Equivalent (12 Input AND Array, OR'd into 4 Opt. Registers)
Datapath ALU:	8-Bit Wide; Configurable as 2 Accumulators, 2 Data Registers, 2 4-Entry FIFOs, an 8-Function ALU, a 4-Function Shift and Masking Function
UDB Configurations:	UARTs, I^2C, SPI, CAN, Timer, Counter, PWM, Logic Gates, LCD Drive Custom User Logic Blocks
Other:	Four Fixed Function 8- or 16-Bit Timer/Counter/PWM Blocks

4.0 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed here may cause permanent damage to the DLP-2232H-PSOC5:

Operating Temperature: 0-70°C

Voltage on Digital Inputs with Respect to Ground: -0.5V to +3.8V

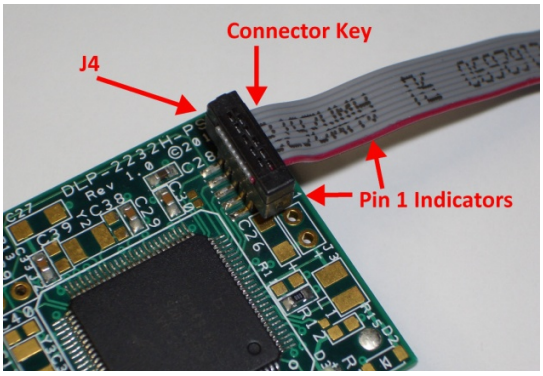
Sink/Source Current on Any I/O: 24 mA / 18 mA (configured for strong drive)

5.0 WARNINGS

- Unplug from the host PC and power adapter before connecting to I/O on the DLP-2232H-PSOC5.
- Isolate the bottom of the board from all conductive surfaces.
- Observe static precautions to prevent damage to the DLP-2232H-PSOC5 module.

6.0 PSoC® 5 Programming

All of the PSoC® 5 device's internal memory can be programmed using the free Cypress PSoC® Programmer Software and a Cypress PSoC® MiniProg 3 Programming Cable (purchased separately) available from Cypress or its distributers. The MiniProg cable connects to the J4 programming port on the DLP-2232H-PSOC5 module. Observe the cable orientation carefully. The connector key pin marking is on the silkscreen at the top edge of the PCB, opposite from the USB connector. The cable orientation is as shown below:



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7.0 EEPROM SETUP / MPROG

The DLP-2232H-PSOC5 has a dual-channel USB interface to the host PC. Channel A of the high-speed USB interface is connected to the PSoC® 5 in FIFO parallel mode to allow for the fastest possible transfers between the USB host and the PSoC® 5. Channel B of the high-speed USB interface is connected to the PSoC® 5 in serial mode to allow for UART communication between the host PC and the PSoC® 5. A 93LC46B EEPROM connected to the USB interface IC is used to store the setup for the two channels. The parameters stored in the EEPROM include the Vendor ID (VID), Product ID (PID), Serial Number, Description String, driver selection (VCP or D2XX) and port type (UART serial or FIFO parallel).

To support the configuration described above, Channel A of the USB device must be configured in 245 FIFO mode, and Channel B of the USB device must be configured in RS232 UART mode. Either VCP or D2XX drivers can be used. By default, the USB device EEPROM configuration is set for D2XX drivers on both channels with 245 FIFO on Channel A and RS232 UART on Channel B. The D2XX drivers provide faster throughput but require working with a *.lib or *.dll library in the host application. The VCP drivers make the DLP-2232H-PSOC5 appear as two RS232 ports to the host application.

The operational modes and other EEPROM selections are written to the EEPROM using the MPROG utility. This utility and its manual are available for download from the bottom of the page at **www.dlpdesign.com**.

8.0 TEST HEX FILE

A test hex file derived from the reference design described earlier is provided as a download from the DLP Design website to customers who purchase the module. This design provides rudimentary access to the I/O features of the DLP-2232H-PSOC5. The DLP-2232H-PSOC5 module comes preprogrammed with this file. The following features are provided:

- Ping
- Read the High/Low State of the I/O Pins
- Drive the I/O Pins High/Low or Read their High/Low State

This hex file is available from the DLP-2232H-PSOC5's download page. (The command structure that supports these features is explained in Section 10.)

9.0 USB DRIVERS

USB drivers for the following operating systems are available for download from the DLP Design website at **www.dlpdesign.com**:

OPERATING SYSTEM SUPPORT	
Windows 7 32-Bit	**Windows 7 64-Bit**
Windows Vista, Vista x64	**Mac OSX**
Windows XP, XP x64	**Mac OS9**
Windows Server 2008, x64	**Mac OS8**
Windows Server 2003, x64	**Linux**
Windows 2000	**Windows CE 4.2-6.0**

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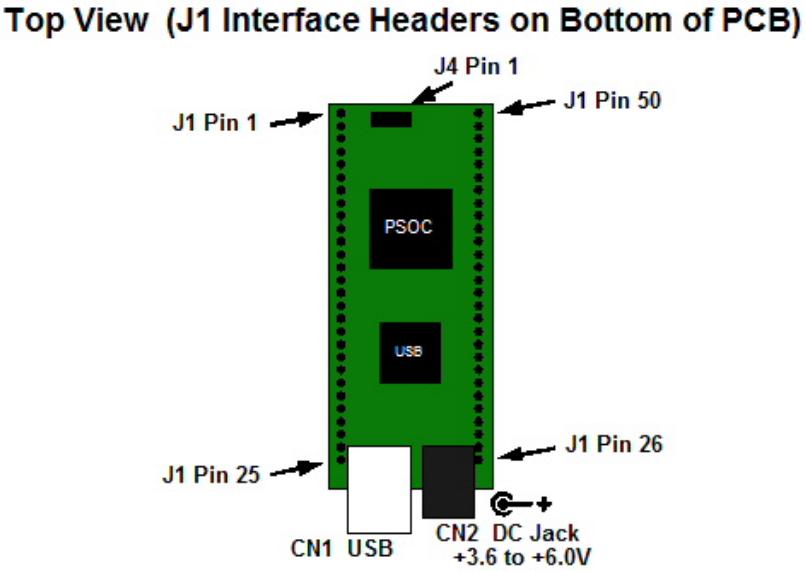
Note:

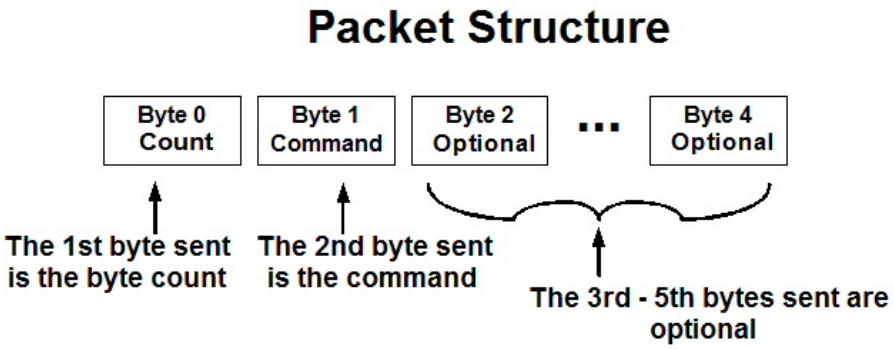
If you are utilizing the dual-mode drivers from FTDI (CDM2.X.X), and you want to use the Virtual COM Port (VCP) drivers instead, then it may be necessary to disable the D2XX drivers first via Device Manager. To do so, right click on the entry under USB Controllers that appears when the DLP-2232H-PSOC5 is connected, select Properties, select the Advanced tab, check the option for "Load VCP" and click OK. Then unplug and replug the DLP-2232H-PSOC5, and a COM port should appear in Device Manager under Ports (COM & LPT).

10.0 USING THE DLP-2232H-PSOC5

Select a power source via Header Pins 24 and 25, and connect the DLP-2232H-PSOC5 to the PC to initiate the loading of the USB drivers. The easiest way to do this is to connect Pins 24 and 25 to each other using a 0.1-inch shunt. This will result in operational power being taken from the host PC.



Connect the DLP-2232H-PSOC5 to the PC to initiate the loading of USB drivers. Once the USB drivers are loaded, the DLP-2232H-PSOC5 is ready for use. All commands are issued as multi-byte command packets consisting of at least two bytes.



You can either utilize the Test Application available from **http://www.dlpdesign.com/test.shtml** with the DLP-2232H-PSOC5 (as described in Section 11), or you can write your own program in your language of choice.

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If you are using the VCP drivers, begin by opening the COM port, and send multi-byte commands as shown in Table 1 below. There is no need to set the baud rate because the DLP-2232H-PSOC5 uses a parallel interface between the USB IC and the PSoC® 5. (The Ping Command can be used to locate the correct COM port used for communicating with the DLP-2232H-PSOC5, or you can look in Device Manager to see which port was assigned by Windows.) If you are using the D2XX drivers as with the Test Application, no COM port selection is necessary.

TABLE 1

Command Packets

Command Packet	Description	Byte	Hex Value	Return/Comments
Ping	Issues Ping	0	0x02	Packet Byte Count
		1	0x27	Ping Command - 0x50 [1] (ASCII 'P') will be returned indicating that the DLP-2232H-PSOC5 is found on the selected port.
Flash	Flashes LED	0	0x02	Packet Byte Count
		1	0x28	Flashes LED command; lasts approximately one second. Returns echo of command sent (0x28) [1] only.
LED On/Off	Accesses the Internal Version/ Status Registers	0	0x03	Packet Byte Count
		1	0x29	Control LED Command
		2	0x00 or 0x01	LED State: 0x00 = LED Off; 0x01 = LED On Returns echo of command sent (0x29) [1] only.
Read/Write Pin	Reads the State or Writes to One of the User I/O Pins	0	0x04 or 0x05	Packet Byte Count: 4 Bytes required for Read, 5 bytes required for Write.
		1	0x30	Read/Write Pin Command
		2	0x00 – 0xF7[4]	User I/O channel/port pin numbers (these are described in Table 2).
		3	0x00 or 0x01	Selects Write or Read as follows: 0x00 = Write Pin (Specified Pin is an Output) 0x01 = Read Pin (Specified Pin is an Input) User I/O pin 0xnn is read and returns[1] the first byte as: 0x00 = User I/O Pin 0xnn is Low 0x01 = User I/O Pin 0xnn is High Read Pin returns echo of command sent (0x30) [1,2] as the second byte.
		4[5]	0x00 or 0x01	Write Value: 0x00 = User I/O Pin 0xnn is Low 0x01 = User I/O Pin 0xnn is High Write Pin returns echo of command sent (0x30) [1,2] only.

Notes:
1. If the value 0xE0 is returned the module received an invalid command byte (not 0x27,0x28,0x29 or 0x30).
2. If the value 0xE1 is returned the module received an invalid port pin byte (refer to table 2 for valid ports).
3. If the value 0xE3 is returned the module received a read request for a write only port pin (P15.6 & P15.7).
4. Not all Hex values between 0x00 and 0xF7 are valid (refer to Table 2 for valid channel values).
5. Byte 4 is only needed when Byte 3 is set to 0 (Write).

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The USER I/O Read/Write Pin Command's I/O number mapping to the physical I/O pins on the DLP-2232H-PSOC5 board are described in the following table:

TABLE 2			
Module User I/O			
I/O Number	**DLP-2232H-PSOC5 Pin**	**CY8C5588 Pin**	**PSoC® 5 Pin Configurations Available**
0x00 (P0.0)	J1 Pin 33	71	Port 0.0: GPIO (Digital I/O, Analog I/O), OpAmp 2 Out
0x01 (P0.1)	J1 Pin 36	72	Port 0.1: GPIO (Digital I/O, Analog I/O), OpAmp 0 Out
0x02 (P0.2)	J1 Pin 35	73	Port 0.2: GPIO (Digital I/O, Analog I/O), OpAmp 0+, SAR 1 REF
0x03 (P0.3)	J1 Pin 34	74	Port 0.3: GPIO (Digital I/O, Analog I/O), OpAmp 0-, REF 0
0x04 (P0.4)	J1 Pin 31	76	Port 0.4: GPIO (Digital I/O, Analog I/O), OpAmp 2+, SAR 0 REF
0x05 (P0.5)	J1 Pin 29	77	Port 0.5: GPIO (Digital I/O, Analog I/O), OpAmp 2-
0x06 (P0.6)	J1 Pin 30	78	Port 0.6: GPIO (Digital I/O, Analog I/O), IDAC 0
0x07 (P0.7)	J1 Pin 32	79	Port 0.7: GPIO (Digital I/O, Analog I/O), IDAC 2
0x20 (P2.0)	J1 Pin 45	95	Port 2.0: GPIO (Digital I/O, Analog I/O)
0x21 (P2.1)	J1 Pin 43	96	Port 2.1: GPIO (Digital I/O, Analog I/O)
0x22 (P2.2)	J1 Pin 38	97	Port 2.2: GPIO (Digital I/O, Analog I/O)
0x23 (P2.3)	J1 Pin 41	98	Port 2.3: GPIO (Digital I/O, Analog I/O)
0x24 (P2.4)	J1 Pin 42	99	Port 2.4: GPIO (Digital I/O, Analog I/O)
0x25 (P2.5)	J1 Pin 44	1	Port 2.5: GPIO (Digital I/O, Analog I/O)
0x26 (P2.6)	J1 Pin 39	2	Port 2.6: GPIO (Digital I/O, Analog I/O)
0x27 (P2.7)	J1 Pin 40	3	Port 2.7: GPIO (Digital I/O, Analog I/O)
0x30 (P3.0)	J1 Pin 14	44	Port 3.0: GPIO (Digital I/O, Analog I/O), IDAC 1
0x31 (P3.1)	J1 Pin 12	45	Port 3.1: GPIO (Digital I/O, Analog I/O), IDAC 3
0x32 (P3.2)	J1 Pin 16	46	Port 3.2: GPIO (Digital I/O, Analog I/O), OpAmp 3-, REF 1
0x33 (P3.3)	J1 Pin 13	47	Port 3.3: GPIO (Digital I/O, Analog I/O), OpAmp 3+
0x34 (P3.4)	J1 Pin 19	48	Port 3.4: GPIO (Digital I/O, Analog I/O), OpAmp 1-
0x35 (P3.5)	J1 Pin 15	49	Port 3.5: GPIO (Digital I/O, Analog I/O), OpAmp 1+
0x36 (P3.6)	J1 Pin 17	51	Port 3.6: GPIO (Digital I/O, Analog I/O), OpAmp 1 Out
0x37 (P3.7)	J1 Pin 18	52	Port 3.7: GPIO (Digital I/O, Analog I/O), OpAmp 3 Out
0x40 (P4.0)	J1 Pin 11	69	Port 4.0: GPIO (Digital I/O, Analog I/O),
0x41 (P4.1)	J1 Pin 10	70	Port 4.1: GPIO (Digital I/O, Analog I/O)
0x42 (P4.2)	J1 Pin 9	80	Port 4.2: GPIO (Digital I/O, Analog I/O)
0x43 (P4.3)	J1 Pin 8	81	Port 4.3: GPIO (Digital I/O, Analog I/O)
0x44 (P4.4)	J1 Pin 7	82	Port 4.4: GPIO (Digital I/O, Analog I/O)
0x45 (P4.5)	J1 Pin 6	83	Port 4.5: GPIO (Digital I/O, Analog I/O)
0x46 (P4.6)	J1 Pin 5	84	Port 4.6: GPIO (Digital I/O, Analog I/O)
0x47 (P4.7)	J1 Pin 4	85	Port 4.7: GPIO (Digital I/O, Analog I/O)
0xC0 (P12.0)	J1 Pin 21	53	Port 12.0: SIO (Digital I/O, Analog I/O), I^2C 1: SDA
0xC1 (P12.1)	J1 Pin 22	54	Port 12.1: SIO (Digital I/O, Analog I/O), I^2C 1: SCL
0xC2 (P12.2)	J1 Pin 27	67	Port 12.2: SIO (Digital I/O, Analog I/O)
0xC3 (P12.3)	J1 Pin 26	68	Port 12.3: SIO (Digital I/O, Analog I/O)
0xC4 (P12.4)	J1 Pin 47	4	Port 12.4: SIO (Digital I/O, Analog I/O), I^2C 0: SCL
0xC5 (P12.5)	J1 Pin 48	5	Port 12.5: SIO (Digital I/O, Analog I/O), I^2C 0: SDA
0xC6 (P12.6)	J1 Pin 50	29	Port 12.6: SIO (Digital I/O, Analog I/O)
0xC7 (P12.7)	J1 Pin 49	30	Port 12.7: SIO (Digital I/O, Analog I/O)

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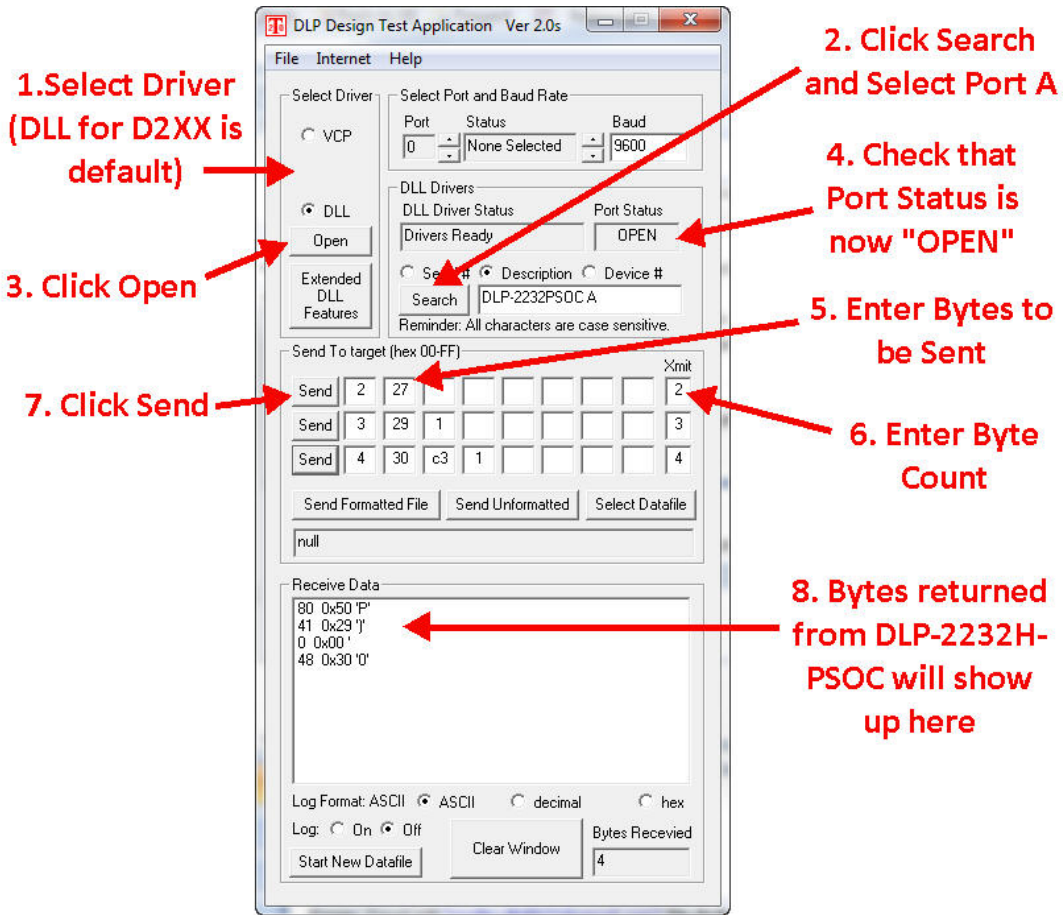
0xF6 (P15.6)	J1 Pin 2	35	Port 15.6: USBIO, D+, SWDIO (See Note 1)
0xF7 (P15.7)	J1 Pin 1	36	Port 15.7: USBIO, D-, SWDCK (See Note 1)

Note 1: Not implemented on the DLP-2232H-PSOC5 module. Can be implemented by adding a crystal.

TABLE 3		
Module Power		
I/O Number	**DLP-2232H-PSOC5 Pin**	**Description**
+5V IN	J1 Pin 24	+5V Input to the DLP-2232H-PSOC5
+5V USB	J1 Pin 25	+5V Supplied by Host PC USB Port
GND	J1 Pin 3, 20, 23, 28, 37 and 46	Ground

11.0 USING THE DLP TEST APPLICATION (OPTIONAL)

Users can either design their own application interface to send USB commands to the DLP-2232H-PSOC5 module or utilize the test application tool available from DLP Design. The Test Application is available in a free version for download from the DLP Design website at **www.dlpdesign.com/test.shtml**. Using this tool, single- and multi-byte commands can be sent to the DLP-2232H-PSOC5 board. Once installed the test application is used as follows:



The commands used to interface to the DLP-2232H-PSOC5 are detailed in Section 10 of this datasheet.

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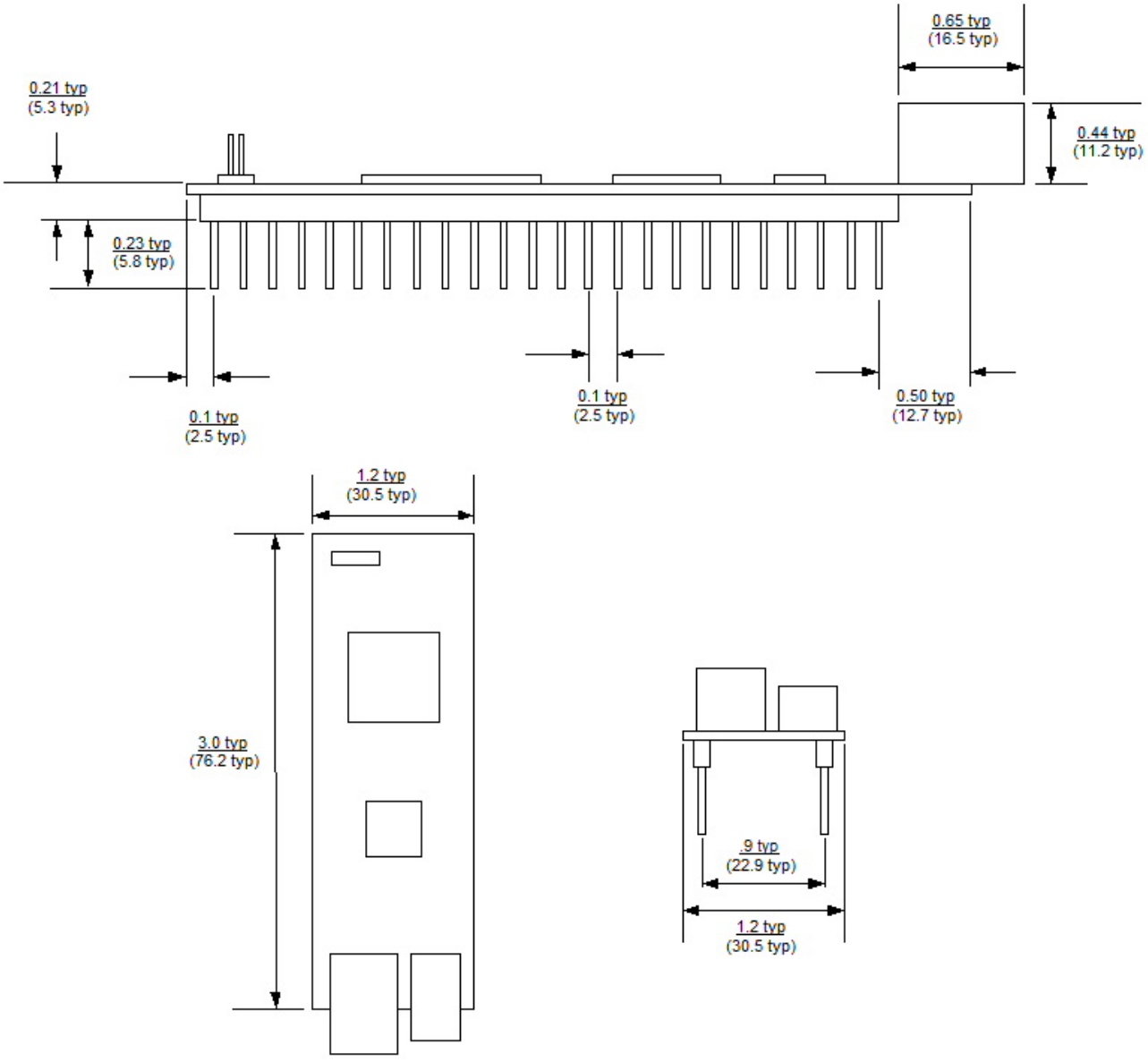
12.0 MECHANICAL DIMENSIONS IN INCHES (MM) (PRELIMINARY)



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14.0 CONTACT INFORMATION

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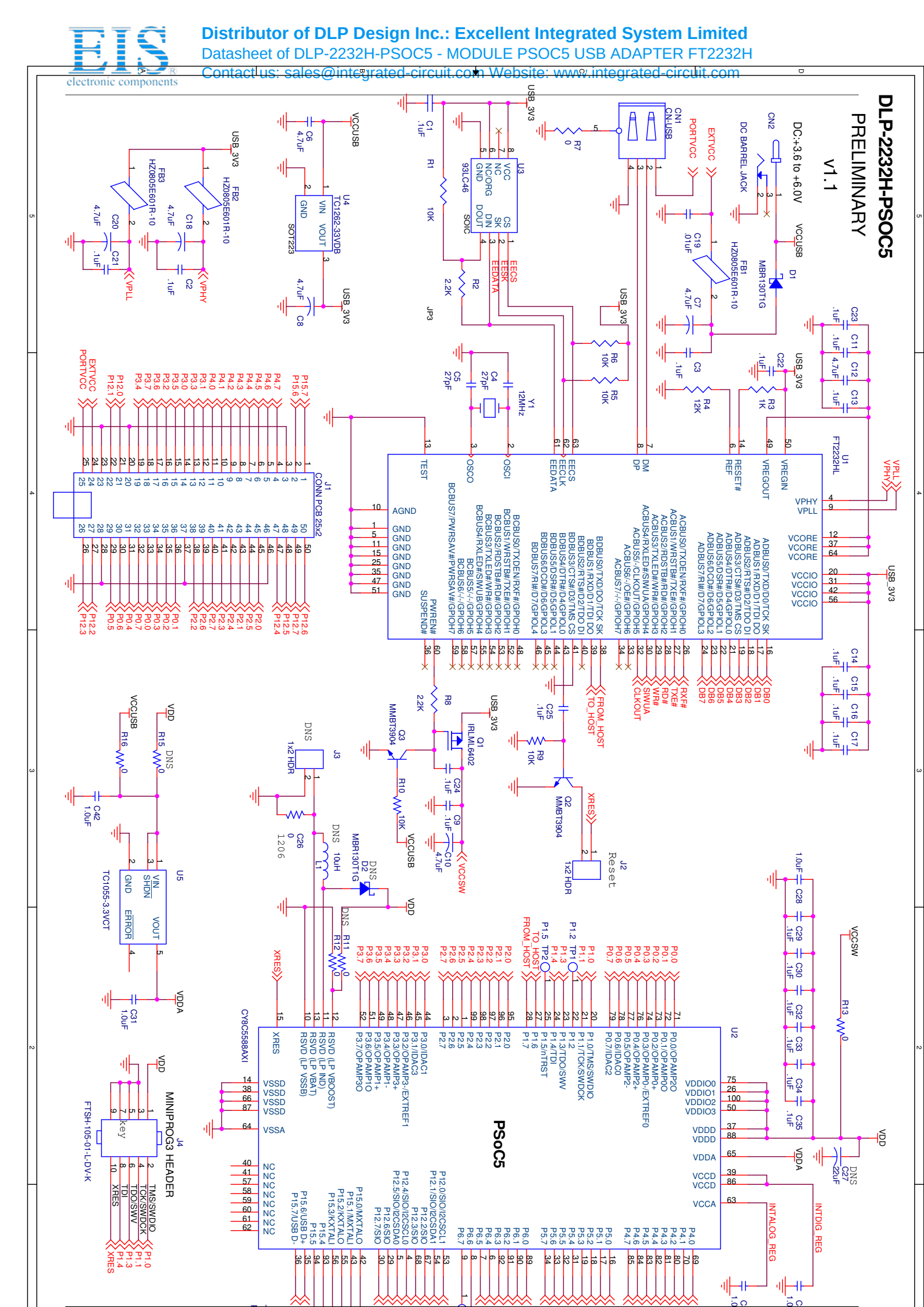
DLP-2232H-PSOC5
PRELIMINARY
v1.1
DC:+3.6 to +6.0
DC BARREL JACK
MBR130T1G
FB1 HZ0805E601R-10
FB2 HZ0805E601R-10
FB3 HZ0805E601R-10
TC1262-33VDB
93LC46
12MHz
FT232HL
TEST
OSCO
OSCI
EECS
EECLK
EEDATA
DM
DP
RESET#
VREGOUT
VREGIN
VPHY
VPLL
VCORE
VCCIO
PWREN#
SUSPEND#
CONN PCB 25x2
TC1055-3.3VCT
MMBT3904
IRLML6402
1x2 HDR
Reset
MINIPROG3 HEADER
TMS/SWDIO
TCK/SWDCK
TDO/SWV
TDI
XRES
CY8C5568AXI
PSoC5
XRES
VSSD
VSSA
VDDIO0
VDDIO1
VDDIO2
VDDIO3
VDDD
VDDA
VCCD
VCCA
INTALOG_REG
INTDIG_REG