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[Alpha & Omega Semiconductor Inc.](#)
[AO5401E](#)

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AO5401E

P-Channel Enhancement Mode Field Effect Transistor

General Description

The AO5401E/L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. AO5401E and AO5401EL are electrically identical.

-RoHS compliant

-AO5401EL is Halogen Free

Features

V_{DS} (V) = -20V

I_D = -0.5 A (V_{GS} = -4.5V)

$R_{DS(ON)} < 0.8\Omega$ (V_{GS} = -4.5V)

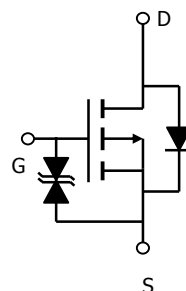
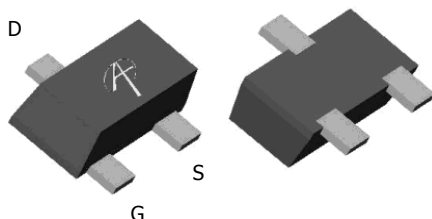
$R_{DS(ON)} < 1\Omega$ (V_{GS} = -2.5V)

$R_{DS(ON)} < 1.3\Omega$ (V_{GS} = -1.8V)

ESD PROTECTED!

SC89-3L

Top View



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	10 Sec	Steady State	Units
Drain-Source Voltage	V_{DS}	-20		V
Gate-Source Voltage	V_{GS}	± 8		V
Continuous Drain Current ^{AF}	I_D	$T_A=25^\circ\text{C}$	-0.5	A
		$T_A=70^\circ\text{C}$	-0.45	
Pulsed Drain Current ^B	I_{DM}	-1		
Power Dissipation ^A	P_D	$T_A=25^\circ\text{C}$	0.38	W
		$T_A=70^\circ\text{C}$	0.24	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	275	330	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	360	450	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	300	350	$^\circ\text{C/W}$

AO5401E
Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =10V, V _{GS} =±4.5V			±1	μA
		V _{DS} =10V, V _{GS} =±8V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-0.4	-0.5	-0.9	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-1			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-0.5A T _J =125°C		0.53 0.75	0.8 0.95	Ω
		V _{GS} =-2.5V, I _D =-0.5A		0.72	1	Ω
		V _{GS} =-1.8V, I _D =-0.3A		0.95	1.3	Ω
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-0.5A		0.9		S
V _{SD}	Diode Forward Voltage	I _S =-0.1A, V _{GS} =0V		-0.66	-1	V
I _S	Maximum Body-Diode Continuous Current				-0.5	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =-10V, f=1MHz		72	100	pF
C _{OSS}	Output Capacitance			17		pF
C _{rss}	Reverse Transfer Capacitance			9		pF
SWITCHING PARAMETERS						
t _{D(on)}	Turn-On DelayTime	V _{GS} =-4.5V, V _{DS} =-10V, R _L =50Ω, R _{GEN} =3Ω		60.5		ns
t _r	Turn-On Rise Time			150		ns
t _{D(off)}	Turn-Off DelayTime			612		ns
t _f	Turn-Off Fall Time			436		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-0.5A, dI/dt=100A/μs		27	35	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-0.5A, dI/dt=100A/μs		8.3		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t_{ON} ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using <300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

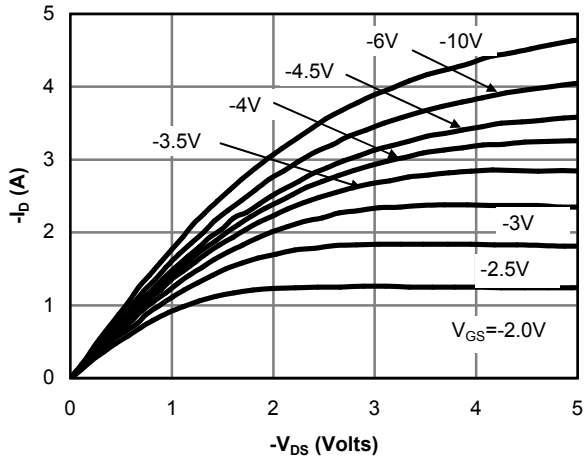


Figure 1: On-Region Characteristics

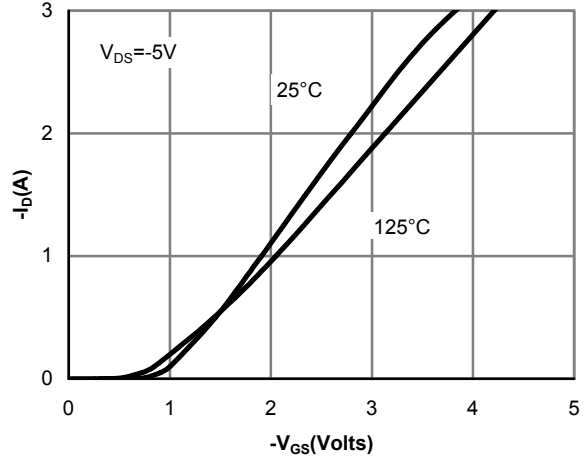


Figure 2: Transfer Characteristics

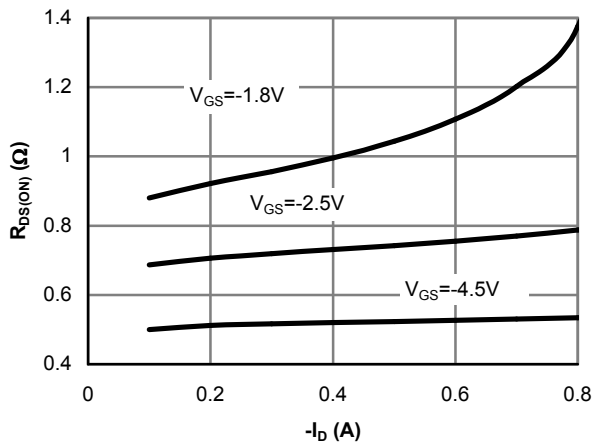


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

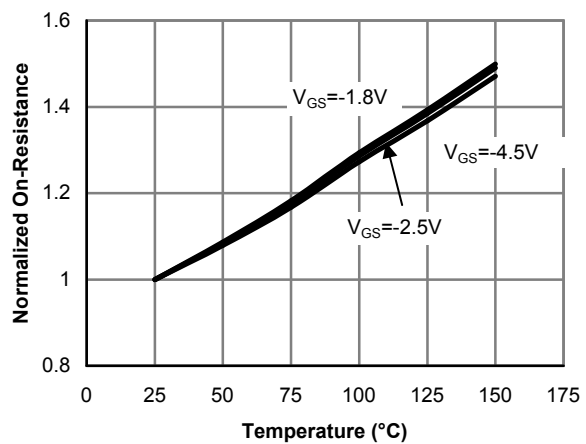


Figure 4: On-Resistance vs. Junction Temperature

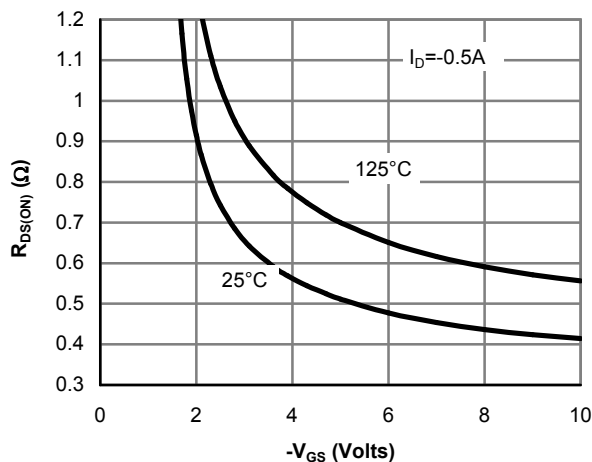


Figure 5: On-Resistance vs. Gate-Source Voltage

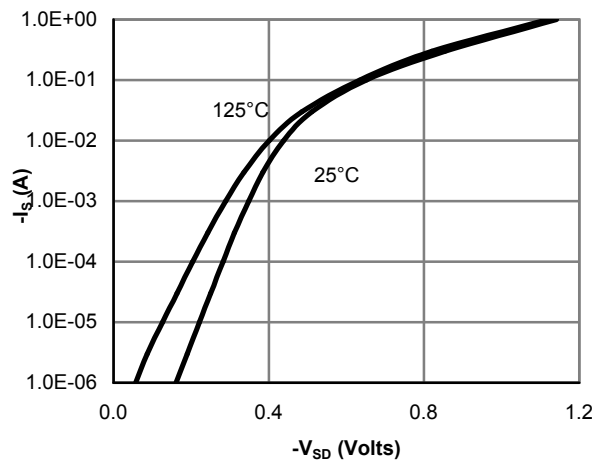


Figure 6: Body-Diode Characteristics

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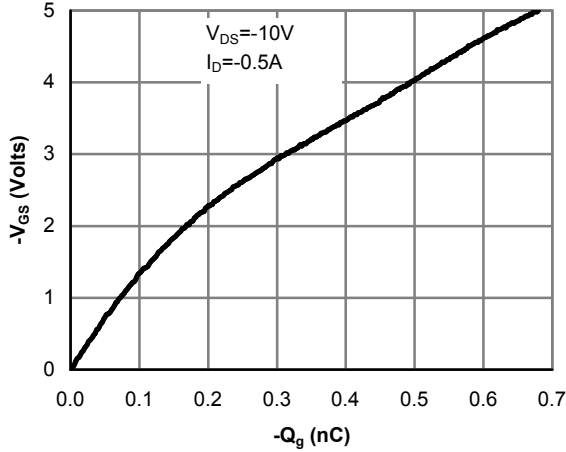


Figure 7: Gate-Charge Characteristics

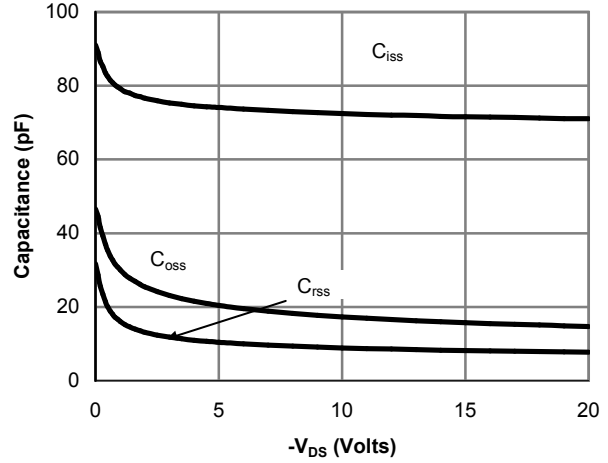


Figure 8: Capacitance Characteristics

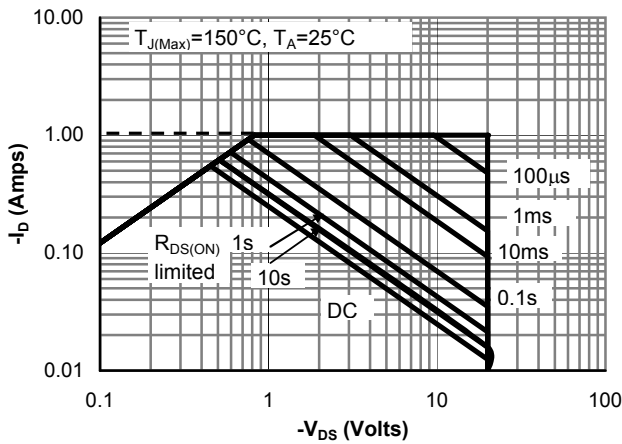


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

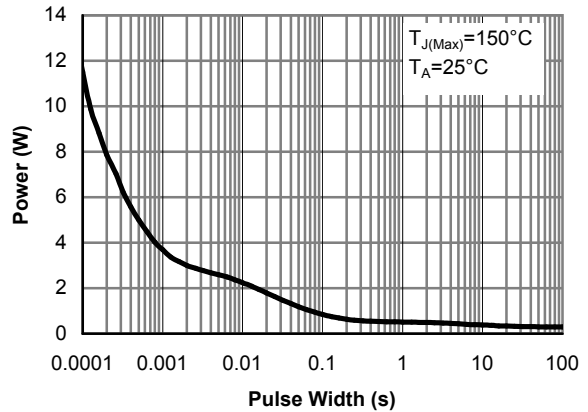


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

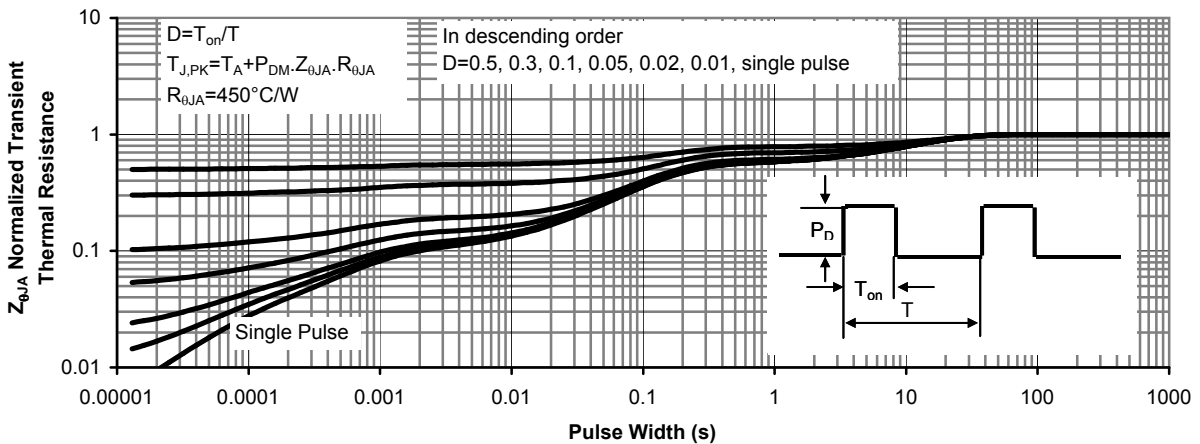
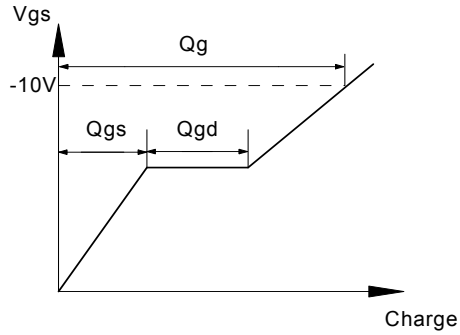
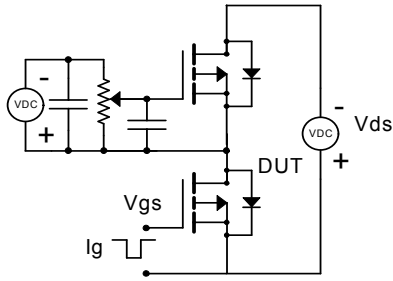


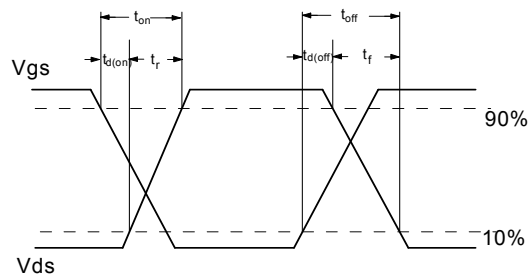
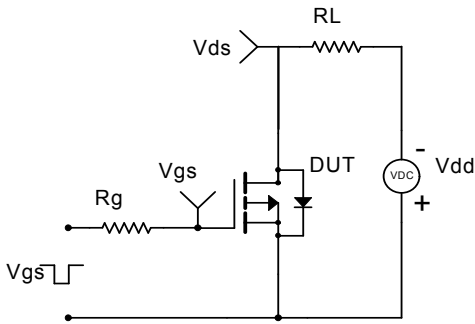
Figure 11: Normalized Maximum Transient Thermal Impedance

AO5401E

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

