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ALPHA & OMEGA SEMICONDUCTOR

AOT412/AOB412L

100V N-Channel MOSFET

SDMOS™
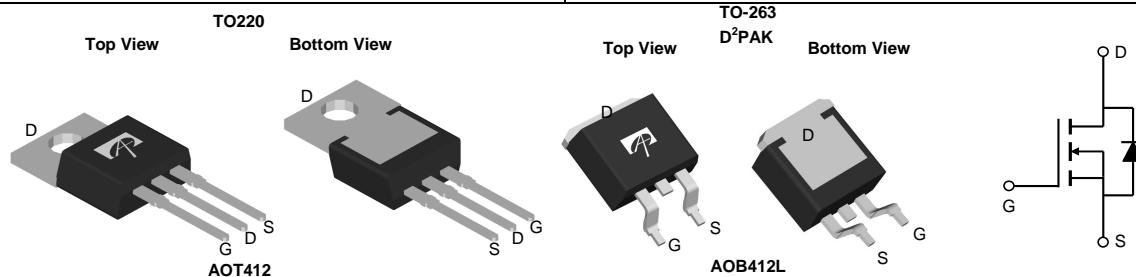
### General Description

The AOT412 & AOB412L are fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge & low Q_{rr}. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

Product Summary

V_{DS}	100V
I_D (at V_{GS}=10V)	60A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 15.8mΩ
$R_{DS(ON)}$ (at V_{GS} = 7V)	< 19.4mΩ

100% UIS Tested
100% R_g Tested

RoHS Compliant

TO220 — Top View / Bottom View — **AOT412**

TO-263 D²PAK — Top View / Bottom View — **AOB412L**

Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C=25℃	I_D	60	A
	T_C=100℃		44	
Pulsed Drain Current [C]		I_{DM}	140	
Continuous Drain Current	T_A=25℃	I_{DSM}	8.2	A
	T_A=70℃		6.6	
Avalanche Current [C]		I_{AS}, I_{AR}	47	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	110	mJ
Power Dissipation [B]	T_C=25℃	P_D	150	W
	T_C=100℃		75	
Power Dissipation [A]	T_A=25℃	P_{DSM}	2.6	W
	T_A=70℃		1.7	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{θJA}$	15	18	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	48	℃/W
Maximum Junction-to-Case	Steady-State	$R_{θJC}$	0.7	1	℃/W

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Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V		100			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=100V, V$_{GS}$=0V				10	µA
			T$_J$=55℃			50	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$= ±25V				100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$, I$_D$=250µA		2.6	3.2	3.8	V
I$_{D(ON)}$	On state drain current	V$_{GS}$=10V, V$_{DS}$=5V		140			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=20A			13.2	15.8	mΩ
		TO220	T$_J$=125℃		25	30	
		V$_{GS}$=7V, I$_D$=20A TO220			15.5	19.4	mΩ
		V$_{GS}$=10V, I$_D$=20A TO263			12.9	15.5	mΩ
		V$_{GS}$=7V, I$_D$=20A TO263			15.2	19.1	mΩ
g$_{FS}$	Forward Transconductance	V$_{DS}$=5V, I$_D$=20A			30		S
V$_{SD}$	Diode Forward Voltage	I$_S$=1A, V$_{GS}$=0V			0.65	1	V
I$_S$	Maximum Body-Diode Continuous Current					60	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=50V, f=1MHz		2150	2680	3220	pF
C$_{oss}$	Output Capacitance			180	260	340	pF
C$_{rss}$	Reverse Transfer Capacitance			60	100	140	pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz		0.5	1	1.5	Ω
SWITCHING PARAMETERS							
Q$_g$(10V)	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=50V, I$_D$=20A		36	45	54	nC
Q$_{gs}$	Gate Source Charge			14	17	20	nC
Q$_{gd}$	Gate Drain Charge			9	15	21	nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=50V, R$_L$=2Ω, R$_{GEN}$=3Ω			19		ns
t$_r$	Turn-On Rise Time				16		ns
t$_{D(off)}$	Turn-Off DelayTime				27		ns
t$_f$	Turn-Off Fall Time				10		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=20A, dI/dt=500A/µs		15	22	29	ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=20A, dI/dt=500A/µs		67	96	125	nC

A. The value of R$_{θJA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$ =25℃. The Power dissipation P$_{DSM}$ is based on R$_{θJA}$ and the maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design, and the maximum temperature of 175℃ may be used if the PCB allow s it.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=175℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=175℃. Ratings are based on low frequency and duty cycles to keep initial T$_J$ =25℃.

D. The R$_{θJA}$ is the sum of the thermal impedence from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=175℃. The SOA curve provides a single pulse ratin g.

G. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$=25℃.

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
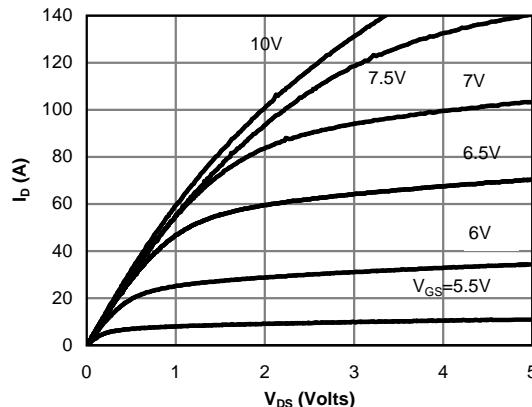
Fig 1: On-Region Characteristics (Note E)
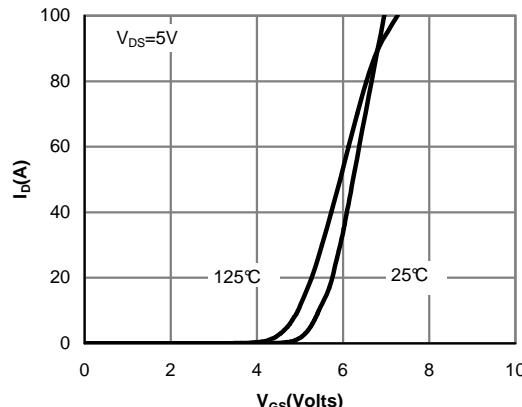


Figure 2: Transfer Characteristics (Note E)
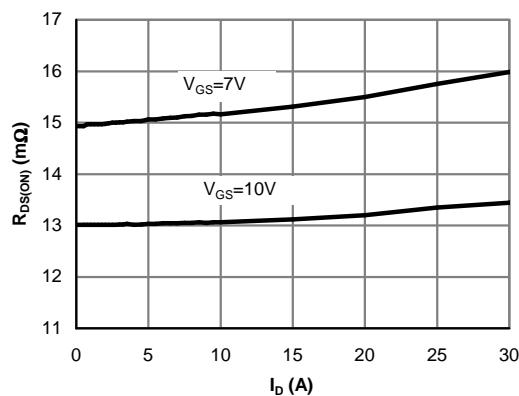
Figure 3: On-Resistance vs. Drain Current and Gate
Voltage (Note E)
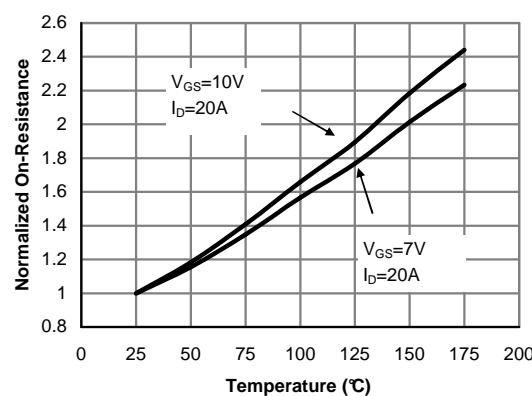
Figure 4: On-Resistance vs. Junction Temperature
(Note E)
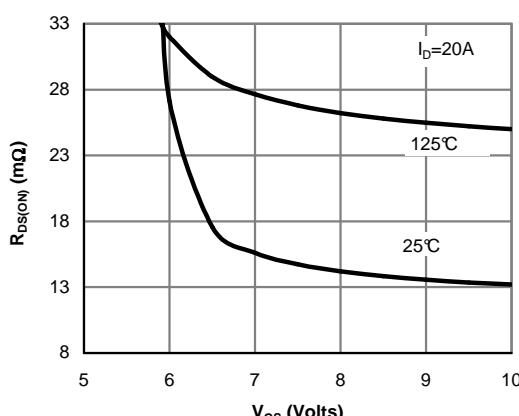

Figure 5: On-Resistance vs. Gate-Source Voltage
(Note E)
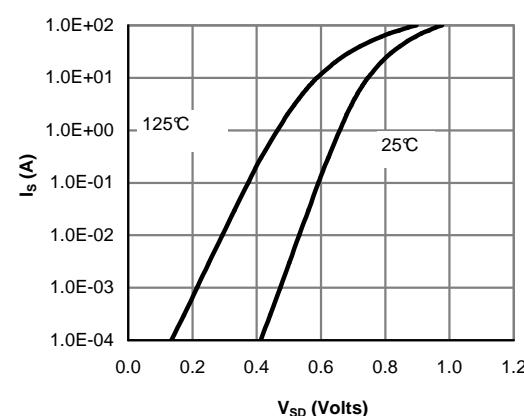
Figure 6: Body-Diode Characteristics (Note E)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

V_{DS}=50V
I_D=20A
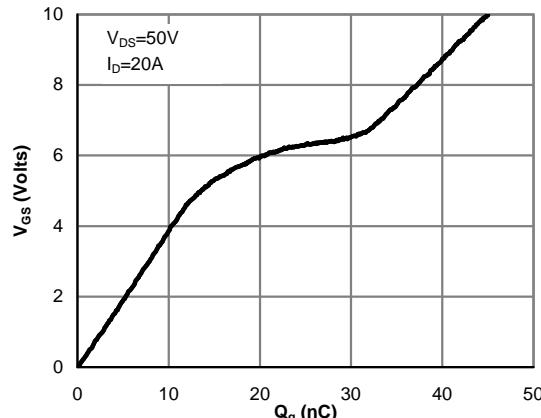
Figure 7: Gate-Charge Characteristics

C_{iss}

C_{oss} C_{rss}
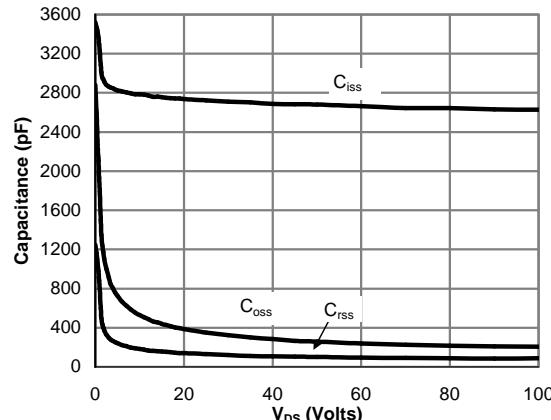
Figure 8: Capacitance Characteristics

$R_{DS(ON)}$ limited

DC

10µs
100µs
1ms
10ms

$T_{J(Max)}$=175℃
T_C=25℃
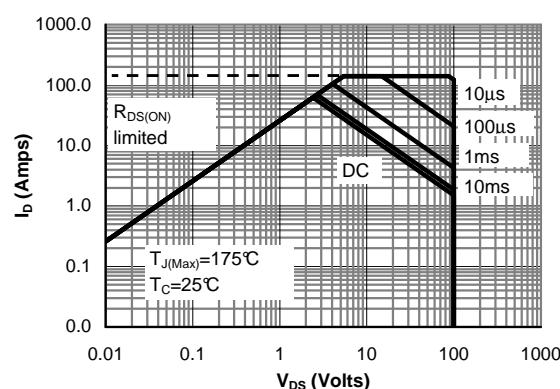
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

$T_{J(Max)}$=175℃
T_C=25℃
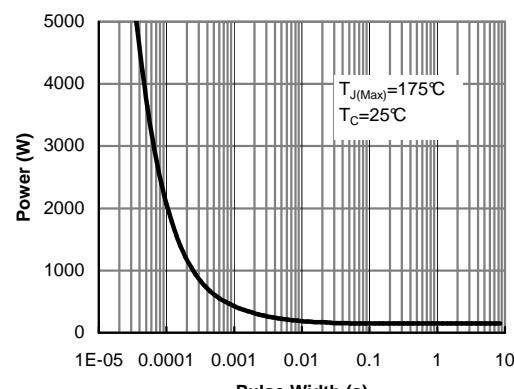
Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

$D=T_{on}/T$
$T_{J,PK}=T_C+P_{DM}\cdot Z_{\theta JC}\cdot R_{\theta JC}$
$R_{\theta JC}$=1℃/W

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse

P_D

T_{on}

T
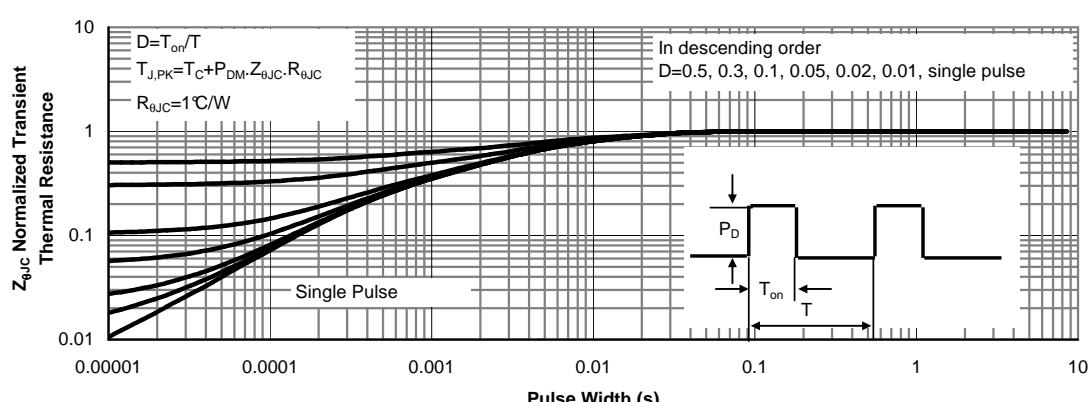
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
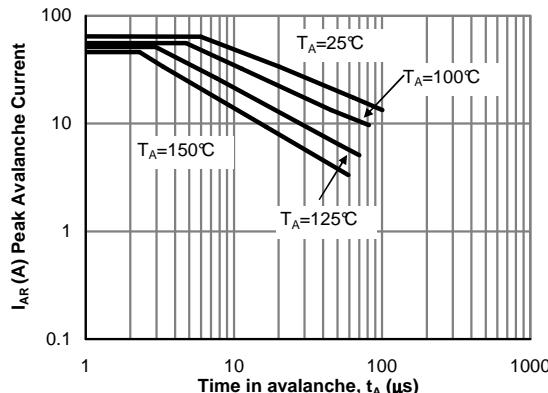
Figure 12: Single Pulse Avalanche capability (Note C)
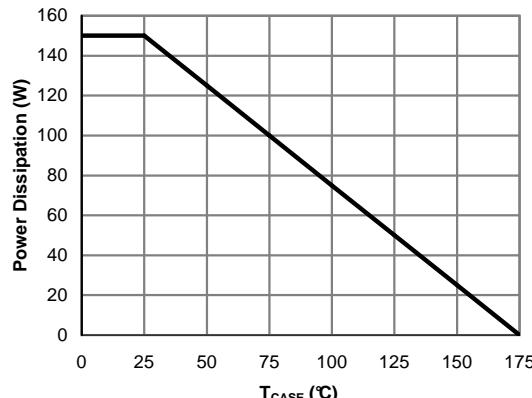

Figure 13: Power De-rating (Note F)
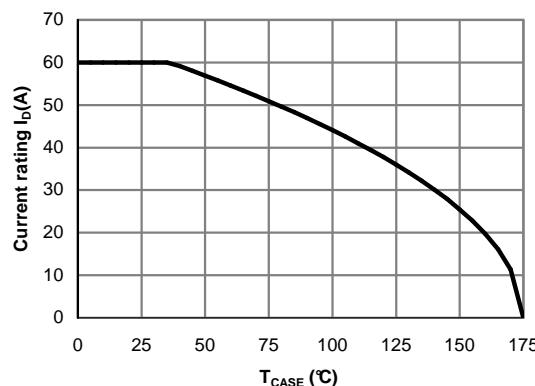

Figure 14: Current De-rating (Note F)
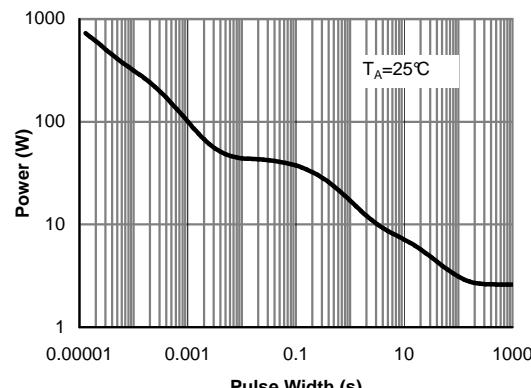

Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)
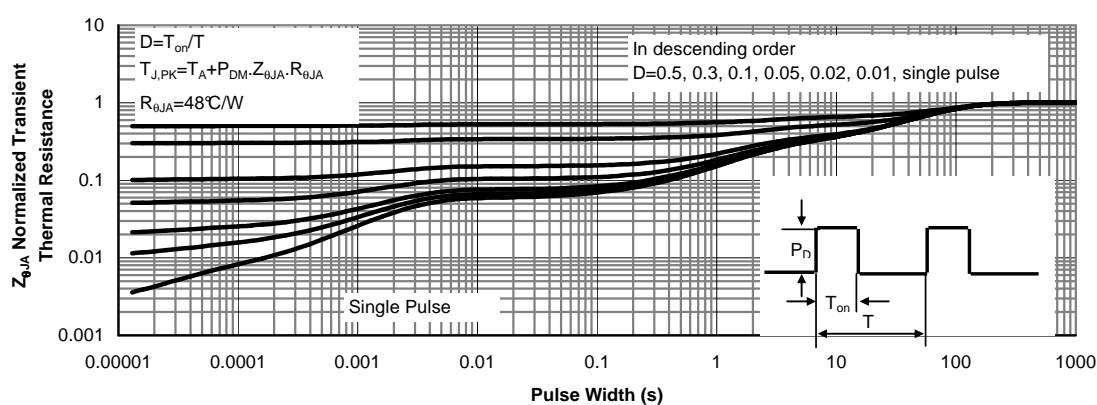
Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

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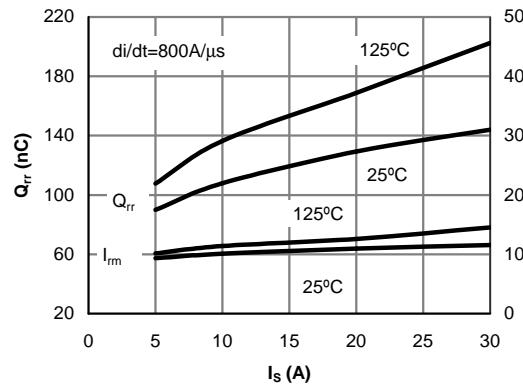
Figure 17: Diode Reverse Recovery Charge and Peak
Current vs. Conduction Current
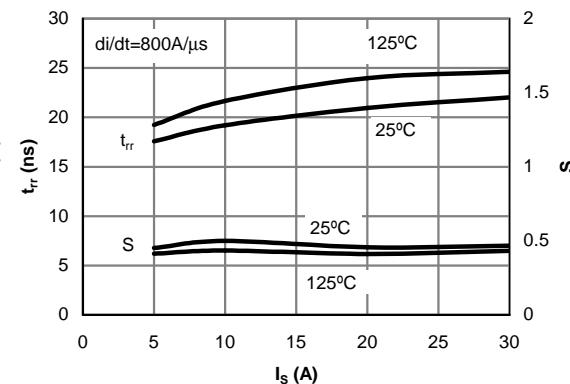
Figure 18: Diode Reverse Recovery Time and
Softness Factor vs. Conduction Current
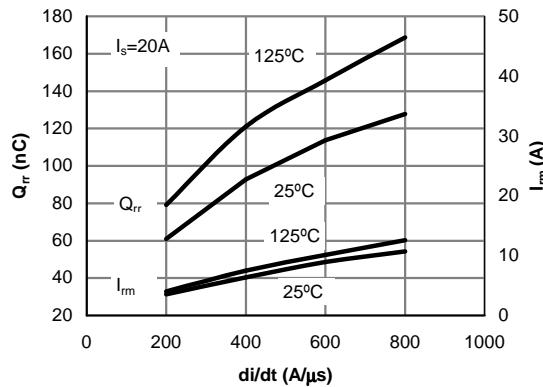
Figure 19: Diode Reverse Recovery Charge and
Peak Current vs. di/dt
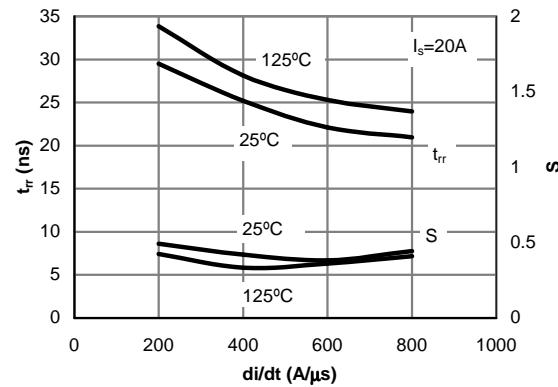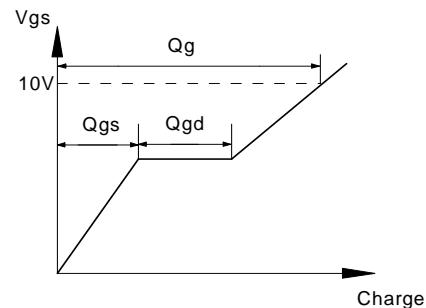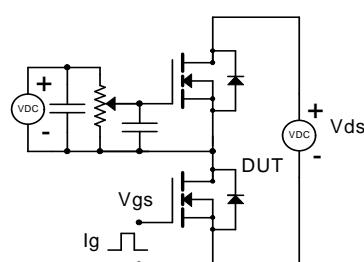
Figure 20: Diode Reverse Recovery Time and
Softness Factor vs. di/dt

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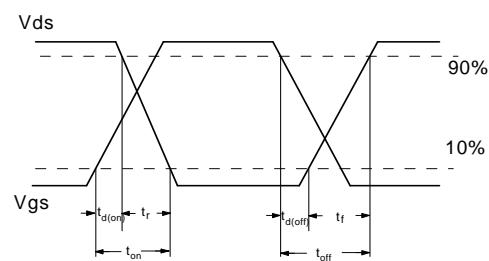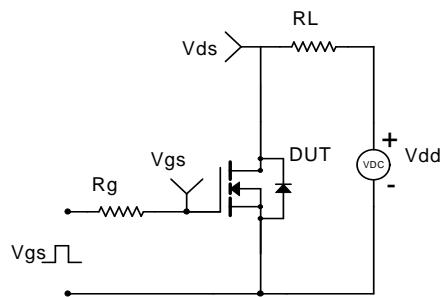
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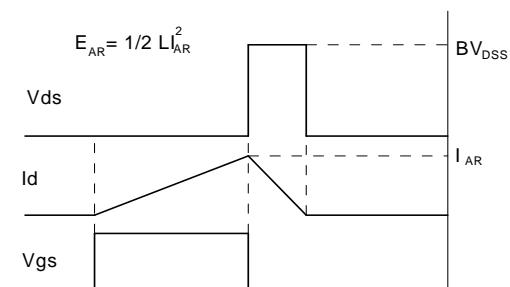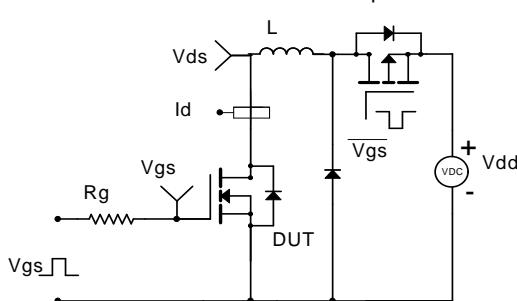
Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2 \, LI_{AR}^2$$

Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int Idt$$