

# FDMS3626S

## PowerTrench® Power Stage

### 25V Asymmetric Dual N-Channel MOSFET

#### Features

Q1: N-Channel

■ Max  $r_{DS(on)}$  = 5.0 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 17.5 A

■ Max  $r_{DS(on)}$  = 5.7 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 16 A

Q2: N-Channel

■ Max  $r_{DS(on)}$  = 2.6 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 25 A

■ Max  $r_{DS(on)}$  = 3.2 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 22 A

■ Low inductance packaging shortens rise/fall times, resulting in lower switching losses

■ MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing

■ RoHS Compliant

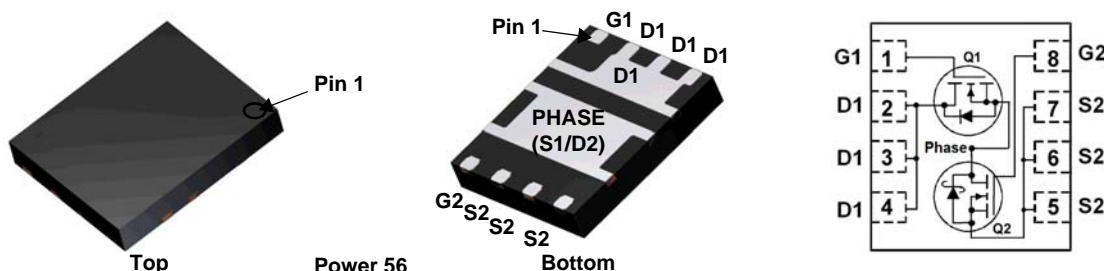


#### General Description

This device includes two specialized N-Channel MOSFETs in a dual PQFN package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

#### Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE



#### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol         | Parameter  | Q1                 | Q2                | Units            |
|----------------|--|--------------------|-------------------|------------------|
| $V_{DS}$       | Drain to Source Voltage  | 25                 | 25                | V                |
| $V_{GS}$       | Gate to Source Voltage (Note 4)                                      | $\pm 12$           | $\pm 12$          | V                |
| $I_D$          | Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$ | 30                 | 55                | A                |
|                | -Continuous $T_A = 25^\circ\text{C}$                                 | 17.5 <sup>1a</sup> | 25 <sup>1b</sup>  |                  |
|                | -Pulsed  | 70                 | 100               |                  |
| $E_{AS}$       | Single Pulse Avalanche Energy (Note 3)                               | 29                 | 45                | mJ               |
| $P_D$          | Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$      | 2.2 <sup>1a</sup>  | 2.5 <sup>1b</sup> | W                |
|                | Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$      | 1.0 <sup>1c</sup>  | 1.0 <sup>1d</sup> |                  |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range                     | -55 to +150        |                   | $^\circ\text{C}$ |

#### Thermal Characteristics

|                 |   |                   |                   |                    |
|-----------------|---|-------------------|-------------------|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 57 <sup>1a</sup>  | 50 <sup>1b</sup>  | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 125 <sup>1c</sup> | 120 <sup>1d</sup> |                    |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case    | 3.0               | 3.0               |                    |

#### Package Marking and Ordering Information

| Device Marking | Device    | Package  | Reel Size | Tape Width | Quantity   |
|----------------|-----------|----------|-----------|------------|------------|
| 080D<br>100D   | FDMS3626S | Power 56 | 13 "      | 12 mm      | 3000 units |

**Electrical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|--------|-----------|-----------------|------|-----|-----|-----|-------|
|--------|-----------|-----------------|------|-----|-----|-----|-------|

**Off Characteristics**

|                                      |   |  |          |          |          |                        |                                |
|--------------------------------------|---|--|----------|----------|----------|------------------------|--------------------------------|
| $BV_{DSS}$                           | Drain to Source Breakdown Voltage         | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$<br>$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$  | Q1<br>Q2 | 25<br>25 |          |                        | V                              |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$<br>$I_D = 10\text{ mA}$ , referenced to $25\text{ }^{\circ}\text{C}$ | Q1<br>Q2 |          | 12<br>25 |                        | mV/ $^{\circ}\text{C}$         |
| $I_{DSS}$                            | Zero Gate Voltage Drain Current           | $V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$   | Q1<br>Q2 |          |          | 1<br>500               | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$                            | Gate to Source Leakage Current            | $V_{GS} = 12\text{ V}/-8\text{ V}$ , $V_{DS} = 0\text{ V}$   | Q1<br>Q2 |          |          | $\pm 100$<br>$\pm 100$ | nA<br>nA                       |

**On Characteristics**

|  |  |  |          |            |            |            |                        |
|--|--|--|----------|------------|------------|------------|------------------------|
| $V_{GS(th)}$                           | Gate to Source Threshold Voltage                         | $V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$<br>$V_{GS} = V_{DS}$ , $I_D = 1\text{ mA}$  | Q1<br>Q2 | 0.8<br>1.1 | 1.2<br>1.4 | 2.0<br>2.2 | V                      |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$<br>$I_D = 10\text{ mA}$ , referenced to $25\text{ }^{\circ}\text{C}$ | Q1<br>Q2 |            | -4<br>-3   |            | mV/ $^{\circ}\text{C}$ |
| $r_{DS(on)}$                           | Drain to Source On Resistance                            | $V_{GS} = 10\text{ V}$ , $I_D = 17.5\text{ A}$   | Q1       |            | 3.8        | 5.0        | m $\Omega$             |
|  |  | $V_{GS} = 4.5\text{ V}$ , $I_D = 16\text{ A}$  |          |            | 4.4        | 5.7        |                        |
|  |  | $V_{GS} = 10\text{ V}$ , $I_D = 17.5\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$   |          |            | 5.4        | 7.0        |                        |
|  |  | $V_{GS} = 10\text{ V}$ , $I_D = 25\text{ A}$   | Q2       |            | 2.1        | 2.6        |                        |
| $g_{FS}$                               | Forward Transconductance                                 | $V_{DS} = 5\text{ V}$ , $I_D = 17.5\text{ A}$  | Q1       |            | 100        |            | S                      |
|  |  | $V_{DS} = 5\text{ V}$ , $I_D = 25\text{ A}$  | Q2       |            | 227        |            |                        |
|  |  |  |          |            |            |            |                        |

**Dynamic Characteristics**

|           |                              |  |          |  |              |  |          |
|-----------|------------------------------|--|----------|--|--------------|--|----------|
| $C_{iss}$ | Input Capacitance            | Q1:<br>$V_{DS} = 13\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ | Q1<br>Q2 |  | 1570<br>2545 |  | pF       |
| $C_{oss}$ | Output Capacitance           | Q2:<br>$V_{DS} = 13\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ | Q1<br>Q2 |  | 448<br>716   |  | pF       |
| $C_{rss}$ | Reverse Transfer Capacitance |  | Q1<br>Q2 |  | 61<br>103    |  | pF       |
| $R_g$     | Gate Resistance              |  | Q1<br>Q2 |  | 0.4<br>0.9   |  | $\Omega$ |

**Switching Characteristics**

|              |                               |  |          |  |            |  |    |
|--------------|-------------------------------|--|----------|--|------------|--|----|
| $t_{d(on)}$  | Turn-On Delay Time            | Q1:<br>$V_{DD} = 13\text{ V}$ , $I_D = 17.5\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$<br>Q2:<br>$V_{DD} = 13\text{ V}$ , $I_D = 25\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$ | Q1<br>Q2 |  | 7<br>8     |  | ns |
| $t_r$        | Rise Time                     |  | Q1<br>Q2 |  | 2<br>4     |  | ns |
| $t_{d(off)}$ | Turn-Off Delay Time           |  | Q1<br>Q2 |  | 23<br>31   |  | ns |
| $t_f$        | Fall Time                     |  | Q1<br>Q2 |  | 2<br>3     |  | ns |
| $Q_g$        | Total Gate Charge             | $V_{GS} = 0\text{ V}$ to $10\text{ V}$   | Q1<br>Q2 |  | 26<br>41   |  | nC |
| $Q_g$        | Total Gate Charge             | $V_{GS} = 0\text{ V}$ to $4.5\text{ V}$  | Q1<br>Q2 |  | 12<br>19   |  | nC |
| $Q_{gs}$     | Gate to Source Gate Charge    | Q2<br>$V_{DD} = 13\text{ V}$ ,<br>$I_D = 25\text{ A}$  | Q1<br>Q2 |  | 3.3<br>4.9 |  | nC |
| $Q_{gd}$     | Gate to Drain "Miller" Charge |  | Q1<br>Q2 |  | 2.7<br>4.3 |  | nC |

**Electrical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted

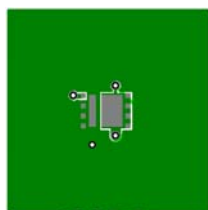
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|--------|-----------|-----------------|------|-----|-----|-----|-------|
|--------|-----------|-----------------|------|-----|-----|-----|-------|

**Drain-Source Diode Characteristics**

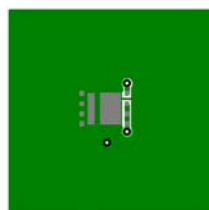
|          |                                       |  |    |  |     |     |    |
|----------|---------------------------------------|--|----|--|-----|-----|----|
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}$ , $I_S = 17.5\text{ A}$ (Note 2)           | Q1 |  | 0.8 | 1.2 | V  |
|          |                                       | $V_{GS} = 0\text{ V}$ , $I_S = 25\text{ A}$ (Note 2)             | Q2 |  | 0.8 | 1.2 |    |
| $t_{rr}$ | Reverse Recovery Time                 | Q1<br>$I_F = 17.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ | Q1 |  | 23  |     | ns |
|          |                                       |  | Q2 |  | 23  |     |    |
| $Q_{rr}$ | Reverse Recovery Charge               | Q2<br>$I_F = 25\text{ A}$ , $di/dt = 300\text{ A}/\mu\text{s}$   | Q1 |  | 9   |     | nC |
|          |                                       |  | Q2 |  | 22  |     |    |

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



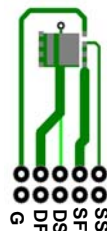
a. 57  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 50  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



c. 125  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper



d. 120  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Q1 :  $E_{AS}$  of 29 mJ is based on starting  $T_J = 25\text{ }^{\circ}\text{C}$ ; N-ch:  $L = 1.2\text{ mH}$ ,  $I_{AS} = 7\text{ A}$ ,  $V_{DD} = 23\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 16\text{ A}$ .

Q2:  $E_{AS}$  of 45 mJ is based on starting  $T_J = 25\text{ }^{\circ}\text{C}$ ; N-ch:  $L = 0.4\text{ mH}$ ,  $I_{AS} = 15\text{ A}$ ,  $V_{DD} = 23\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 23.8\text{ A}$ .

4. As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

# Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

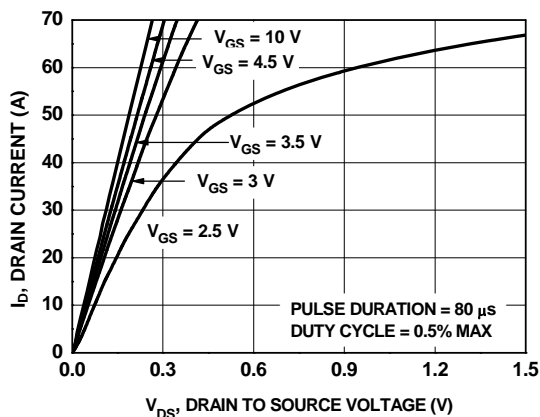


Figure 1. On Region Characteristics

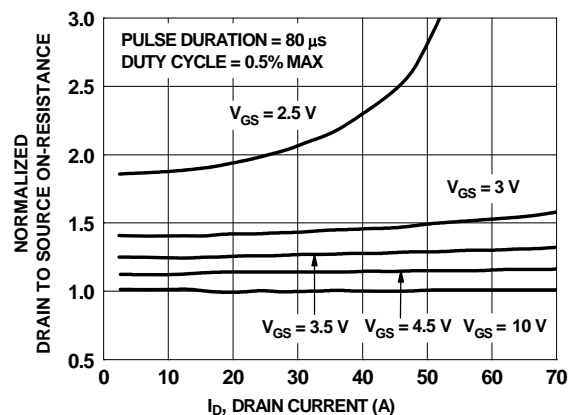


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

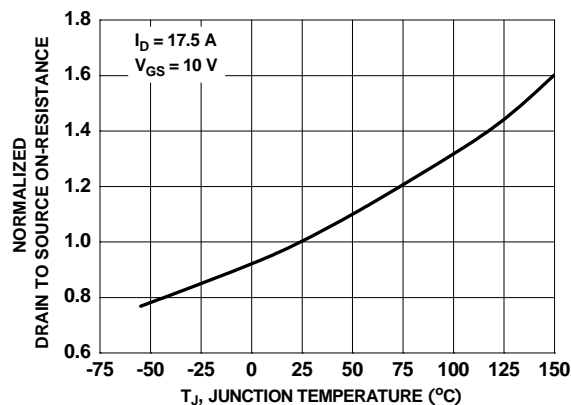


Figure 3. Normalized On Resistance vs Junction Temperature

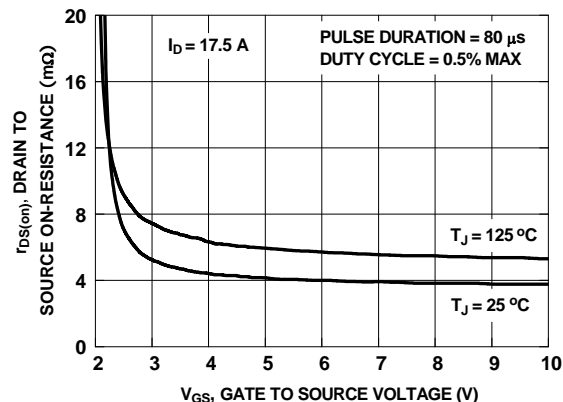


Figure 4. On-Resistance vs Gate to Source Voltage

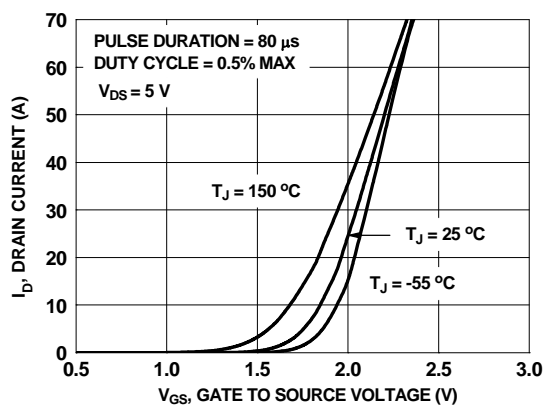


Figure 5. Transfer Characteristics

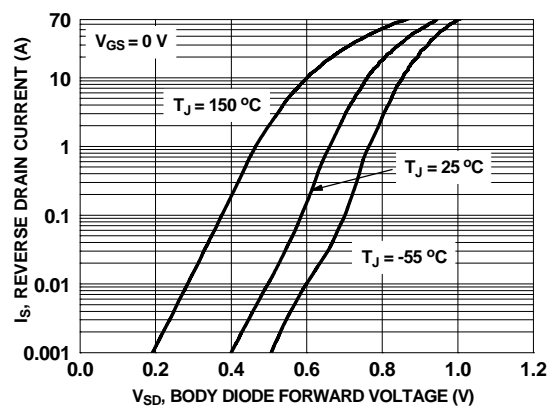


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

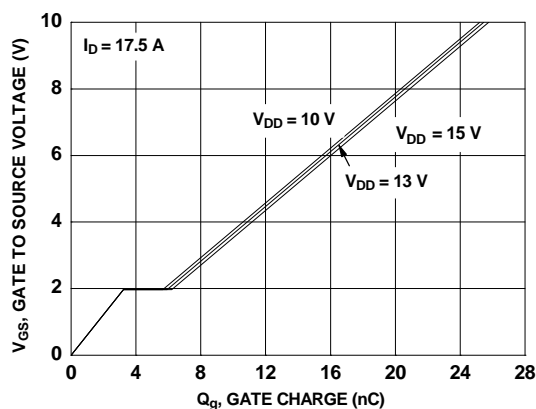


Figure 7. Gate Charge Characteristics

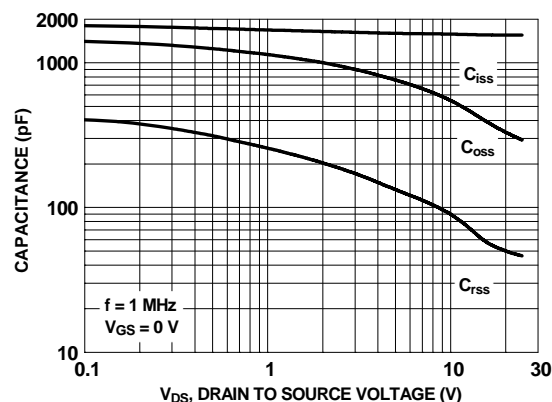


Figure 8. Capacitance vs Drain to Source Voltage

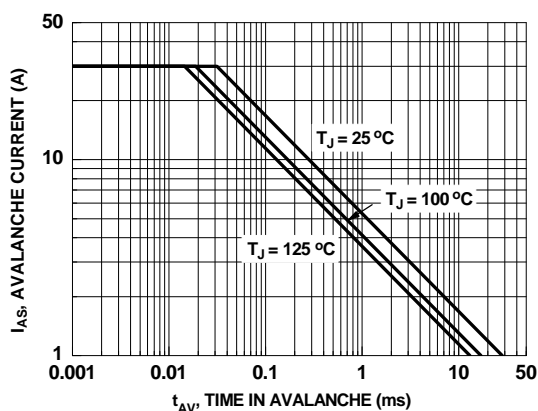


Figure 9. Unclamped Inductive Switching Capability

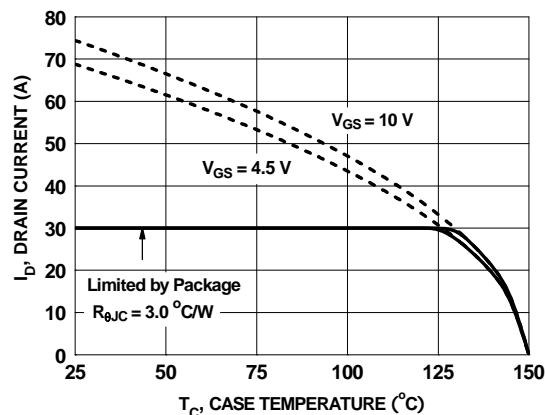


Figure 10. Maximum Continuous Drain Current vs Case Temperature

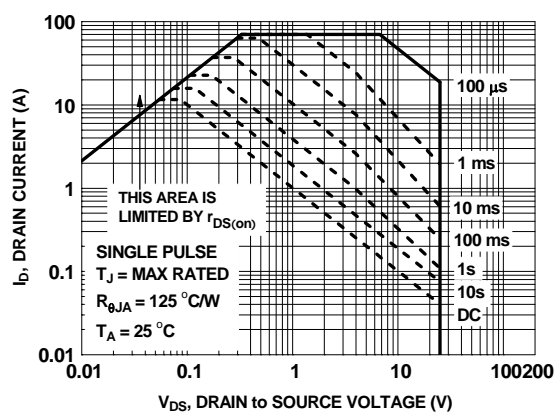


Figure 11. Forward Bias Safe Operating Area

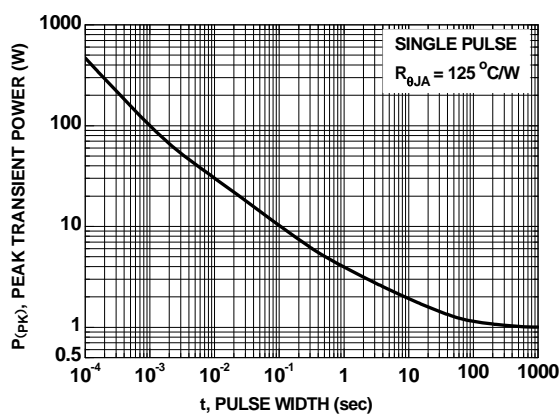


Figure 12. Single Pulse Maximum Power Dissipation

# Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

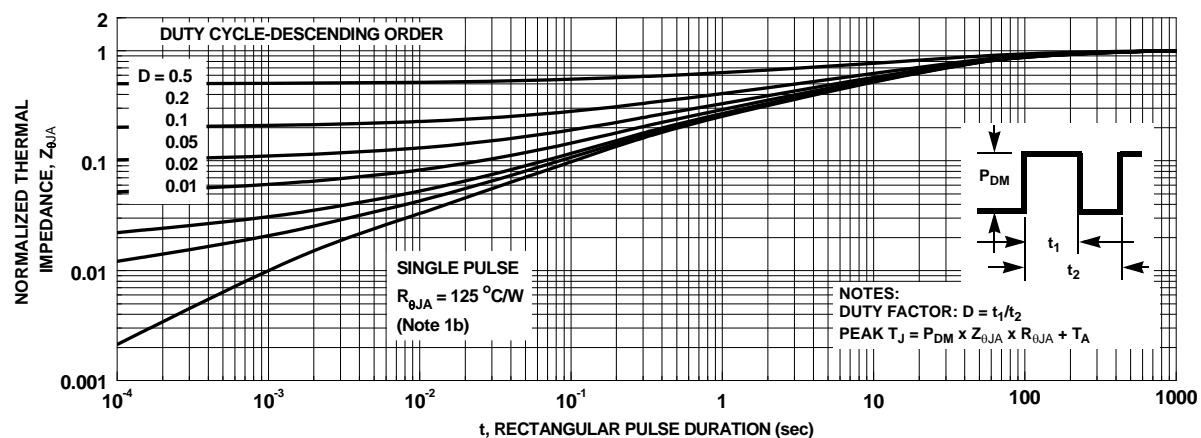


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

# Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

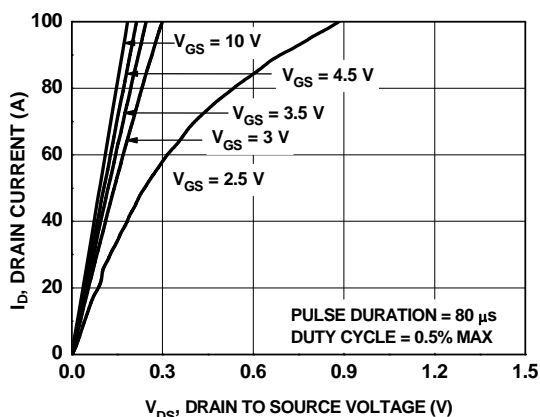


Figure 14. On-Region Characteristics

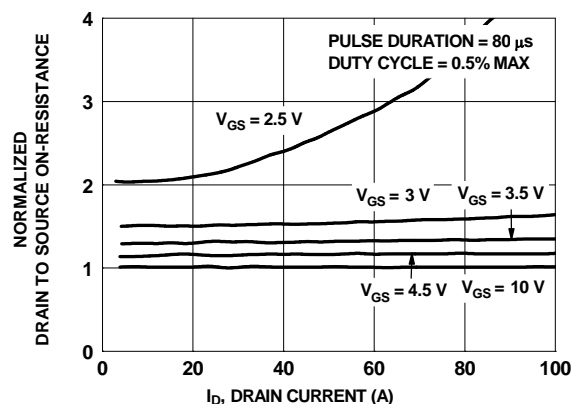


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

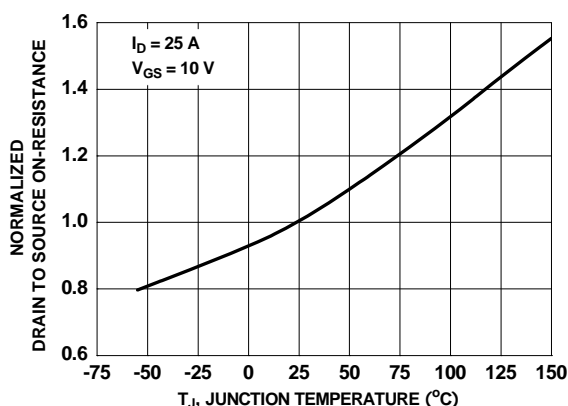


Figure 16. Normalized On-Resistance vs Junction Temperature

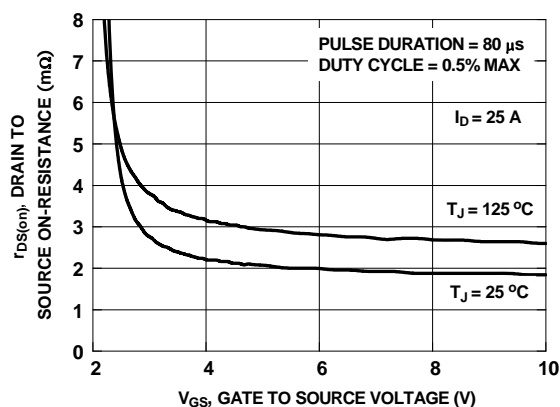


Figure 17. On-Resistance vs Gate to Source Voltage

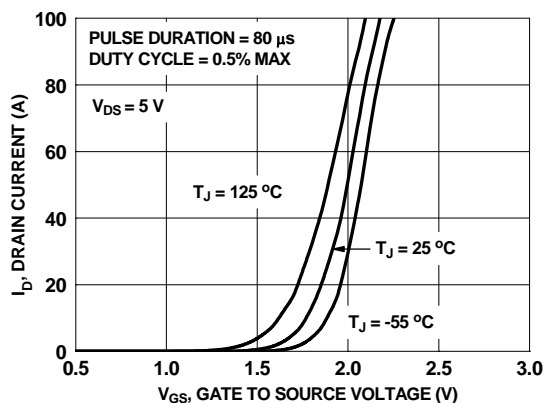


Figure 18. Transfer Characteristics

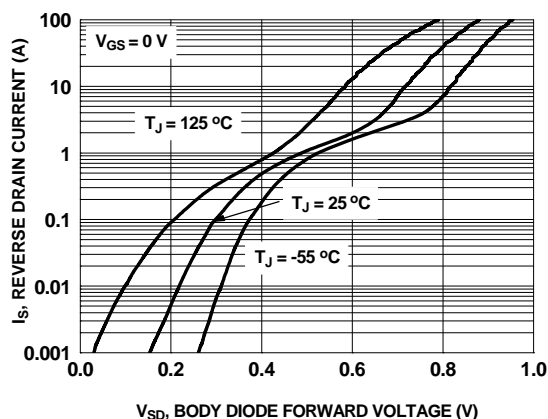


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

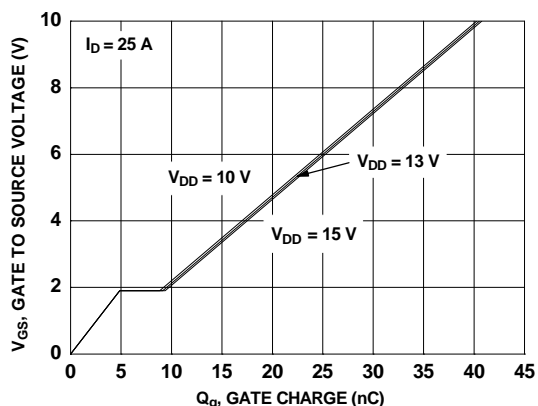


Figure 20. Gate Charge Characteristics

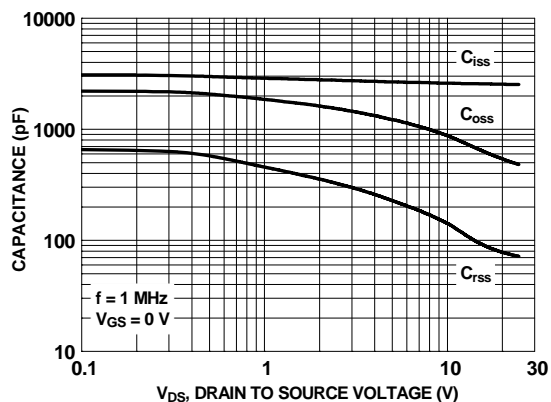


Figure 21. Capacitance vs Drain to Source Voltage

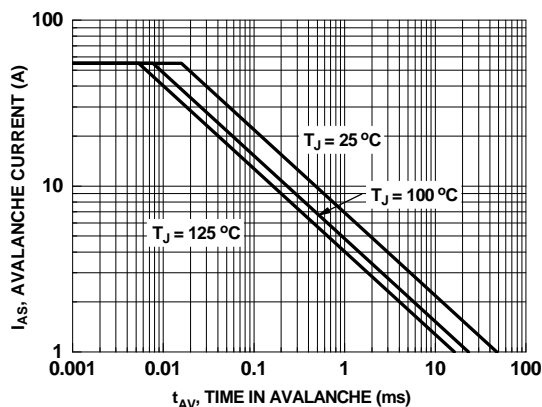


Figure 22. Unclamped Inductive Switching Capability

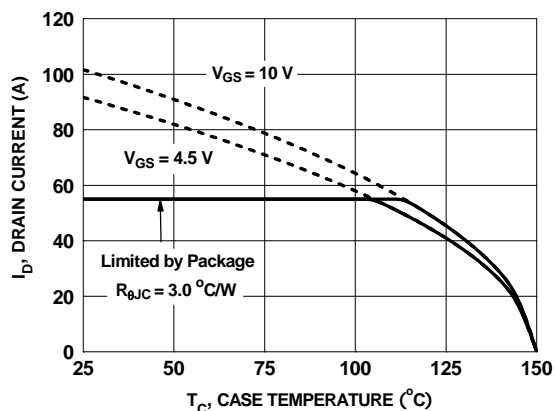


Figure 23. Maximum Continuous Drain Current vs Case Temperature

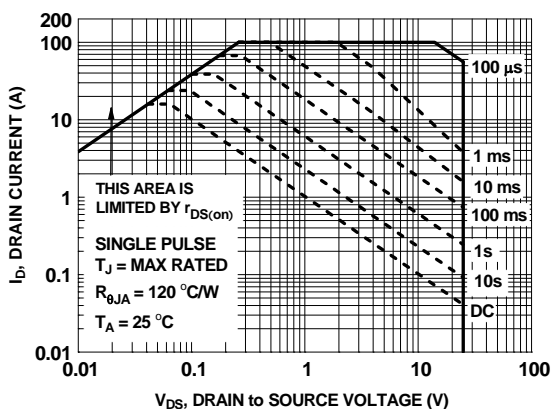


Figure 24. Forward Bias Safe Operating Area

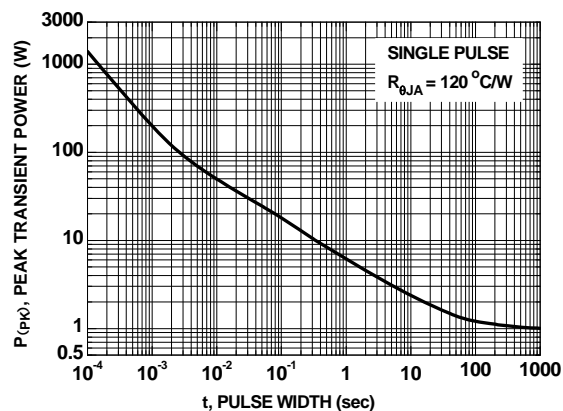


Figure 25. Single Pulse Maximum Power Dissipation



# Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

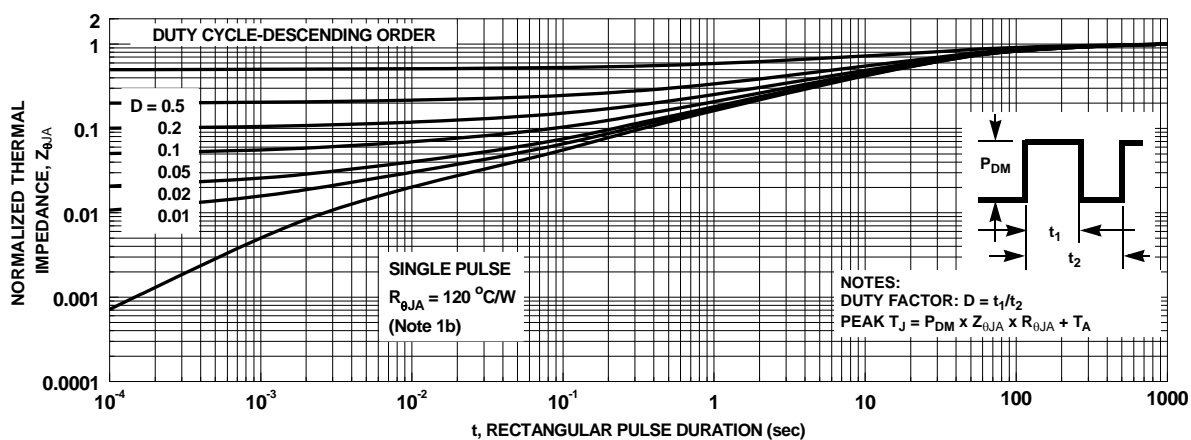


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

## Typical Characteristics (continued)

### SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS3626S.

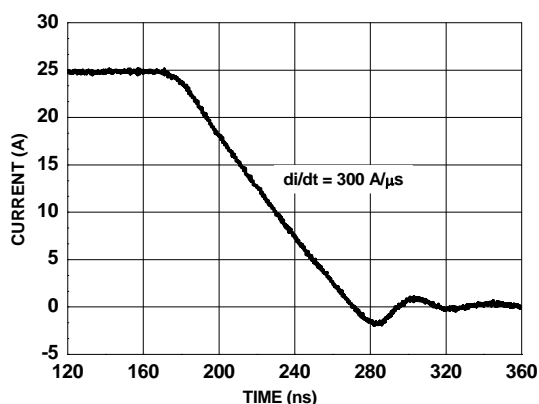


Figure 27. FDMS3626S SyncFET body diode reverse recovery characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

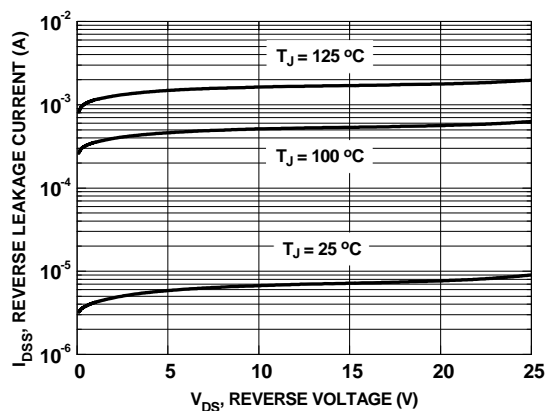
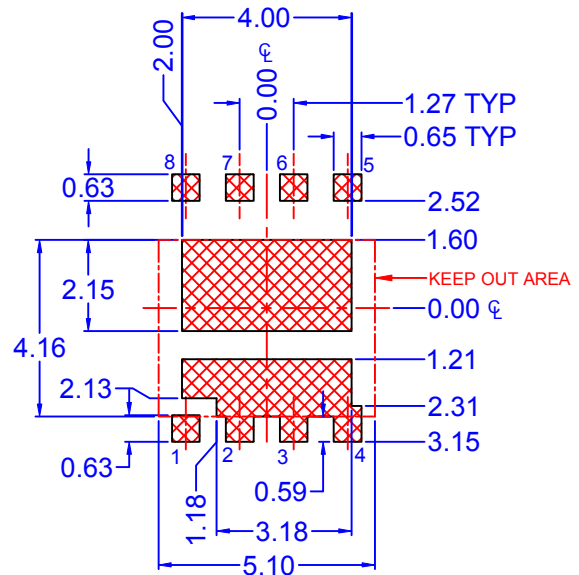
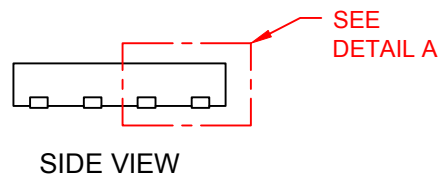
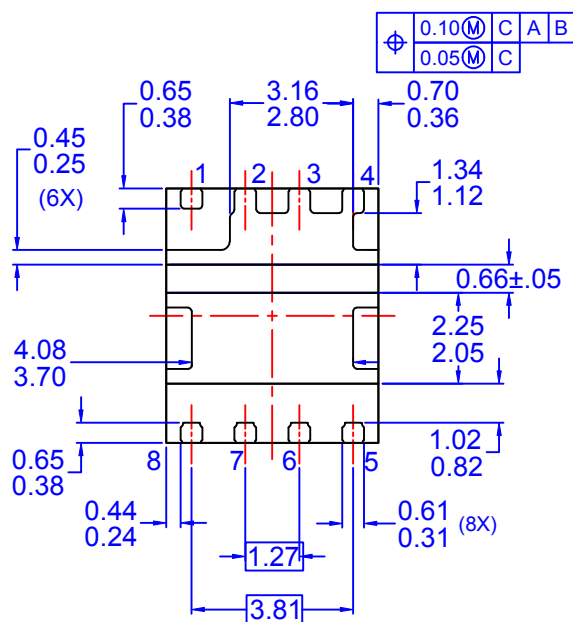


Figure 28. SyncFET body diode reverse leakage versus drain-source voltage



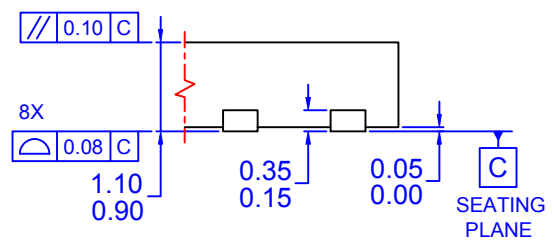
### RECOMMENDED LAND PATTERN FOR SAWN / PUNCHED TYPE



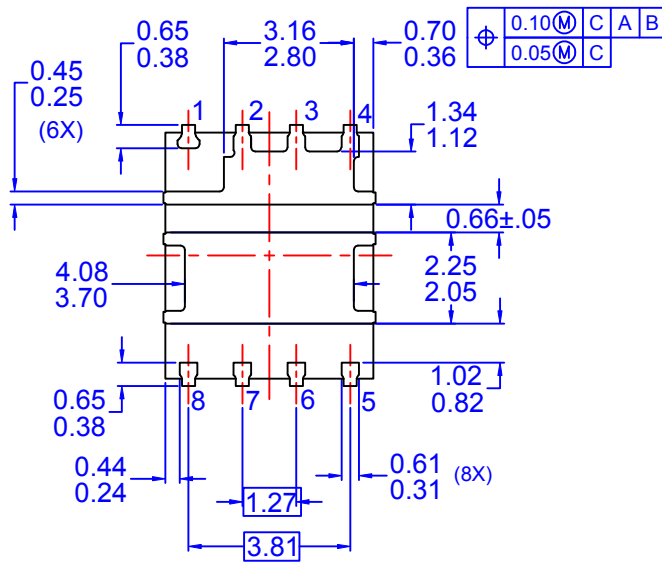
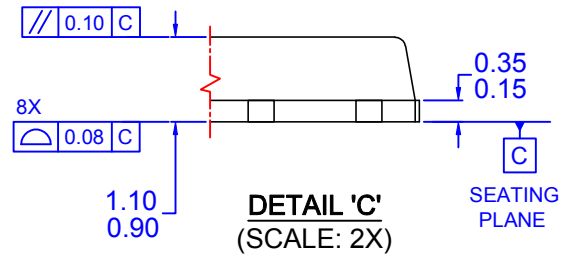
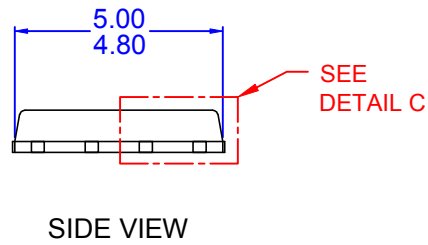
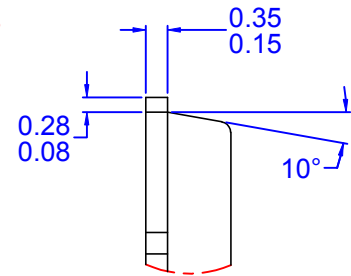
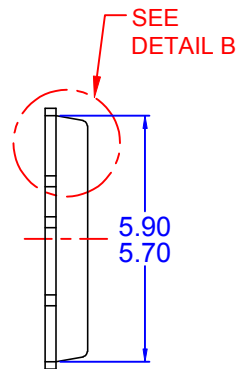
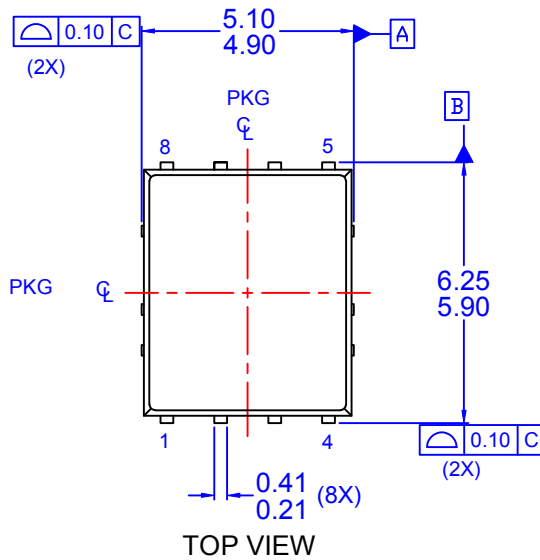
BOTTOM VIEW

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OPTION - A (SAWN TYPE)



**DETAIL 'A'**  
(SCALE: 2X)



OPTION - B (PUNCHED TYPE)

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE:  
JEDEC REGISTRATION, MO-240, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: PQFN08EREV6.
  - G) FAIRCHILD SEMICONDUCTOR



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### Definition of Terms

| Datasheet Identification | Product Status        | Definition  |
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