



FDMS86101DC

N-Channel Dual Cool™ 56 Shielded Gate PowerTrench® MOSFET

100 V, 60 A, 7.5 mΩ

Features

- Shielded Gate MOSFET Technology
- Dual Cool™ Top Side Cooling PQFN package
- Max $r_{DS(on)}$ = 7.5 mΩ at $V_{GS} = 10$ V, $I_D = 14.5$ A
- Max $r_{DS(on)}$ = 12 mΩ at $V_{GS} = 6$ V, $I_D = 11.5$ A
- High performance technology for extremely low $r_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

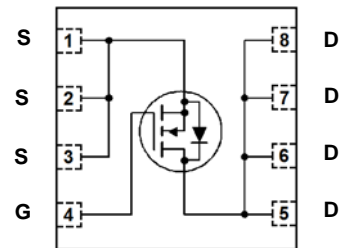
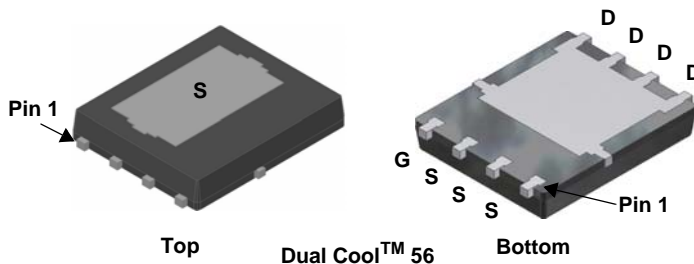


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Applications

- Primary DC-DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Conditions	Rated Value	Units
V_{DS}	Drain to Source Voltage		100	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	-Continuous $T_C = 25$ °C	60	A
		-Continuous $T_A = 25$ °C (Note 1a)	14.5	
		-Pulsed	200	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	216	mJ
P_D	Power Dissipation	$T_C = 25$ °C	125	W
		$T_A = 25$ °C (Note 1a)	3.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

Symbol	Parameter	Conditions	Rated Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	2.3	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
86101	FDMS86101DC	Dual Cool™ 56	13"	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		70		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2	2.7	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-10		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 14.5\ \text{A}$		6	7.5	m Ω
		$V_{GS} = 6\ \text{V}, I_D = 11.5\ \text{A}$		8.3	12	
		$V_{GS} = 10\ \text{V}, I_D = 14.5\ \text{A}, T_J = 125^\circ\text{C}$		10	13	
g_{FS}	Forward Transconductance	$V_{DD} = 10\ \text{V}, I_D = 14.5\ \text{A}$		44		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$		2354	3135	pF
C_{oss}	Output Capacitance			467	625	pF
C_{rss}	Reverse Transfer Capacitance			23	35	pF
R_g	Gate Resistance			0.1	1.4	3

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}, I_D = 14.5\ \text{A},$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		14	25	ns
t_r	Rise Time			8.2	17	ns
$t_{d(off)}$	Turn-Off Delay Time			25	40	ns
t_f	Fall Time			5.5	11	ns
$Q_g(TOT)$	Total Gate Charge		$V_{GS} = 0\ \text{V to } 10\ \text{V}$		31	44
	Total Gate Charge	$V_{GS} = 0\ \text{V to } 5\ \text{V}$	$V_{DD} = 50\ \text{V}$ $I_D = 14.5\ \text{A}$	18	25	nC
Q_{gs}	Total Gate Charge			8.3		nC
Q_{gd}	Gate to Drain "Miller" Charge			7		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 2.7\ \text{A}$ (Note 2)		0.71	1.2	V
		$V_{GS} = 0\ \text{V}, I_S = 14.5\ \text{A}$ (Note 2)		0.78	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 14.5\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		54	87	ns
Q_{rr}	Reverse Recovery Charge			62	99	nC

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

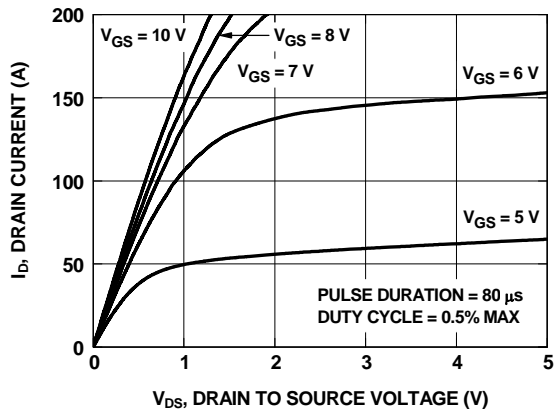


Figure 1. On-Region Characteristics

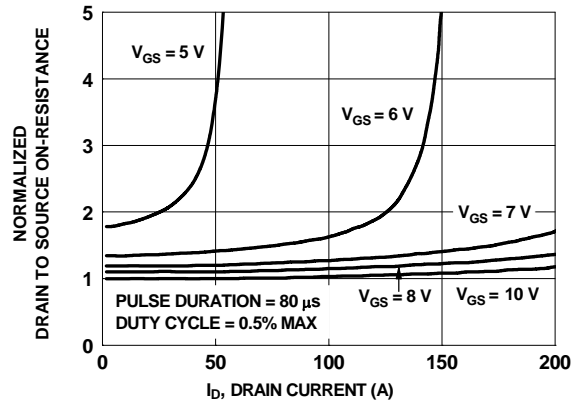


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

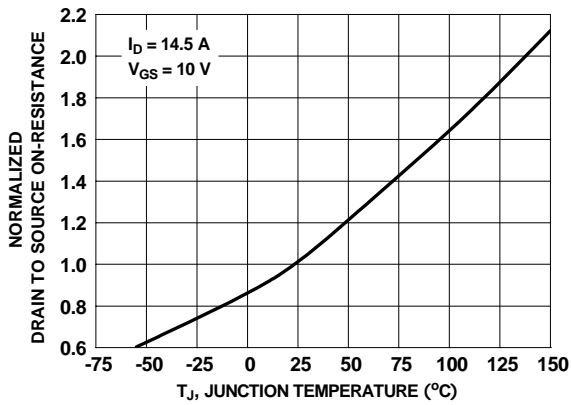


Figure 3. Normalized On-Resistance vs Junction Temperature

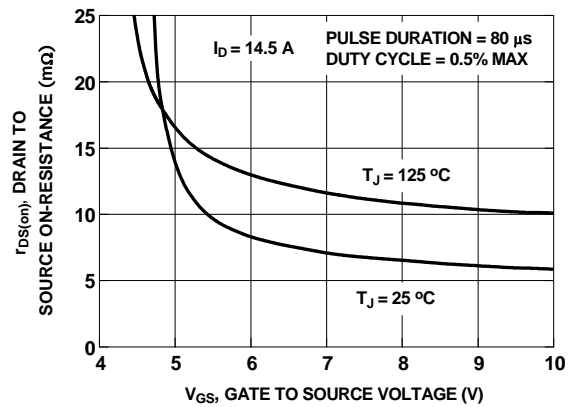


Figure 4. On-Resistance vs Gate to Source Voltage

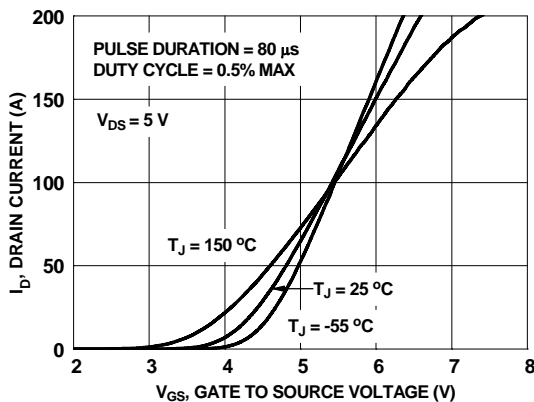


Figure 5. Transfer Characteristics

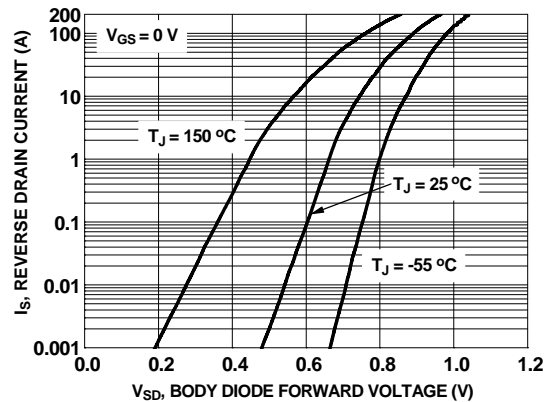


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

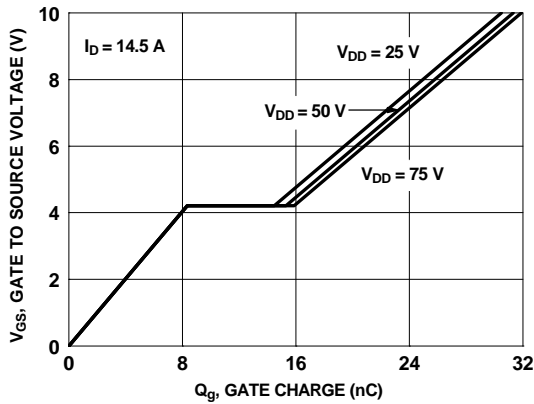


Figure 7. Gate Charge Characteristics

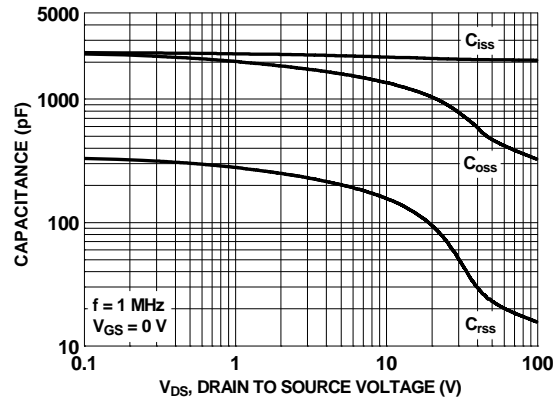


Figure 8. Capacitance vs Drain to Source Voltage

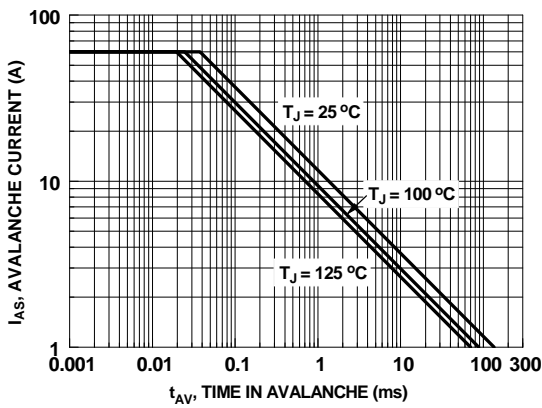


Figure 9. Unclamped Inductive Switching Capability

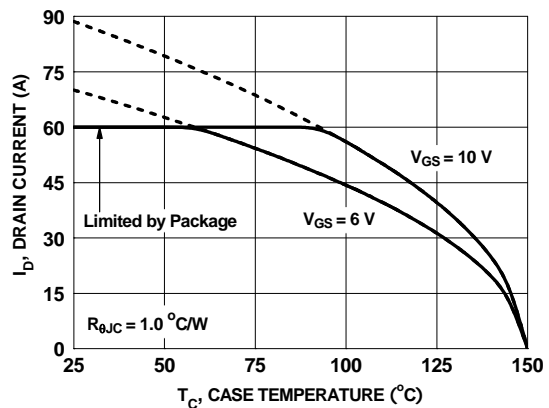


Figure 10. Maximum Continuous Drain Current vs Case Temperature

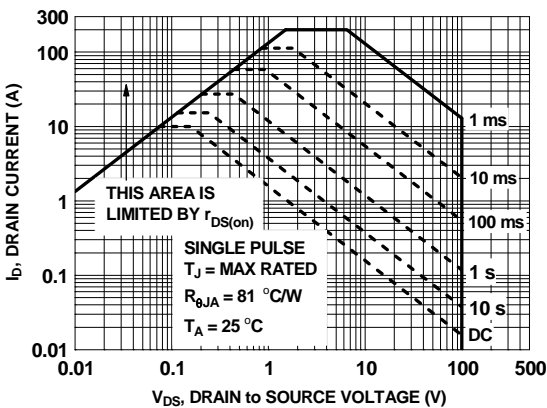


Figure 11. Forward Bias Safe Operating Area

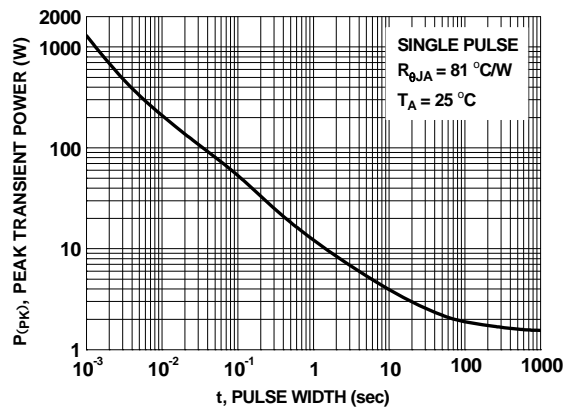


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

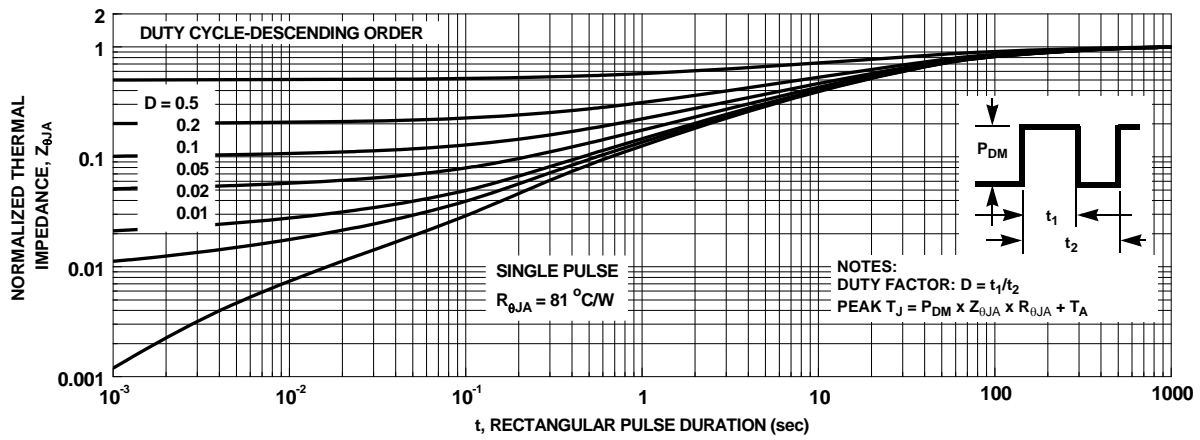
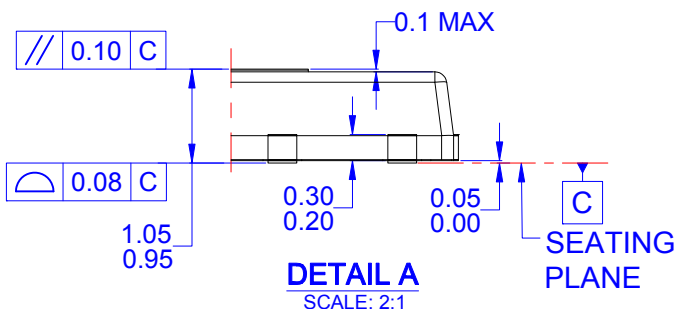
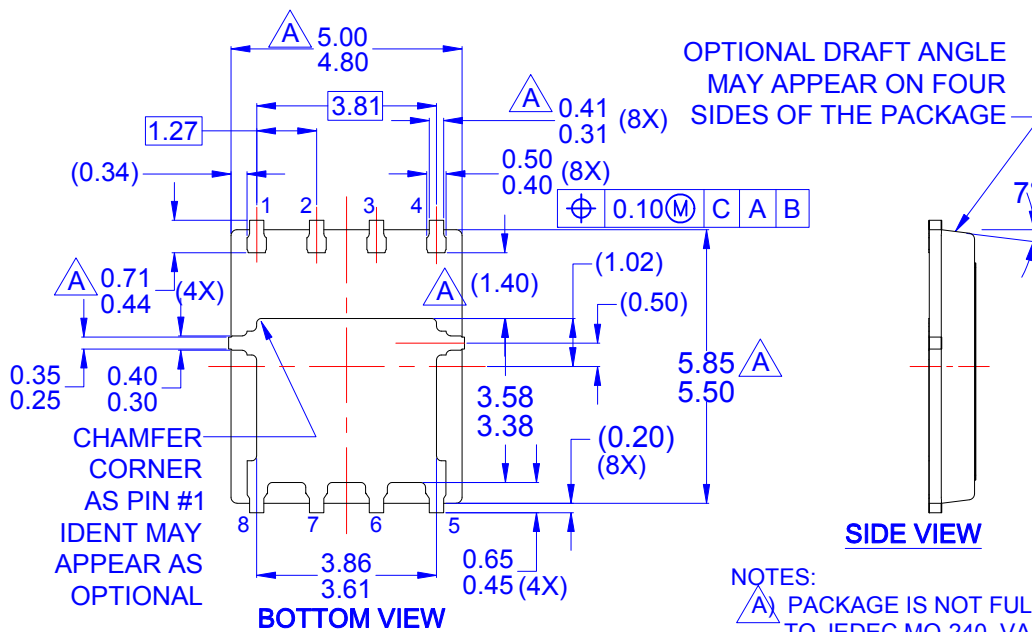
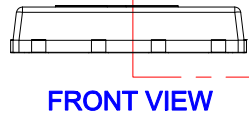
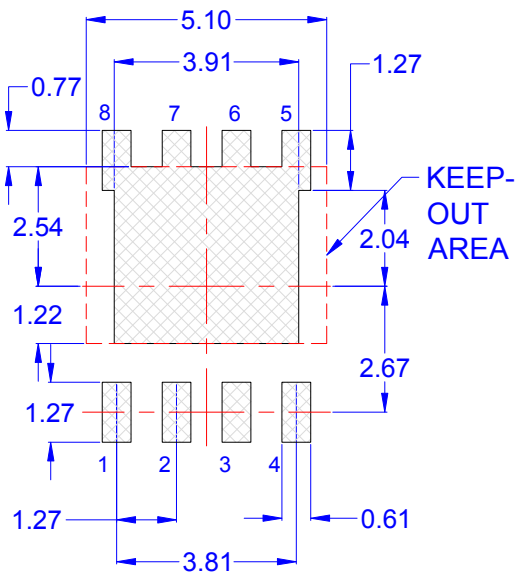
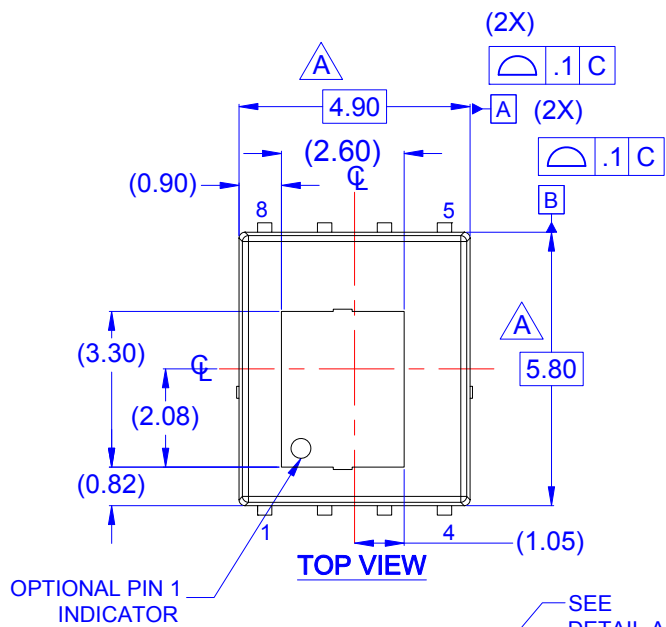


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



- NOTES:
- A) PACKAGE IS NOT FULLY COMPLIANT TO JEDEC MO-240, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
 - F) DRAWING FILE NAME: PQFN08DREV4





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Rev. I77