

FCP190N60 / FCPF190N60

N-Channel SuperFET® II MOSFET

600 V, 20.2 A, 199 mΩ

Features

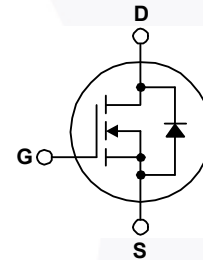
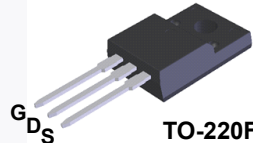
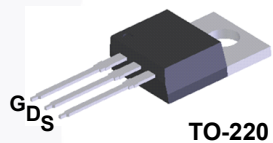
- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 170\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 57\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 160\text{ pF}$)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- LCD / LED / PDP TV Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCP190N60	FCPF190N60	Unit	
V_{DSS}	Drain to Source Voltage	600		V	
V_{GSS}	Gate to Source Voltage	- DC	± 20	V	
		- AC ($f > 1\text{ Hz}$)	± 30		
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	20.2	20.2*	A
		- Continuous ($T_C = 100^\circ\text{C}$)	12.7	12.7*	
I_{DM}	Drain Current	- Pulsed (Note 1)	60.6	60.6*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	400		mJ	
I_{AR}	Avalanche Current (Note 1)	4.0		A	
E_{AR}	Repetitive Avalanche Energy (Note 1)	2.1		mJ	
dv/dt	MOSFET dv/dt	100		V/ns	
	Peak Diode Recovery dv/dt (Note 3)	20			
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	208	39	W
		- Derate Above 25°C	1.67	0.31	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$	
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$	

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FCP190N60	FCPF190N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.6	3.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP190N60	FCP190N60	TO-220	Tube	N/A	N/A	50 units
FCPF190N60	FCPF190N60	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C	-	0.67	-	$\text{V}/^\circ\text{C}$
BV_{DS}	Drain to Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 20\text{ A}$	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	1.3	-	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	0.17	0.199	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 10\text{ A}$	-	21	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	-	2220	2950	pF
C_{oss}	Output Capacitance		-	1630	2165	
C_{rss}	Reverse Transfer Capacitance		-	85	128	
C_{oss}	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	42	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	160	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 10\text{ A},$ $V_{GS} = 10\text{ V}$	-	57	74	nC
Q_{gs}	Gate to Source Gate Charge		-	9	-	
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	21	
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	1	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 10\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 4.7\ \Omega$	-	20	50	ns
t_r	Turn-On Rise Time		-	10	30	
$t_{d(off)}$	Turn-Off Delay Time		-	64	138	
t_f	Turn-Off Fall Time		(Note 4)	-	5	

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	20.2	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	60.6	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 10\text{ A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 10\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	320	-	ns
Q_{rr}	Reverse Recovery Charge		-	5.1	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 4\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 10\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

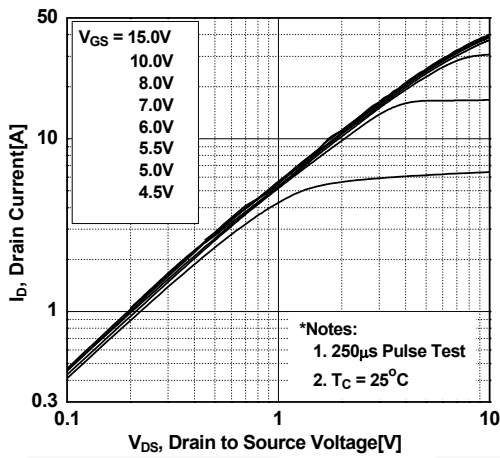


Figure 2. Transfer Characteristics

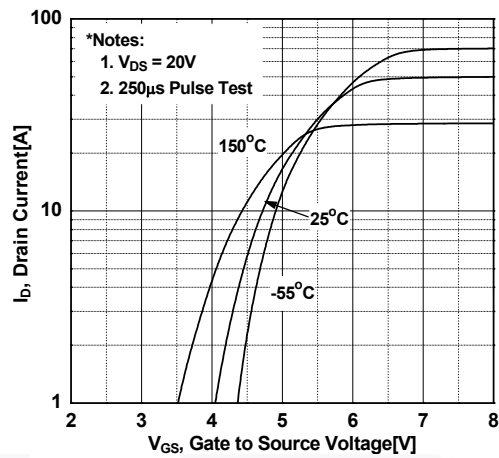


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

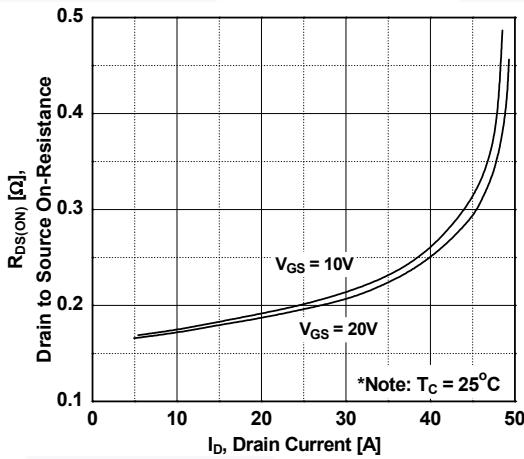


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

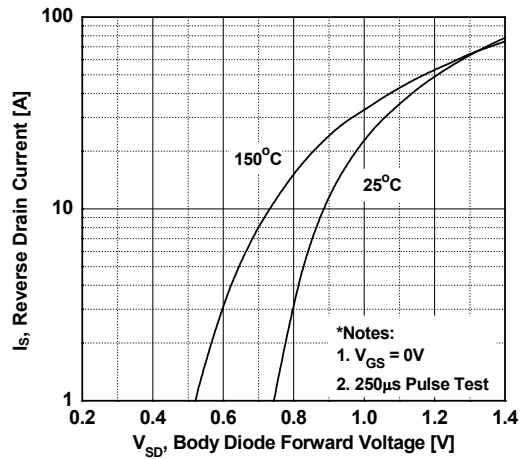


Figure 5. Capacitance Characteristics

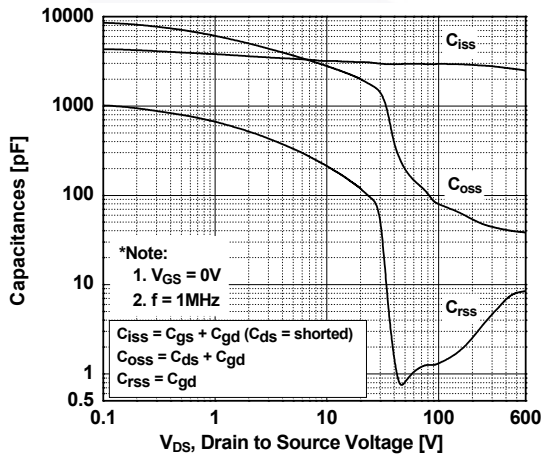
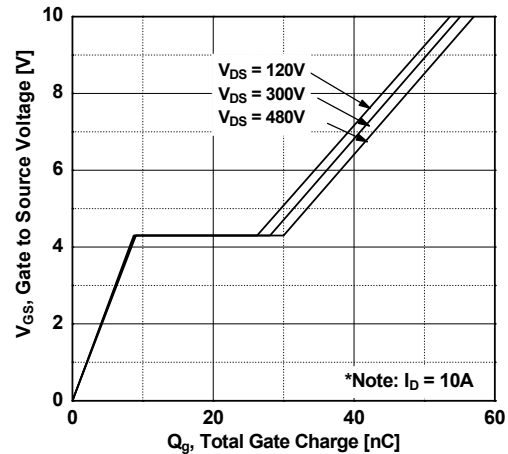


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

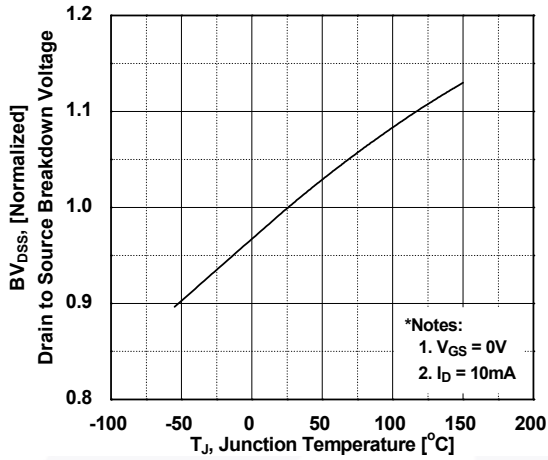


Figure 8. On-Resistance Variation vs. Temperature

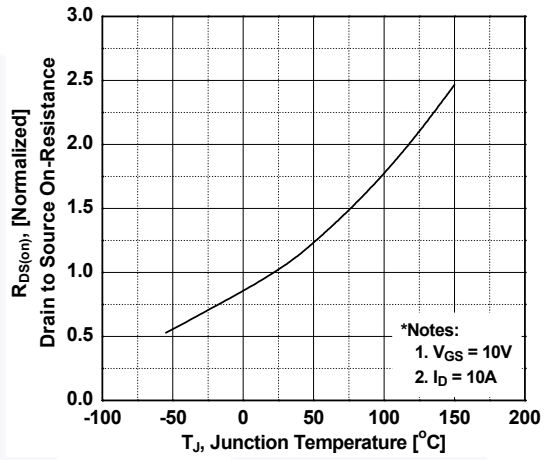


Figure 9. Maximum Safe Operating Area for FCP190N60

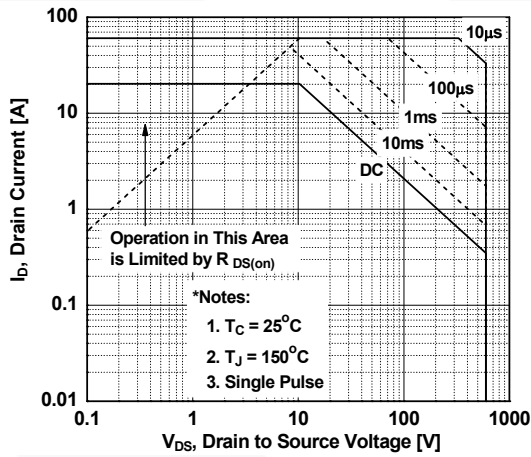


Figure 10. Maximum Safe Operating Area for FCPF190N60

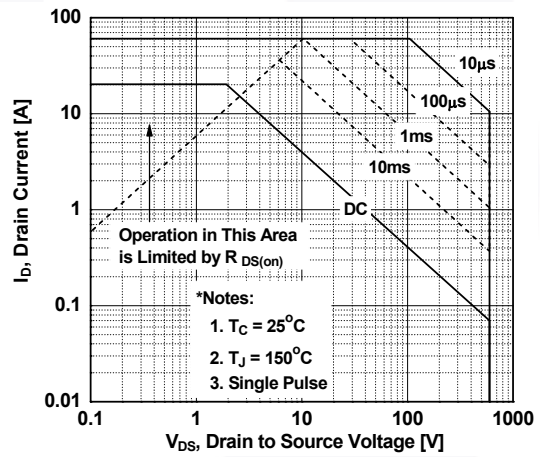


Figure 11. Maximum Drain Current vs. Case Temperature

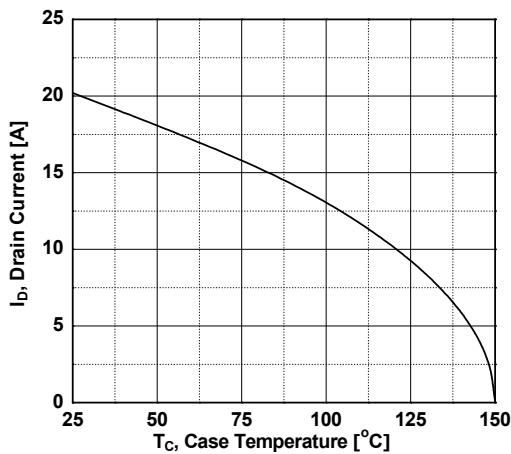
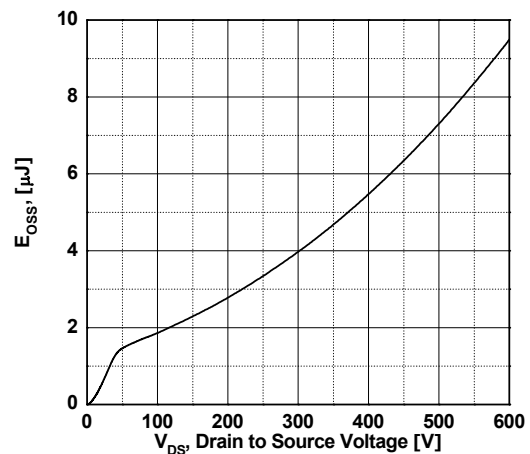


Figure 12. E_oss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve for FCP190N60

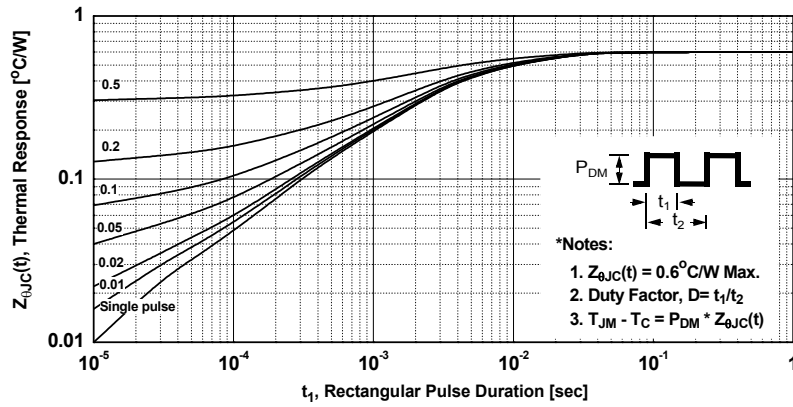


Figure 14. Transient Thermal Response Curve for FCPF190N60

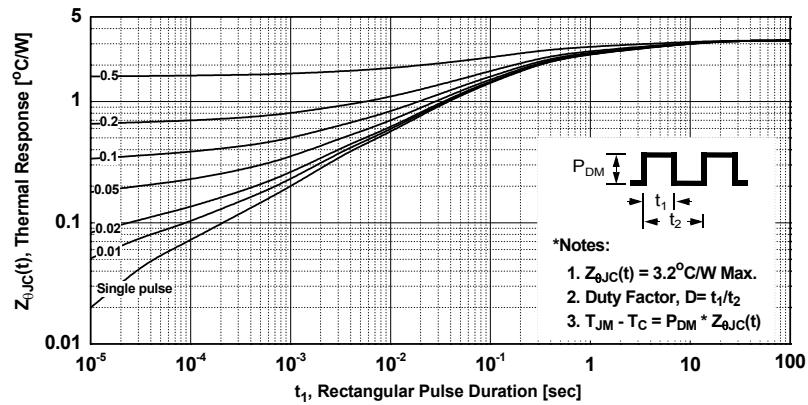




Figure 15. Gate Charge Test Circuit & Waveform



Figure 16. Resistive Switching Test Circuit & Waveforms



Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

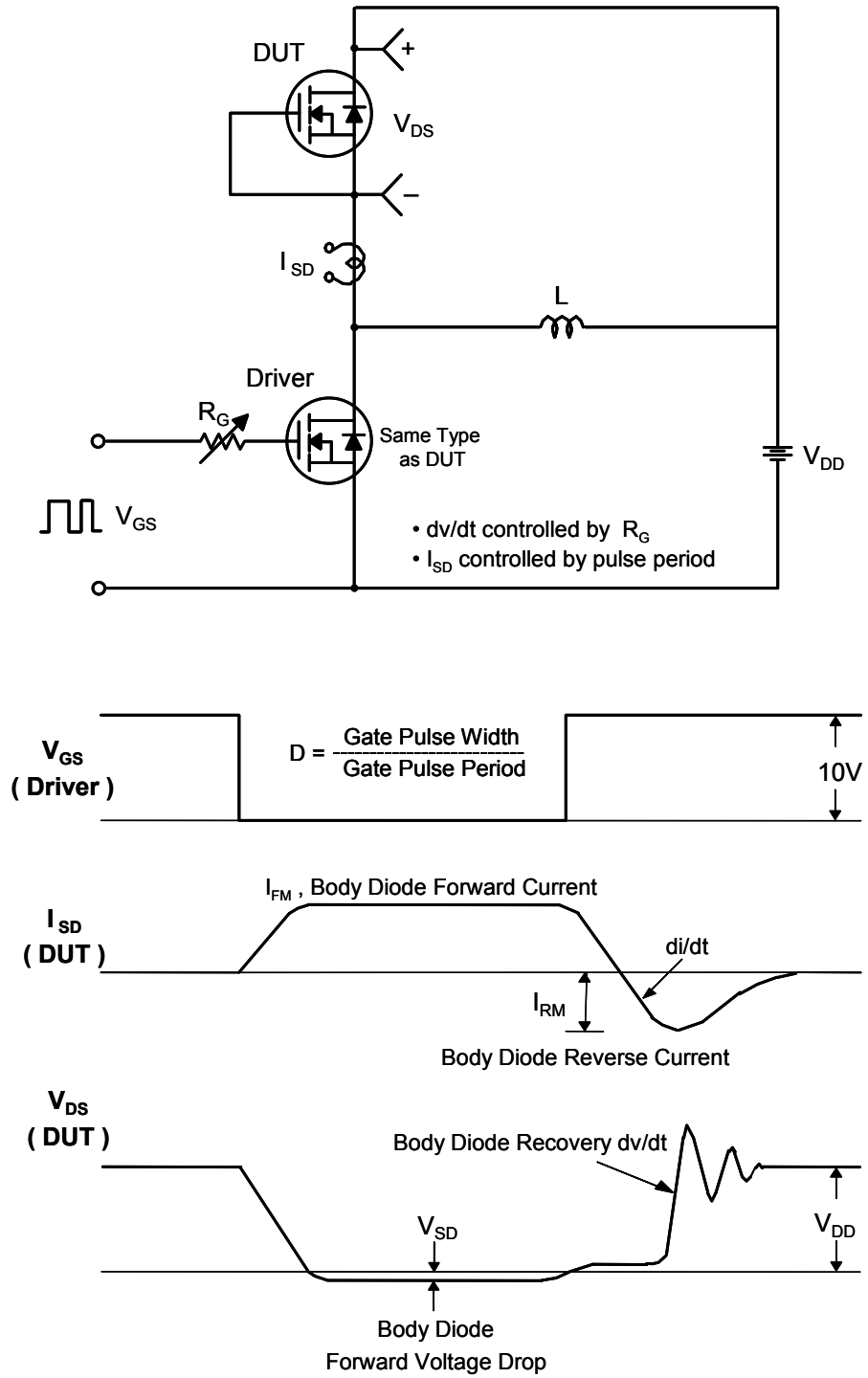
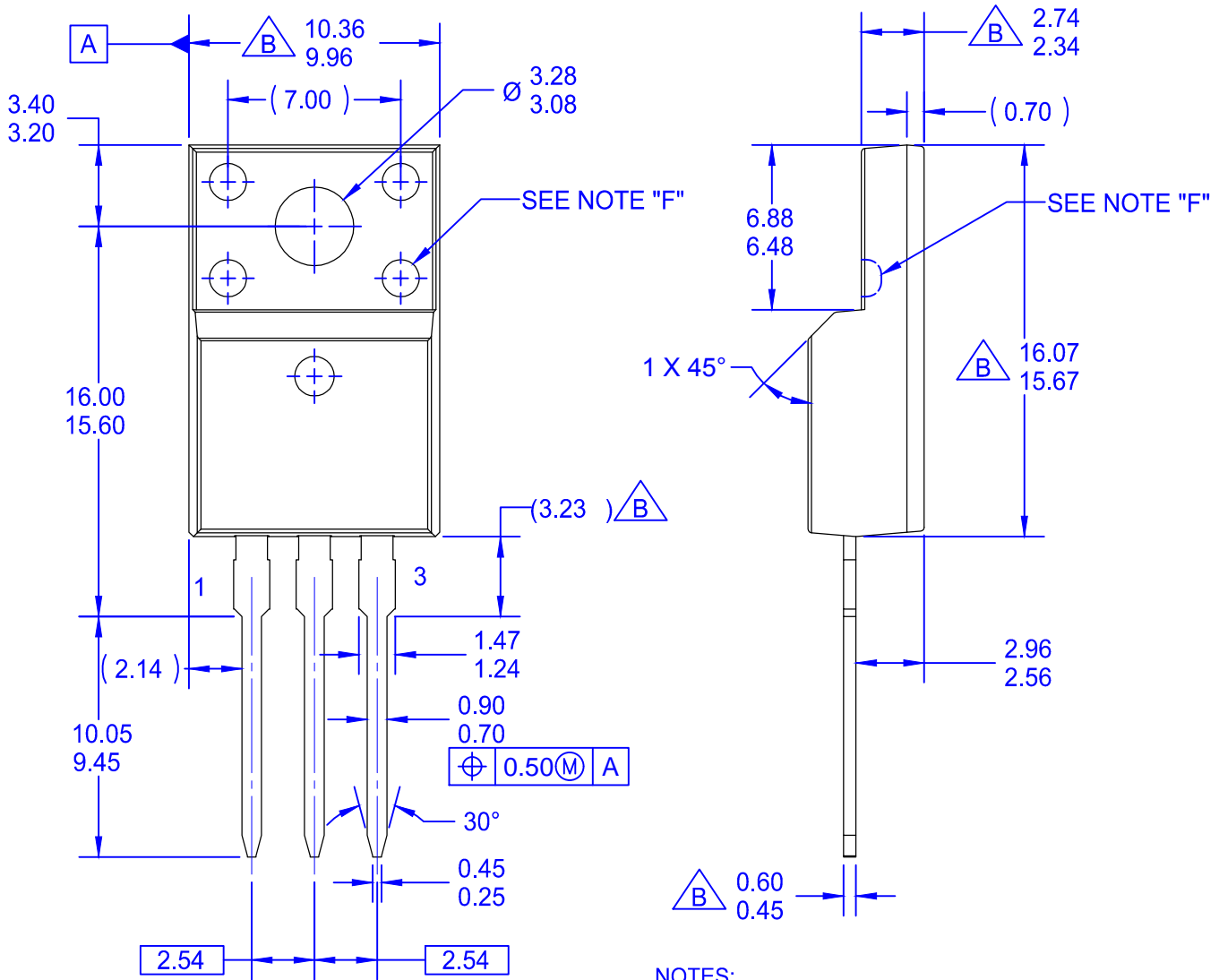


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms



- NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
 - D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
 - E) DOES NOT COMPLY JEDEC STANDARD VALUE.
 - F) "A1" DIMENSIONS AS BELOW:
 SINGLE GAUGE = 0.51 - 0.61
 DUAL GAUGE = 1.10 - 1.45
 - G) DRAWING FILE NAME: TO220B03REV9
 - H) PRESENCE IS SUPPLIER DEPENDENT
 - I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV4



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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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