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October 1987
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MM74C93 4-Bit Binary Counter

General Description

The MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R₀₁ and R₀₂, and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

All inputs are protected against static discharge damage.

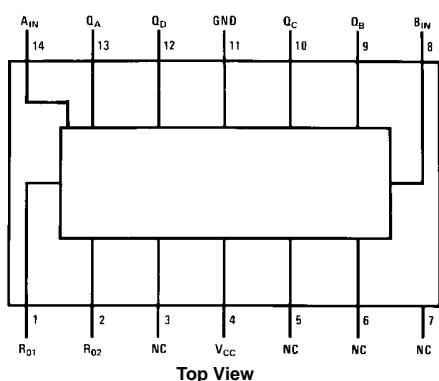
Features

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power compatibility:
Fan out of 2 TTL driving 74L
- The MM74C93 follows the MM74L93 Pinout

Ordering Code:

Order Number	Package Number	Package Description
MM74C93N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

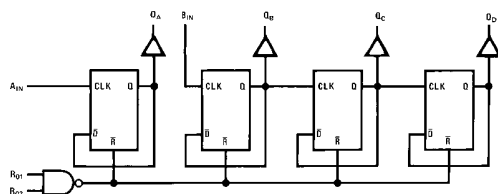


Truth Table

4-Bit Binary Counter Binary Count Sequence

Count	Output			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Logic Diagram



Output Q_A is connected to input B for binary count sequence.
 H = HIGH Level
 L = LOW Level
 X = Irrelevant

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Function Tables

Reset/Count Function Table

Reset Inputs				Output			
R ₀₁	R ₀₂	R ₉₁	R ₉₂	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

Reset/Count Function Table

Reset Inputs		Output			
R ₀₁	R ₀₂	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

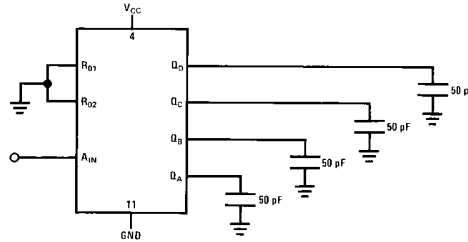
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Absolute Maximum Ratings (Note 1)						
Voltage at Any Pin (Note 1)		-0.3V to $V_{CC} + 0.3V$				
Operating Temperature Range (T_A)		-55°C to +125°C				
Power Dissipation (P_D)						
Dual-In-Line		700 mW				
Small Outline		500 mW				
Operating V_{CC} Range		3V to 15V				
Absolute Maximum V_{CC}		18V				
Storage Temperature Range (T_S)		-65°C to +150°C				
Lead Temperature (T_L)						
(Soldering, 10 seconds)		260°C				
<p>Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.</p>						
DC Electrical Characteristics						
Min/Max limits apply across temperature range unless otherwise noted						
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = +10 \mu A$ $V_{CC} = 10V, I_O = +10 \mu A$			0.5 1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage MM74C90, MM74C93	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage MM74C90, MM74C93	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage MM74C90, MM74C93	$V_{CC} = 4.75V, I_O = -360 \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage MM74C90, MM74C93	$V_{CC} = 4.75V, I_O = -360 \mu A$			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	8.0	16		mA

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AC Electrical Characteristics (Note 2)						
T _A = 25°C, C _L = 50 pF, unless otherwise specified						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{pd0} , t _{pd1}	Propagation Delay Time from A _{1N} to Q _A	V _{CC} = 5V V _{CC} = 10V		200 80	400 150	ns
t _{pd0} , t _{pd1}	Propagation Delay Time from A _{1N} to Q _B (MM74C93)	V _{CC} = 5V V _{CC} = 10V		450 160	850 300	ns
t _{pd0} , t _{pd1}	Propagation Delay Time from A _{1N} to Q _B (MM74C90)	V _{CC} = 5V V _{CC} = 10V		450 160	800 300	ns
t _{pd0} , t _{pd1}	Propagation Delay Time from A _{1N} to Q _C (MM74C93)	V _{CC} = 5V V _{CC} = 10V		500 200	1050 400	ns
t _{pd0} , t _{pd1}	Propagation Delay Time from A _{1N} to Q _C (MM74C93)	V _{CC} = 5V V _{CC} = 10V		500 200	1000 400	ns
t _{pd0} , t _{pd1}	Propagation Delay Time from A _{1N} to Q _D (MM74C93)	V _{CC} = 5V V _{CC} = 10V		600 250	1200 500	ns
t _{pd0} , t _{pd1}	Propagation Delay Time from A _{1N} to Q _D (MM74C90)	V _{CC} = 5V V _{CC} = 10V		450 160	800 300	ns
t _{pd0} , t _{pd1}	Propagation Delay Time from R ₀₁ or R ₀₂ to Q _A , Q _B , Q _C or Q _D (MM74C93)	V _{CC} = 5V V _{CC} = 10V		150 75	300 150	ns
t _{pd0} , t _{pd1}	Propagation Delay Time from R ₀₁ or R ₀₂ to Q _A , Q _B , Q _C or Q _D (MM74C90)	V _{CC} = 5V V _{CC} = 10V		200 75	400 150	ns
t _{pd0} , t _{pd1}	Propagation Delay Time from R ₉₁ or R ₉₂ to Q _A or Q _D (MM74C90)	V _{CC} = 5V V _{CC} = 10V		250 100	500 200	ns
t _{PW}	Min. R ₀₁ or R ₀₂ Pulse Width (MM74C93)	V _{CC} = 5V V _{CC} = 10V	600 30	250 125		ns
t _{PW}	Min. R ₀₁ or R ₀₂ Pulse Width (MM74C90)	V _{CC} = 5V V _{CC} = 10V	600 300	250 125		ns
t _{PW}	Min. R ₉₁ or R ₉₂ Pulse Width (MM74C90)	V _{CC} = 5V V _{CC} = 10V	500 250	200 100		ns
t _r , t _f	Maximum Clock Rise and Fall Time	V _{CC} = 10V V _{CC} = 10V			15 5	μs
t _W	Minimum Clock Pulse Width	V _{CC} = 5V V _{CC} = 10V	250 100	100 50		ns
f _{MAX}	Maximum Clock Frequency	V _{CC} = 5V V _{CC} = 10V	2 5			MHz
C _{IN}	Input Capacitance	Any Input (Note 3)		5		pF
C _{PD}	Power Dissipation Capacitance	Per Package (Note 4)		45		pF

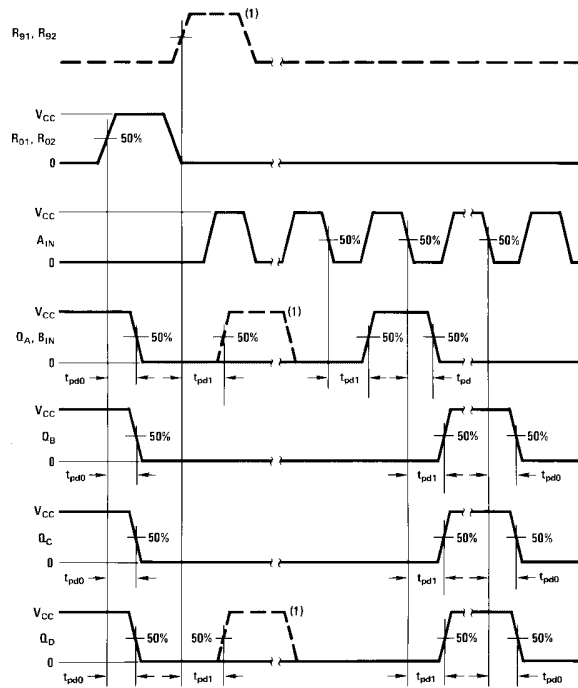
Note 2: AC Parameters are guaranteed by DC correlated testing.
Note 3: Capacitance is guaranteed by periodic testing.
Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see Family Characteristics application note—AN-90.

AC Test Circuits



Clock rise and fall time $t_r = t_f = 20$ ns

Switching Time Waveforms



MM74C90 and MM74C93 are solid line waveforms. Dashed line waveforms are for MM74C90 only.

MM74C93 4-Bit Binary Counter

Physical Dimensions inches (millimeters) unless otherwise noted

**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
 Package Number N14A**

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