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CVM5XXM User's Guide

2/21/00

The CVM5XXM Member module emulates the 14-pin PIC16C505 and the 8-pin PIC12C508, PIC12C509, PIC12CE518, and PIC12CE519 micro-controllers. These devices are part of the 12 bit PICmicro family and therefore requires the 5X FAMILY module (CVM5XF) for operation. The PIC12CE518 and PIC12CE519 devices have EEPROM support.

EMULATOR DISCREPENCIES:

Due to BONDOUT limitations, the following features are either NOT SUPPORTED or are modified slightly:

- The Wake-Up on pin change feature is not supported. The GPWU bit (OPTION.7) has no affect. And the corresponding flag GPWUF (STATUS.7) has no meaning.
- The "weak pull-up" resistors are enabled/disabled by hardware jumpers on the member pod rather than through the GPPU bit (OPTION.6). This bit has no affect.
- Mathias provides the operating clock so the OSCCAL register has no affect. You can program Mathias for any clock frequency between 30KHz and 20MHz. The real PIC devices run at around 4 MHz from their internal oscillator.
- GP3 is an INPUT ONLY on the real device to accommodate that pin's alternative use as MCLR. The emulator provides a full INPUT/OUTPUT pin for this function. The MCLR signal is brought into the bondout chip through a different connection. You should ALWAYS SET the corresponding TRIS bit for GP3 to properly emulate this INPUT-ONLY behavior.
- In an actual device, setting the TOCS bit (OPTION.5) automatically forces GP2 to be an input, over-riding the TRIS bit for GP2. The emulator DOES NOT automatically force GP2 to be an input. YOU MUST SET TRIS.2 YOURSELF, if you use GP2 as a T0CS input.
- In an actual device, GPIO bits 6 and 7 are not implemented and will always read back '0'. In the emulator, these bits are actually present and will read back whatever was last written to them if the corresponding TRIS bits are cleared. If these TRIS bits are SET, then these bits read FLOATING inputs and their value is indeterminate.
- EEPROM support for PIC12CE518 and PIC12CE519 devices are available on RA0 for SDA (versus GPIO reg, bit 6 on an actual device) and RA1 for SCL (versus GPIO reg, bit 7 on an actual device)

EMULATOR CABLES:



Attach the cable for 8-pin devices to JP8. The cable for 14-pin devices should be attached to JP13.

JUMPER CONFIGURATIONS:



JP4: POWER

If the target permits, you can power the target from the emulator. To do so, place a jumper on JP4 between the center pin (+5EMU) and the pin marked +5VEXT. Moving the jumper the unmarked position isolates the power rails. The default position is to ISOLATE the power rails.



JP5 & JP15: Pin 5 function (both jumpers should be in the same position)

functions as GP2. (default)		functions as T0CKI	
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JP12*: Selects Pin 2 function




functions as GP5. (default)		No connection.*	
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JP9*: Select Pin 3 function

functions as GP4. (default)		No Connection*	
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* Since Mathias provides the clock for the bondout chip, JP12 and JP9 are usually set to the GP position or removed completely. The no connection position is appropriate when your target normally drives the OSC pins. This isolates the GP bits so that they are not in contention with your target. NOTE: In either configuration, Mathias provides its own programmable clock, making it easy to emulate a processor in either internal or external clock source mode.

JP6: Selects Pin 4 function

<p>functions as GP2 with the bondout MCLR tied to a weak pull to Mathias VCC. (default)</p> 	<p>BONDOUT MCLR driven by Pin 4 with a weak pullup to Mathias VCC.</p> 
<p>Functions as GP2 with the bondout MCLR tied to the TARGET VCC.</p> 	<p>(the configuration to the left can cause random resets if the target cable is not attached to a target and JP1 is NOT strapped to power the target. It is not normally used.)</p>

JP7, JP10, JP11, JP14 Weak Pull-ups

On the real devices, these three pull-ups are ALL ON or ALL OFF. To properly emulate this, you should set ALL three jumpers to the ON position to enable the weak pull-ups. Conversely, you should set ALL THREE jumpers to the OFF position to disable the weak pull-ups. These are set to the ON position by default.