

# **Excellent Integrated System Limited**

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Fairchild Semiconductor DM74LS90N

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August 1986 Revised March 2000

# DM74LS90 Decade and Binary Counters

#### **General Description**

Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-five for the DM74LS90.

All of these counters have a gated zero reset and the DM74LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four bit binary), the B input is connected to the  $Q_A$  output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the DM74LS90 counters by connecting the  $Q_D$  output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output  $Q_A$ .

#### **Features**

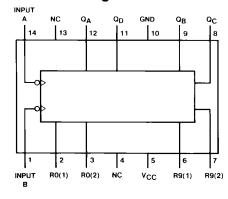
- Typical power dissipation 45 mW
- Count frequency 42 MHz

#### **Ordering Code:**

Order Number	Package Number	Package Description
DM74LS90M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS90N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### **Connection Diagram**



#### **Reset/Count Truth Table**

	Reset Inputs				Out	put		
R0(1)	R0(2)	R9(1)	R9(2)	$Q_D$	Q <sub>C</sub>	QB	$Q_A$	
Н	Н	L	Х	L	L	L	L	
Н	Н	Χ	L	L	L	L	L	
Х	Χ	Н	Н	Н	L	L	Н	
Х	L	Χ	L	COUNT				
L	Χ	L	Χ	COUNT				
L	X	X	L	COUNT				
Х	L	L	Χ	COUNT				

# **JM74LS9**(

#### **Function Tables**

## BCD Count Sequence (Note 1)

Count		Out	tput	
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	Н
2	L	L	Н	L
3	L	L	Н	Н
4	L	Н	L	L
5	L	Н	L	Н
6	L	Н	Н	L
7	L	Н	Н	Н
8	Н	L	L	L
9	Н	L	L	Н

#### **Bi-Quinary (5-2)** (Note 2)

Count		Out	tput	
	$Q_A$	$Q_D$	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	Н
2	L	L	Н	L
3	L	L	Н	Н
4	L	Н	L	L
5	Н	L	L	L
6	Н	L	L	Н
7	Н	L	Н	L
8	Н	L	Н	Н
9	Н	Н	L	L

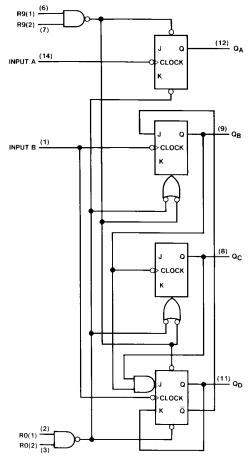
H = HIGH Level L = LOW Level X = Don't Care

Note 1: Output  $\mathbf{Q}_{\mathbf{A}}$  is connected to input B for BCD count.

Note 2: Output  $\mathbf{Q}_{\mathbf{D}}$  is connected to input A for bi-quinary count.

Note 3: Output Q<sub>A</sub> is connected to input B.

### **Logic Diagram**



The J and K inputs shown without connection are for reference only and are functionally at a high level.



#### **Absolute Maximum Ratings**(Note 4)

Supply Voltage Input Voltage (Reset) Input Voltage (A or B) Operating Free Air Temperature Range Storage Temperature Range

7V
7V
5.5V
0°C to +70°C
-65°C to +150°C

Note 4: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

#### **Recommended Operating Conditions**

Symbol	Parameter	1	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage		4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage		2			V
V <sub>IL</sub>	LOW Level Input Voltage				0.8	V
I <sub>OH</sub>	HIGH Level Output Current				-0.4	mA
I <sub>OL</sub>	LOW Level Output Current				8	mA
f <sub>CLK</sub>	Clock Frequency (Note 5)	A to Q <sub>A</sub>	0		32	MHz
		B to Q <sub>B</sub>	0		16	
f <sub>CLK</sub>	Clock Frequency (Note 6)	A to Q <sub>A</sub>	0		20	MHz
		B to Q <sub>B</sub>	0		10	
t <sub>W</sub>	Pulse Width (Note 5)	А	15			
		В	30			ns
		Reset	15			
t <sub>W</sub>	Pulse Width (Note 6)	А	25			
		В	50			ns
		Reset	25			
t <sub>REL</sub>	Reset Release Time (Note 5)		25			ns
t <sub>REL</sub>	Reset Release Time (Note 6)		35			ns
T <sub>A</sub>	Free Air Operating Temperatur	е	0		70	°C

**Note 5:**  $C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, T_A = 25^{\circ}\text{C} \text{ and } V_{CC} = 5\text{V}.$ Note 6:  $C_L=50$  pF,  $R_L=2$   $k\Omega,\,T_A=25^{\circ}C$  and  $V_{CC}=5V.$ 

#### **Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Condition	s	Min	Typ (Note 7)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V <sub>OH</sub>	HIGH Level	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max		2.7	3.4		V
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$		2.1	3.4		V
V <sub>OL</sub>	LOW Level	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max	(Note 8)				
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$	(Note 6)		0.35	0.5	V
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min			0.25	0.4	
II	Input Current @ Max	$V_{CC} = Max, V_I = 7V$	Reset			0.1	
	Input Voltage	V <sub>CC</sub> = Max	Α			0.2	mA
		$V_I = 5.5V$	В			0.4	
I <sub>IH</sub>	HIGH Level	$V_{CC} = Max, V_I = 2.7V$	Reset			20	
	Input Current		Α			40	μΑ
			В			80	1
I <sub>IL</sub>	LOW Level	$V_{CC} = Max, V_I = 0.4V$	Reset			-0.4	
	Input Current		Α			-2.4	mA
			В			-3.2	
Ios	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 9)	•	-20		-100	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 7)			9	15	mA
Note 7: All t	voicals are at Voc = 5V T <sub>*</sub> = 25°C	1			1		1

Note 7: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

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# **DM74LS90**

### **Electrical Characteristics** (Continued)

Note 8:  $Q_A$  outputs are tested at  $I_{OL} = Max$  plus the limit value of  $I_{IL}$  for the B input. This permits driving the B input while maintaining full fan-out capability. Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

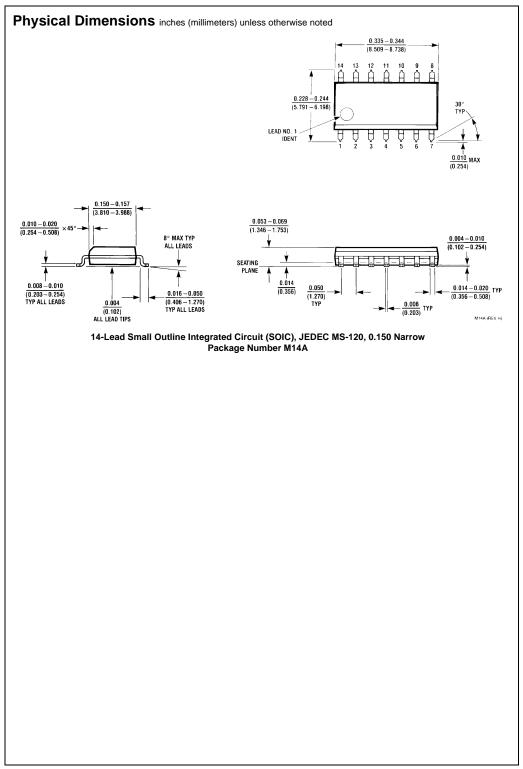
Note 10: I<sub>CC</sub> is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

### Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$

	Parameter	From (Input)	$R_L = 2 k\Omega$				
Symbol		To (Output)	C <sub>L</sub> = 15 pF		C <sub>L</sub> = 50 pF		Units
			Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock	A to Q <sub>A</sub>	32		20		MHz
	Frequency	B to Q <sub>B</sub>	16		10		IVITZ
t <sub>PLH</sub>	Propagation Delay Time	A to Q <sub>A</sub>		16		20	
	LOW-to-HIGH Level Output	A to Q <sub>A</sub>		10		20	ns
t <sub>PHL</sub>	Propagation Delay Time	A to O		18		24	
	HIGH-to-LOW Level Output	A to Q <sub>A</sub>		18		24	ns
t <sub>PLH</sub>	Propagation Delay Time	A += 0		48		50	
	LOW-to-HIGH Level Output	A to Q <sub>D</sub>		48		52	ns
t <sub>PHL</sub>	Propagation Delay Time	A += 0		50			ns
	HIGH-to-LOW Level Output	A to Q <sub>D</sub>		50		60	
t <sub>PLH</sub>	Propagation Delay Time	D to O		16		23	
	LOW-to-HIGH Level Output	B to Q <sub>B</sub>		10		23	ns
t <sub>PHL</sub>	Propagation Delay Time	B to O		21		30	ns
	HIGH-to-LOW Level Output	B to Q <sub>B</sub>		21		30	
t <sub>PLH</sub>	Propagation Delay Time	B to Q <sub>C</sub>		32		37	ns
	LOW-to-HIGH Level Output	B to QC		32		31	115
t <sub>PHL</sub>	Propagation Delay Time	B to Q <sub>C</sub>		35		44	ns
	HIGH-to-LOW Level Output	D 10 QC		33		44	115
t <sub>PLH</sub>	Propagation Delay Time	B to Q <sub>D</sub>		32		36	ns
	LOW-to-HIGH Level Output	B to QD		32		30	115
t <sub>PHL</sub>	Propagation Delay Time	B to Q <sub>D</sub>		35		44	
	HIGH-to-LOW Level Output	B to QD	35		44		ns
t <sub>PLH</sub>	Propagation Delay Time	SET-9 to Q <sub>A</sub> , Q <sub>D</sub>		30		35	ns
	LOW-to-HIGH Level Output	3L 1-3 10 QA, QD		30		33	115
t <sub>PHL</sub>	Propagation Delay Time	SET-9 to Q <sub>B</sub> , Q <sub>C</sub>		40		48	ns
	HIGH-to-LOW Level Output	3⊏1-3 10 ℃B, ℃C		40		40	115
t <sub>PHL</sub>	Propagation Delay Time	SET-0 to Any Q		40		52	ns
	HIGH-to-LOW Level Output	SE 1-U IU AIIY Q		40		32	

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#### **DM74LS90 Decade and Binary Counters** Physical Dimensions inches (millimeters) unless otherwise noted (Continued) (18.80 - 19.56)0.090 14 13 12 11 10 9 8 14 13 12 INDEX AREA $\frac{0.250 \pm 0.010}{(6.350 \pm 0.254)}$ PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX DEPTH OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ $\frac{0.300 - 0.320}{(7.620 - 8.128)}$ $\frac{0.065}{(1.651)}$ $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 4° TYP Optional ¥ $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ 95°±5° (0.508) $\frac{0.125 - 0.150}{(3.175 - 3.810)}$ MIN 0.280 (1.905 ± 0.381) (7.112) MIN 0.014 -0.023 TYP $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ $0.050 \pm 0.010$ (1.270 - 0.254) TYP $0.325 \, {}^{+\, 0.040}_{-\, 0.015}$

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14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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 $\left(8.255 + 1.016 - 0.381\right)$ 

N14A (REV.F)

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