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[DMP4047LFDE-7](#)

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DMP4047LFDE

40V P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)max}$	Package	$I_D max$ $T_A = +25^{\circ}C$
-40V	33mΩ @ $V_{GS} = -10V$	U-DFN2020-6 Type E	-6A
	50mΩ @ $V_{GS} = -4.5V$		-4.9A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- General Purpose Interfacing Switch
- Load Switching
- Battery Management Application
- Power Management Functions

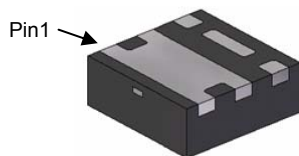
Features

- 0.6mm profile – ideal for low profile applications
- PCB footprint of 4mm²
- Low Gate Threshold Voltage
- Low On-Resistance
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

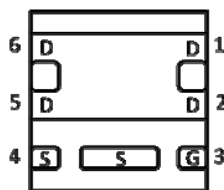
Mechanical Data

- Case: U-DFN2020-6 Type E
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.0065 grams (approximate)

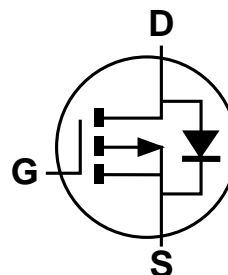
U-DFN2020-6 Type E



Bottom View



Pin Out
Bottom View



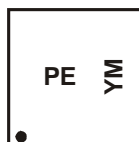
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Marking	Reel size (inches)	Quantity per reel
DMP4047LFDE-7	PE	7	3,000
DMP4047LFDE-13	PE	13	10,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



PE = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: Y = 2011)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-40	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-3.3 -2.6	A
	$t < 5\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-5.3 -4.2	A
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-6.0 -4.8	A
	$t < 5\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-9.5 -7.6	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	-40	A
Maximum Body Diode Continuous Current			I_S	3	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	0.7	W
	$T_A = +70^\circ\text{C}$		0.42	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	180	$^\circ\text{C/W}$
	$t < 5\text{s}$		76	
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	2.1	W
	$T_A = +70^\circ\text{C}$		1.3	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	58	$^\circ\text{C/W}$
	$t < 5\text{s}$		25	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	10.2	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	1	μA	$V_{DS} = -40\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	—	-2.2	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	26	33	m Ω	$V_{GS} = -10\text{V}, I_D = -4.4\text{A}$
			36	50		$V_{GS} = -4.5\text{V}, I_D = -3.7\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	—	5.2	—	S	$V_{DS} = -15\text{V}, I_D = -4.4\text{A}$
Diode Forward Voltage	V_{SD}	—	0.75	1.2	V	$V_{GS} = 0\text{V}, I_S = -3.9\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	1382	—	pF	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	103	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	81	—	pF	
Gate Resistance	R_g	—	7.7	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = -4.5\text{V}$)	Q_g	—	11.2	—	nC	$V_{DS} = -20\text{V}, I_D = -4.9\text{A}$
Total Gate Charge ($V_{GS} = -10\text{V}$)	Q_g	—	23.2	—	nC	
Gate-Source Charge	Q_{gs}	—	3.3	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.9	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	18.4	—	ns	$V_{DS} = -20\text{V}, I_D = -3.9\text{A}$ $V_{GS} = 4.5\text{V}, R_G = 1\Omega$
Turn-On Rise Time	t_r	—	28.2	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	38.8	—	ns	
Turn-Off Fall Time	t_f	—	28.6	—	ns	
Reverse Recovery Time	t_{rr}	—	15.4	—	ns	$I_F = -3.9\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}	—	5.4	—	nC	

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate
 - Short duration pulse test used to minimize self-heating effect
 - Guaranteed by design. Not subject to production testing



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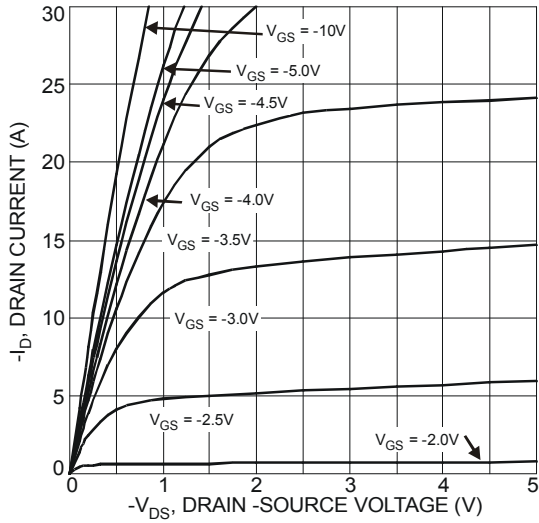


Fig. 1 Typical Output Characteristics

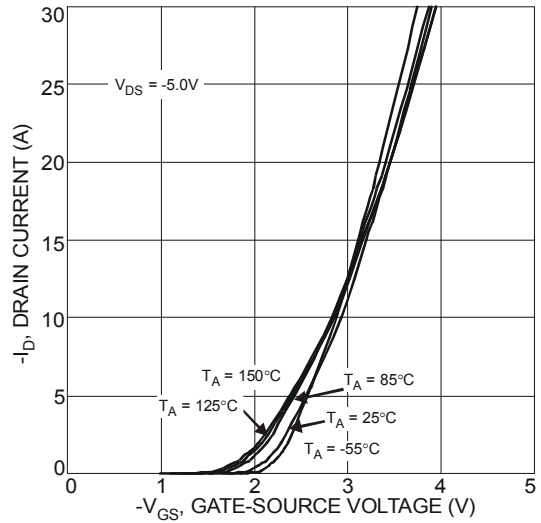


Fig. 2 Typical Transfer Characteristics

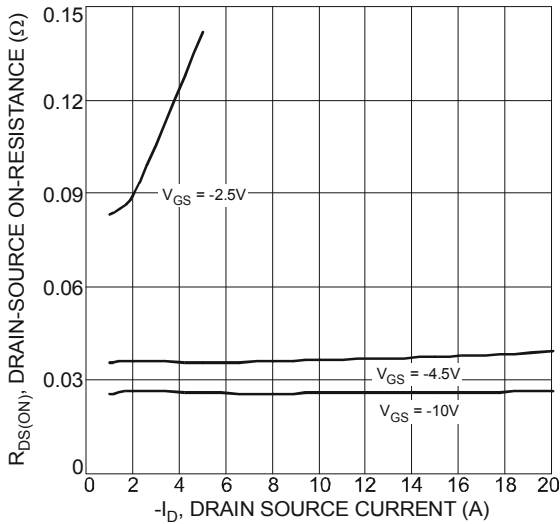


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

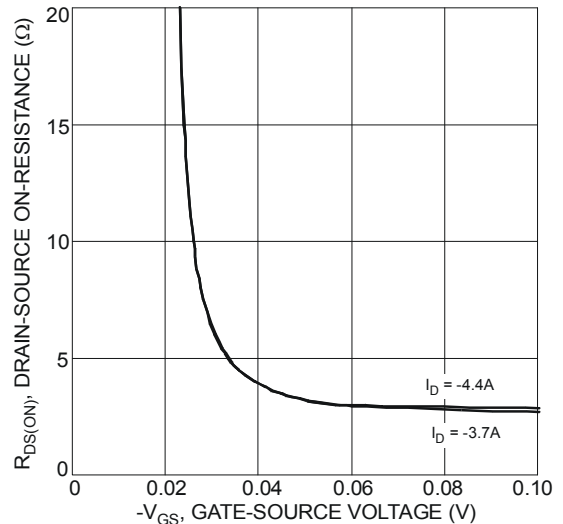


Fig. 4 Typical Drain-Source On-Resistance vs. Gate-Source Voltage

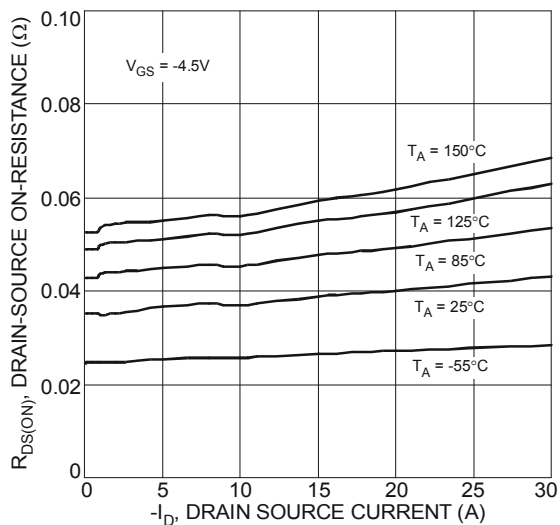


Fig. 5 Typical On-Resistance vs. Drain Current and Temperature

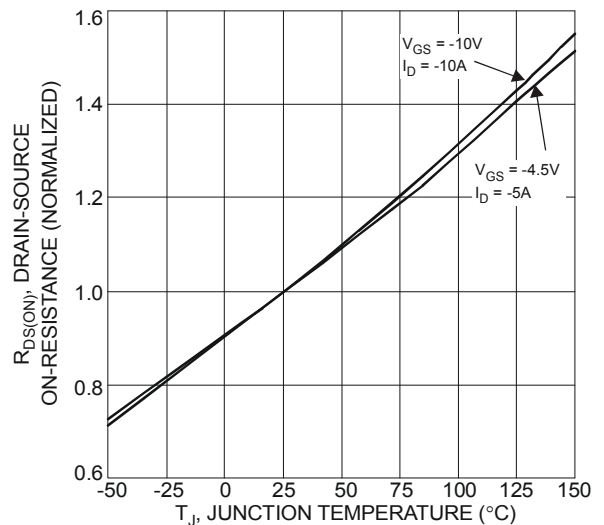


Fig. 6 On-Resistance Variation with Temperature



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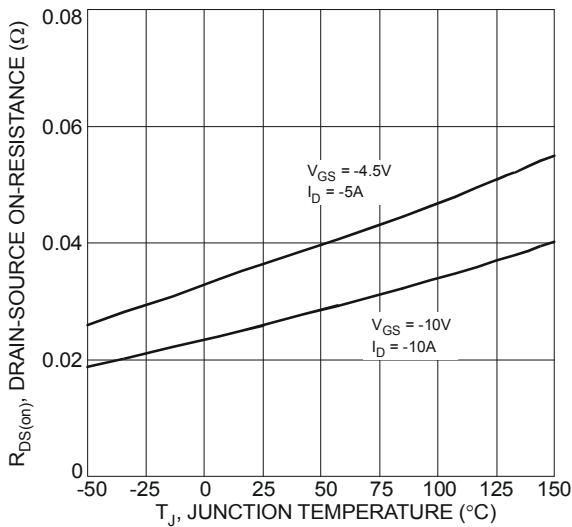


Fig. 7 On-Resistance Variation with Temperature

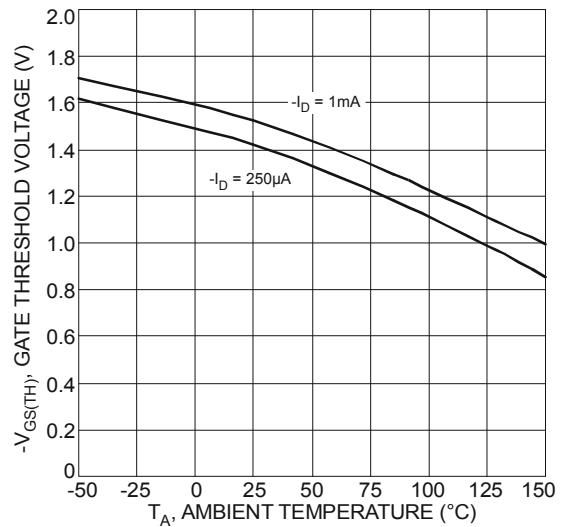


Fig. 8 Gate Threshold Variation vs. Ambient Temperature

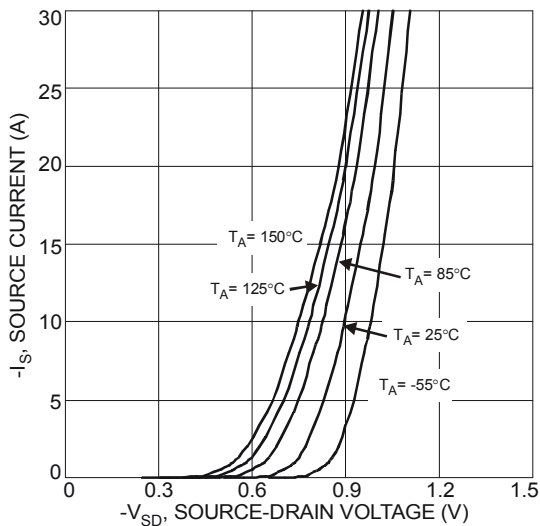


Fig. 9 Diode Forward Voltage vs. Current

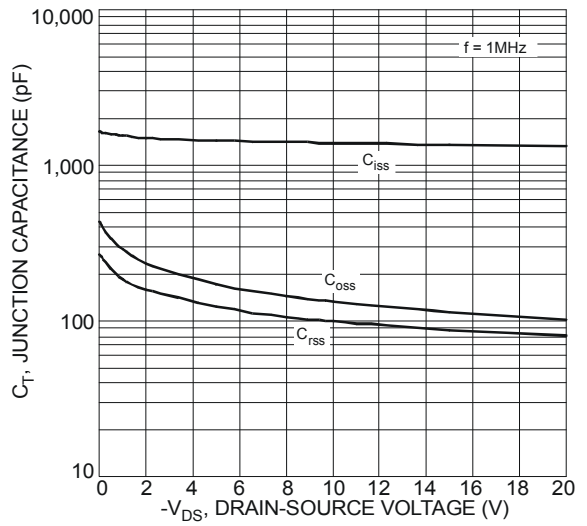


Fig. 10 Typical Junction Capacitance

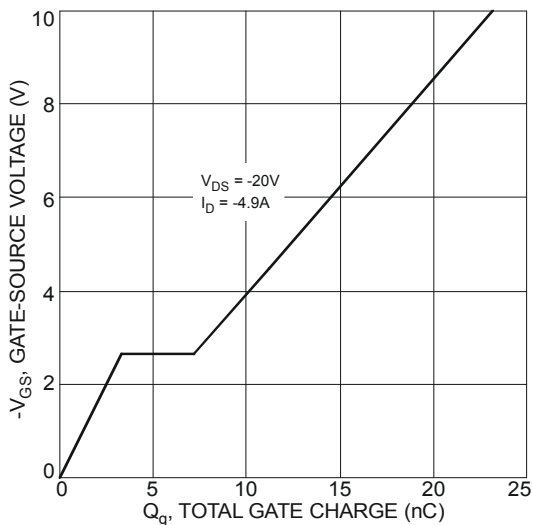


Fig. 11 Gate-Charge Characteristics

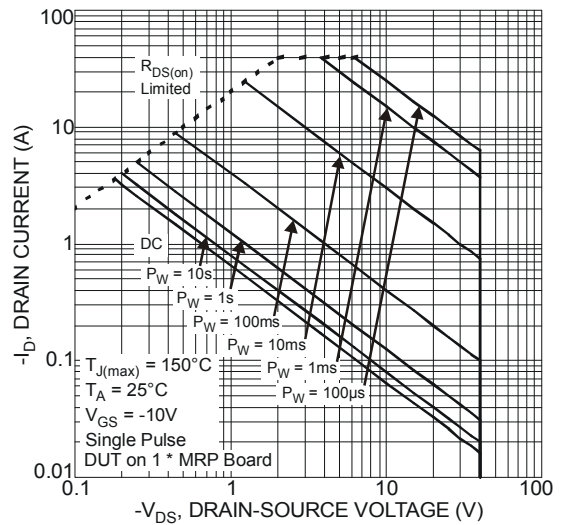
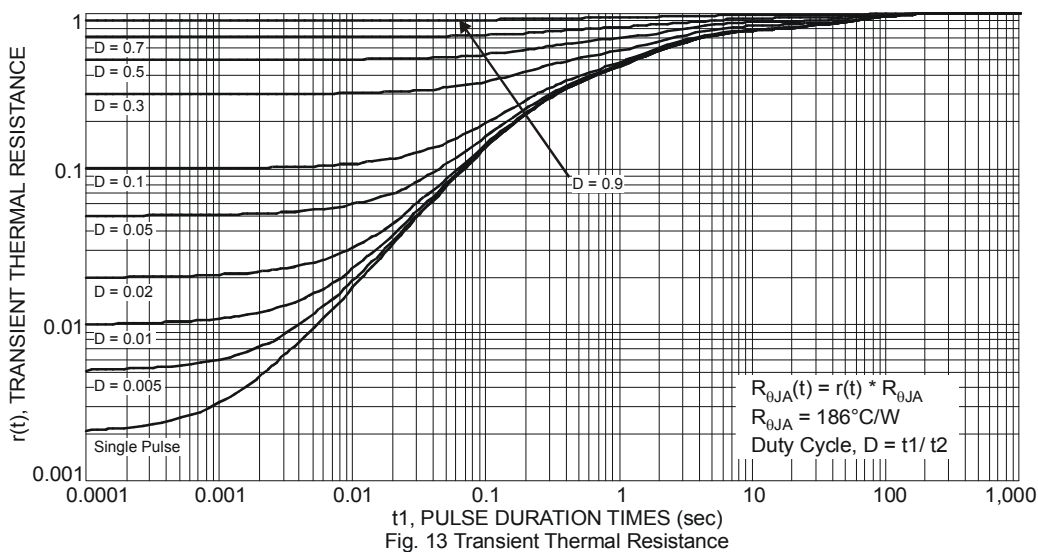


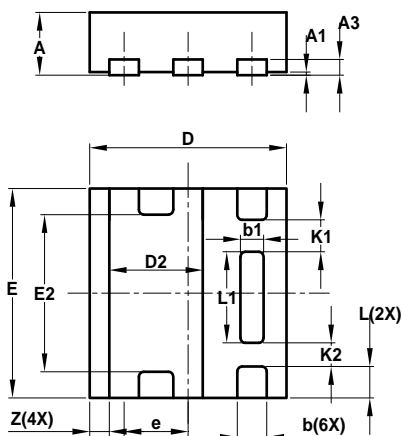
Fig. 12 SOA, Safe Operation Area



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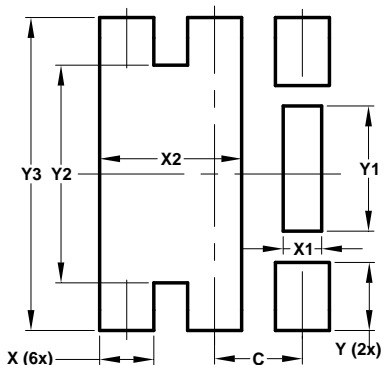
Package Outline Dimensions



U-DFN2020-6 Type E			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	—	—	0.15
b	0.25	0.35	0.30
b1	0.185	0.285	0.235
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
E	1.95	2.05	2.00
E2	1.40	1.60	1.50
e	—	—	0.65
L	0.25	0.35	0.30
L1	0.82	0.92	0.87
K1	—	—	0.305
K2	—	—	0.225
Z	—	—	0.20

All Dimensions in mm

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.285
X2	1.050
Y	0.500
Y1	0.920
Y2	1.600
Y3	2.300

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