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Texas Instruments
BQ294524DRVR

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bq294502, bq294504, bq294512, bq294514
bq294515, bq294522, bq294524, bq294532
bq294562, bq294572, bq294582, bq294592

SLUSAJ3D – SEPTEMBER 2011 – REVISED JULY 2015

bq2945xx Overvoltage Protection For 2-Series and 3-Series Cell Li-Ion Batteries

1 Features

- 2-Series and 3-Series Cell Overvoltage Monitor for Secondary Protection
- Fixed Programmable Delay Timer
- Fixed OVP Threshold
  - Available Range From 3.85 V to 4.6 V
- Fixed OVP Delay Option: 4 s or 6.5 s
- High-Accuracy Overvoltage Protection: ±10 mV
- Low Power Consumption I_{CC} ≈ 1 µA ($V_{CELL(ALL)}$ < $V_{PROTECT}$)
- Low Leakage Current per Cell Input < 100 nA
- Small Package Footprint
  - 6-Pin SON

2 Applications

- Second-Level Protection in Li-Ion Battery Packs in:
  - Tablets
  - Slates
  - Power Tools
  - Notebook Computers
  - Portable Equipment and Instrumentation

3 Description

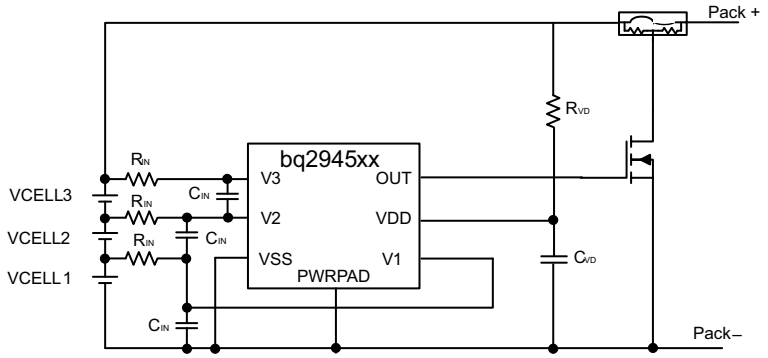
The bq2945xx family of products is a secondary-level voltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition. Based on the configuration, an output is triggered after a fixed delay if any of the two or three cells has an overvoltage condition. This output is triggered into a high state after an overvoltage condition satisfies the specified delay timer.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq2945xx	SON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2012) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added Overvoltage to description ... 1
- Changed bullets to consolidate feature item ... 1
- Added the bq294514 Device ... 1
- Added Fixed OVP Delay Option to Features ... 1
- Changed Absolute Maximum Ratings ... 5
- Changed format of graphs ... 8

Changes from Revision B (February 2012) to Revision C — **Page**

- Added the bq294515 Device to Production Data ... 4
- Added the bq294524 Device to Production Data ... 4
- Added the bq294532 Device to Production Data ... 4
- Added the bq294572 Device to Production Data ... 4
- Changed Overvoltage Detection Hysteresis ... 6
- Added Output Voltage Versus Output Current graphic ... 8
- Changed Timing for Customer Test Mode figure ... 11

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Changes from Revision A (November 2011) to Revision B **Page**

- Changed the bq294504 Device to Production Data 1
- Added the bq294512 Device 1
- Added the bq294592 Device 1
- Added a second I_{CC} Test Condition 6
- Changed Fault Detection Delay Time in bq2945x4 Test Mode Specifications 7

Changes from Original (September 2011) to Revision A **Page**

- Added the bq294582 Device to Production Data 4

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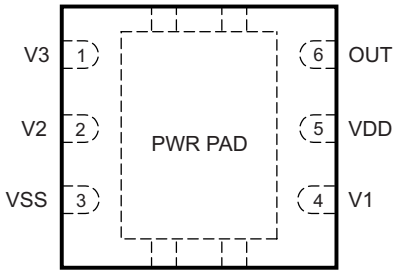
5 Device Options

T_A	PART NUMBER	OVP (V)	DELAY TIME (s)
–40°C to +110°C	bq294502	4.35	4
	bq294504	4.35	6.5
	bq294512	4.4	4
	bq294514	4.4	6.5
	bq294515	4.425	4
	bq294522	4.45	4
	bq294524	4.45	6.5
	bq294532	4.5	4
	bq294562	4.25	4
	bq294572	4	4
	bq294582	4.225	4
	bq294584(1)	4.225	6.5
	bq294592	4.3	4

(1) Product Preview only

6 Pin Configuration and Functions

DRV Package
6-Pin SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	6	OA	Output drive for external N-channel FET.
PWRPAD	—	—	VSS pin to be connected to the PWRPAD on the printed-circuit-board (PCB) for proper operation.
V1	4	IA	Sense input for positive voltage of the lowest cell in the stack.
V2	2	IA	Sense input for positive voltage of the second cell from the bottom of the stack.
V3	1	IA	Sense input for positive voltage of the third cell from the bottom of the stack.
VDD	5	P	Power supply
VSS	3	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage	VDD–VSS	–0.3	30	V
Input voltage	V1–VSS or V2–VSS or V3–VSS+	–0.3	30	V
	V3–V2 or V2–V1	–0.3	8	V
Output voltage	OUT–VSS	–0.3	30	V
Continuous total power dissipation, P_{TOT}		See *Thermal Information*		
Lead temperature (soldering, 10 s), T_{SOLDER}			300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See Figure 8.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}(1)		3		25	V
Input voltage	V3–V2 or V2–V1 or V1–VSS	0		5	V
Operating ambient temperature, T_A		–40		110	°C

(1) See *Typical Application*.

7.4 Thermal Information

THERMAL METRIC(1)		bq2945xx DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	90.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	110.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	96.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 10.8 V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 3 V to 15 V (unless otherwise noted).

TEST NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE PROTECTION THRESHOLD VCx							
1.0	V_{OV}	$V_{(PROTECT)}$ – Overvoltage Detection	bq294502, fixed delay 4 s		4.35		V
1.1			bq294504, fixed delay 6.5 s		4.35		
1.2			bq294512, fixed delay 4 s		4.4		
1.3			bq294514, fixed delay 6.5 s		4.4		
1.4			bq294515, fixed delay 4 s		4.425		
1.5			bq294522, fixed delay 4 s		4.45		
1.6			bq294524, fixed delay 6.5 s		4.45		
1.7			bq294532, fixed delay 4 s		4.5		
1.8			bq294562, fixed delay 4 s		4.25		
1.9			bq294572, fixed delay 4 s		4		
1.10			bq294582, fixed delay 4 s		4.225		
1.11			bq294584, fixed delay 6.5 s (1)		4.225		
1.12			bq294592, fixed delay 4 s		4.3		
1.13	V_{HYS}	Overvoltage Detection Hysteresis		250	300	400	mV
1.14	V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
1.15	$V_{OA\ –DRIFT}$	OV Detection Accuracy due to Temperature	T_A = –40°C T_A = 0°C T_A = 60°C T_A = 110°C	–40 –20 –24 –54		44 20 24 54	mV
SUPPLY AND LEAKAGE CURRENT							
1.16	I_{CC}	Supply Current	(V3–V2) = (V2–V1) = (V1–VSS) = 4 V (See Figure 8 for reference)		1	2	µA
			(V3–V2) = (V2–V1) = (V1–VSS) = 2.8 V with T_A = –40°C to 60°C			1.25	
1.17	I_{IN}	Input Current at Vx Pins	Measured at V3, V2, and V1 = 4 V (V2–V1) = (V1–VSS) = 4 V T_A = 0°C to 60°C (See Figure 8 for reference.)	–0.1		0.1	µA
OUTPUT DRIVE OUT							
1.18	V_{OUT}	Output Drive Voltage	(V3–V2) or (V2–V1) or (V1–VSS) > V_{OV} V_{DD} = 7.2 V, I_{OH} = 100 µA, T_A = –40°C to 110°C	6			V
1.19			Two of the three cells are short circuit and only one cell is powered (V3–V2) or (V2–V1) or (V1–VSS) > V_{OV} V_{DD} = Vx (Cell voltage), I_{OH} = 100 µA, T_A = –40°C to 110°C		VDD – 0.2		V
1.20			(V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, I_{OL} = 100 µA, T_A = 25°C T_A = –40°C to 110°C		250	400	mV
1.21	$I_{OUT(Short)}$	OUT Short Circuit Current	OUT = 0 V (V3–V2) or (V2–V1) or (V1–VSS) > V_{OV}			4.5	mA
1.22	t_R	Output Rise Time	CL = 1 nF, $V_{OH(OUT)}$ = 0 V to 5 V (2)		5		µs
1.23	Z_O	Output Impedance			2	5	kΩ

(1) Product Preview only.
(2) Specified by design. Not 100% tested in production.

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Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VDD = 10.8 V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 3 V to 15 V (unless otherwise noted).

TEST NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FIXED DELAY TIMER							
1.24	t_{DELAY}	Fault Detection Delay Time	Fixed Delay, bq2945x2	3.2	4	4.8	s
			Fixed Delay, bq2945x4	5.2	6.5	7.8	
1.25	t_{DELAY_CTM}	Fault Detection Delay Time in Test Mode	Fixed Delay (Internal settings)		15		ms

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7.6 Typical Characteristics

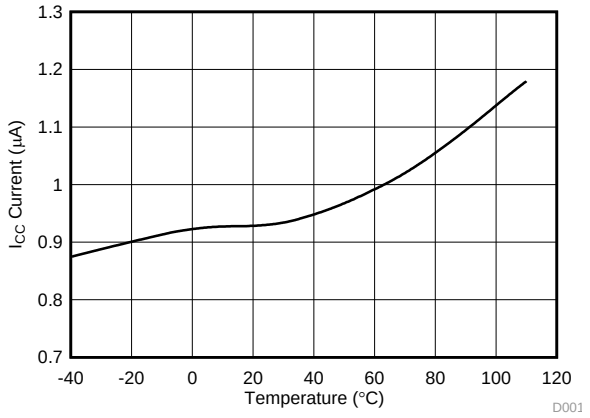

Figure 1. I_{CC} Current Consumption vs Temperature

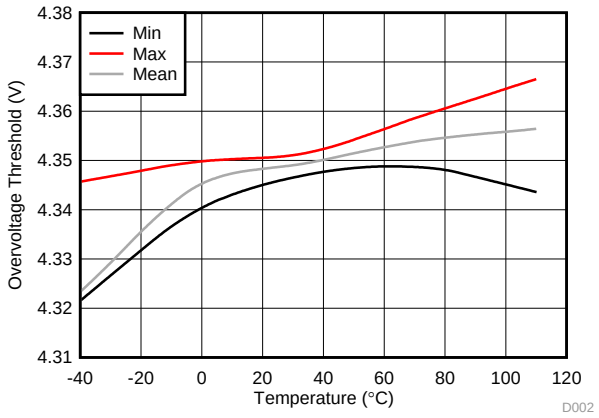

Figure 2. bq294502 Overvoltage Threshold (OVT) vs Temperature

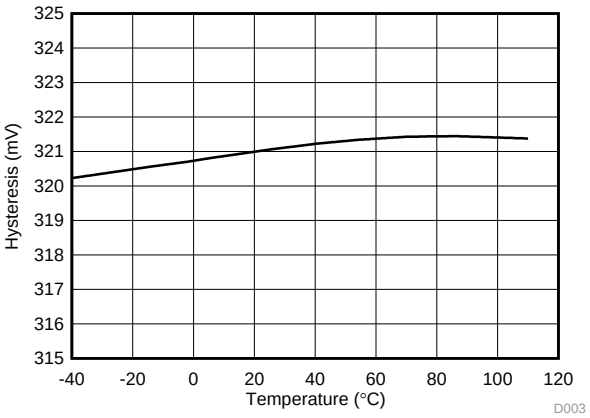

Figure 3. Hysteresis V_{HYS} vs Temperature

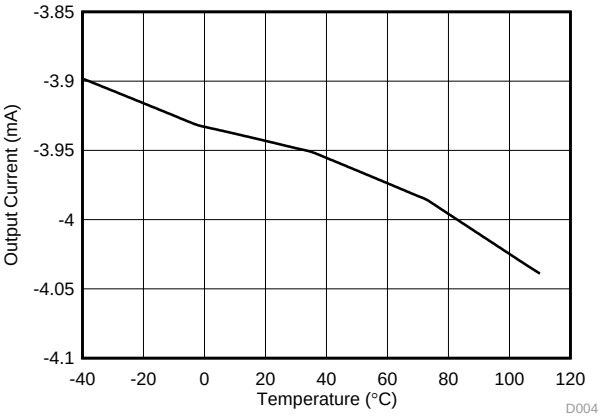

Figure 4. Output Current I_{OUT} vs Temperature

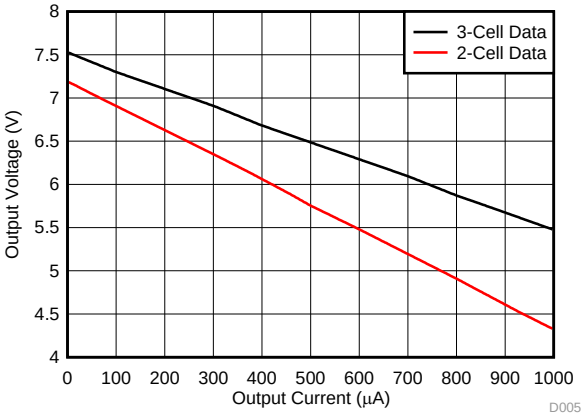

Figure 5. Output Voltage vs Output Current

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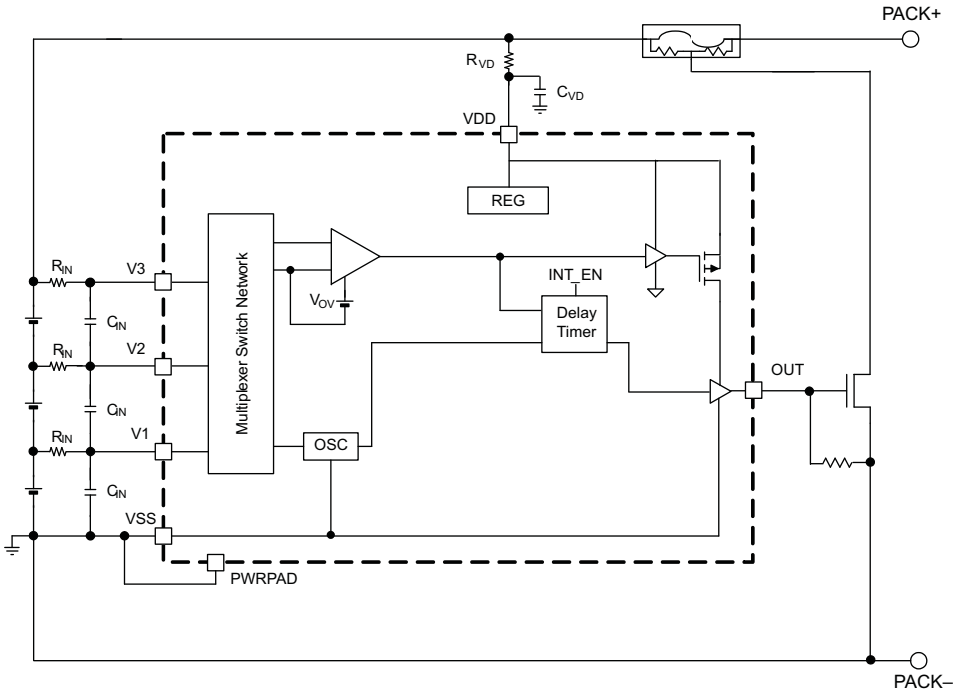
8 Detailed Description

8.1 Overview

The bq2945xx is a second-level overvoltage (OV) protector. Each cell is monitored independently by comparing the actual cell voltage to a protection voltage threshold, V_{OV}. The protection threshold is preprogrammed at the factory with a range from 3.85 V to 4.65 V.

8.2 Functional Block Diagram



8.3 Feature Description

The voltage sensing for each cell is done independently using a multiplexer. The method of overvoltage detection is comparing the voltage to an overvoltage protection voltage V_{OV}. Once the voltage exceeds the programmed fixed value, the delay timer circuit is activated. This delay (t_{DELAY}) is fixed for either a 4-s or 6.5-s delay. When these conditions are satisfied, the OUT terminal is transitioned to a high level. This output (OUT) is released to a low condition if *all* of the cell inputs (Vx) are below the OVP threshold minus the Vhys.

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Feature Description (continued)

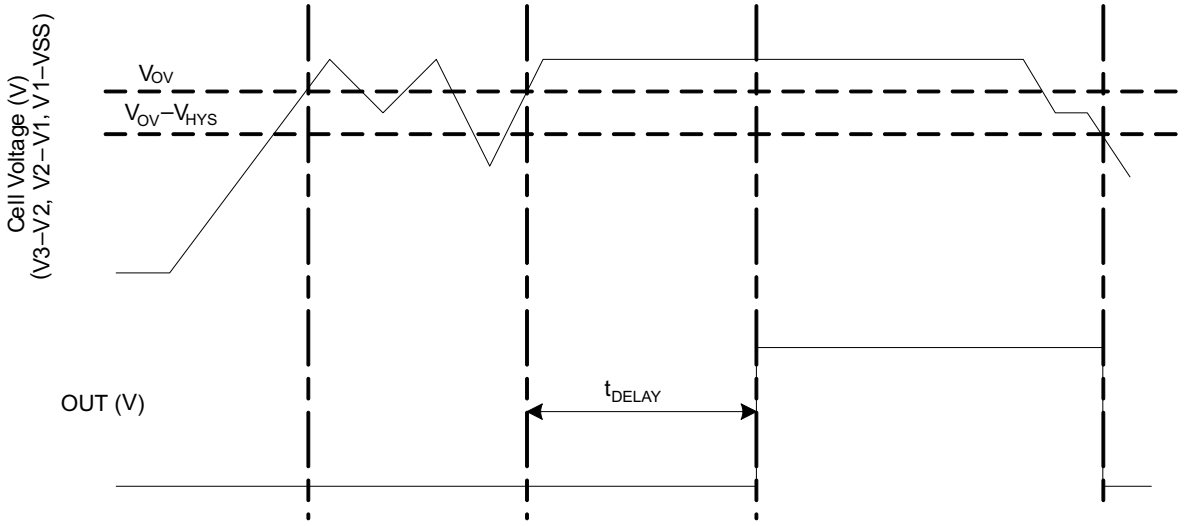

Figure 6. Timing for Overvoltage Sensing

8.3.1 Sense Positive Input for VX

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.2 Output Drive, OUT

The gate of an external N-channel MOSFET is connected to this terminal. This output transitions to a high level when an overvoltage condition is detected and after the programmed delay timer. OUT will reset to a low level if the cell voltage falls below the V_{OV} threshold before the fixed delay timer expires.

8.3.3 Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.3.4 Thermal Pad, PWRPAD

For correct operation, the power pad (PWRPAD) is connected to the V_{SS} terminal on the PCB.

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When all of the cell voltages are below the overvoltage threshold, VOV, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1–VSS), (V2–V1) and (V3–V2). The OUT pin is inactive in this mode.

8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceeds the overvoltage threshold, V_{OV} for the configured OV delay time, tDELAY. The OUT pin will pull high internally. An external FET ihen turns on, shorting the fuse to ground, which allows the battery and/or charger power to blow the fuse. When all of the cell voltages fall below (V_{OV}–V_{HYS}), the device returns to NORMAL mode.

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Device Functional Modes (continued)

8.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V3 (see Figure 7). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit CTM, remove the VDD to VC3 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into CTM. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 7 shows the timing for CTM.

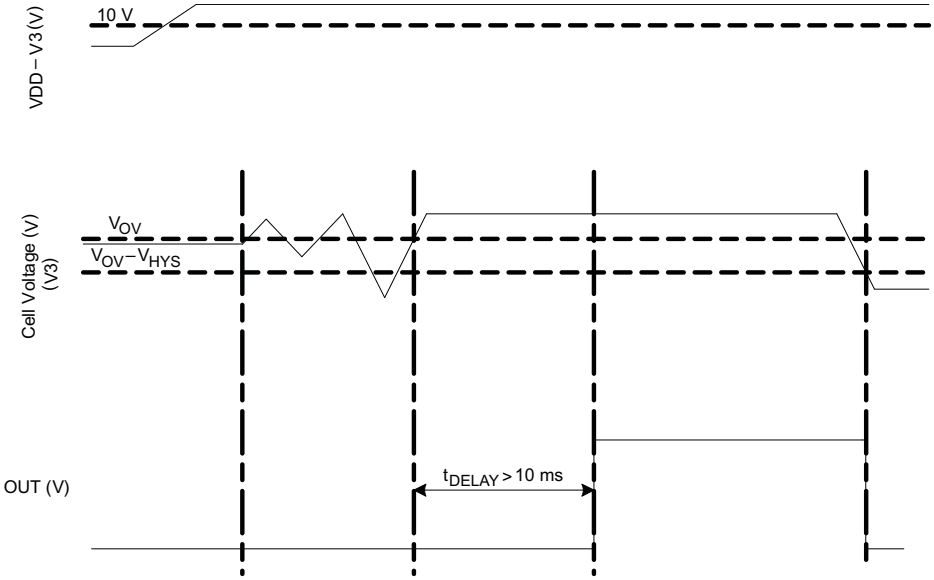

Figure 7. Timing for Customer Test Mode

Figure 8 shows the measurement for current consumption for the product for both VDD and Vx.

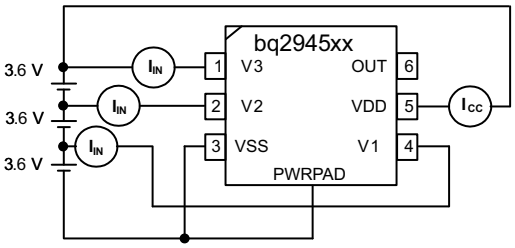

Figure 8. Configuration for IC Current Consumption Test

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq2945xx devices are a family of second-level protectors used for overvoltage protection of the battery pack in the application. The device, when configuring the OUT pin with active high, drives a NMOS FET that connects the fuse to ground in the event of a fault condition. This provides a shorted path to use the battery and/or charger power to blow the fuse and cut the power path.

9.2 Typical Application

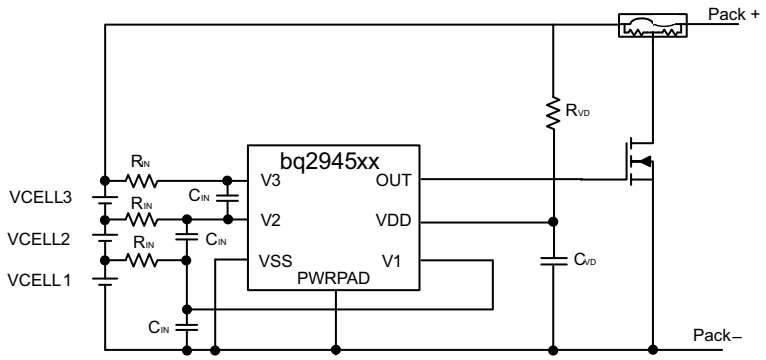

Figure 9. Application Configuration Schematic

9.2.1 Design Requirements

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements. Figure 9 shows each external component.

Table 1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	TYP	MAX	UNIT
Voltage monitor filter resistance	RIN	900	1000	1100	Ω
Voltage monitor filter capacitance	CIN	0.01		0.1	µF
Supply voltage filter resistance	RVD	100		1K	Ω
Supply voltage filter capacitance	CVD		0.1		µF

9.2.2 Detailed Design Procedure

1. Determine the overvoltage threshold and delay time. Select the proper device from the table in *Device Options*, or contact TI for a different configuration.
2. Determine the number of cell in series. The device supports 2-S to 3-S cell configuration. For 2-S configuration, V3 pin should be shorted to V2.
3. Follow the application configuration schematic (see Figure 9) to connect the device.

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9.2.3 Application Curves

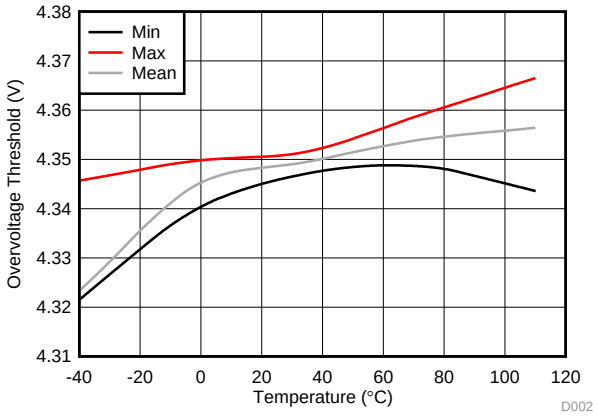

Figure 10. OVT vs Temperature

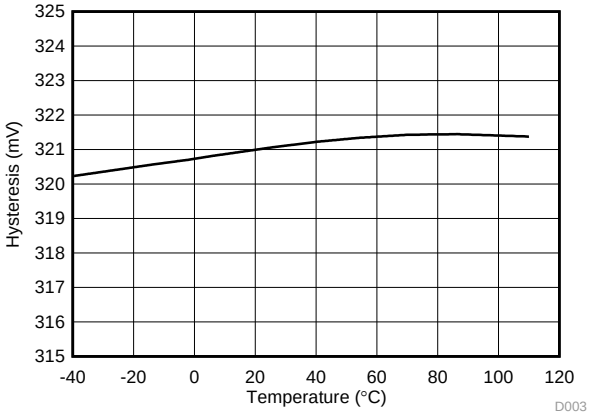

Figure 11. V_{HYS} vs Temperature

9.3 System Examples

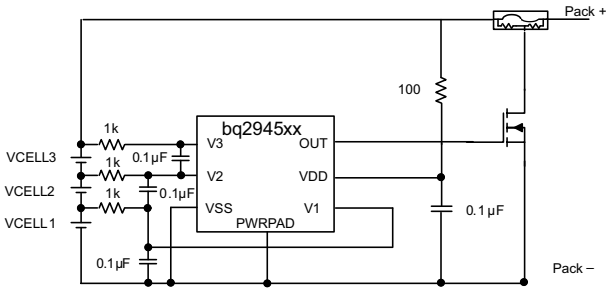

Figure 12. 3-Series Cell Configuration With Fixed Delay

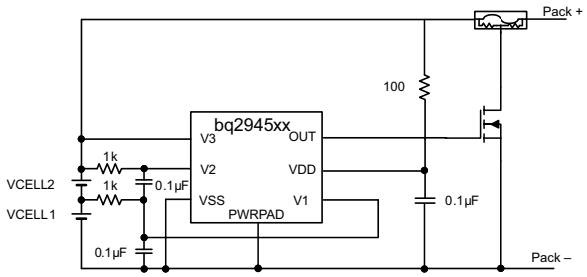

Figure 13. 2-Series Cell Configuration With Internal Fixed Delay

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10 Power Supply Recommendations

The maximum power of this device is 25 V on VDD.

11 Layout

11.1 Layout Guidelines

- Ensure the RC filters for the V1 and VDD pins are placed as close as possible to the target terminal, reducing the tracing loop area.
- The VSS pin should be routed to the CELL– terminal.
- Ensure the trace connecting the fuse to the gate, source of the NFET to the Pack– is sufficient to withstand the current during a fuse blown event.

11.2 Layout Example

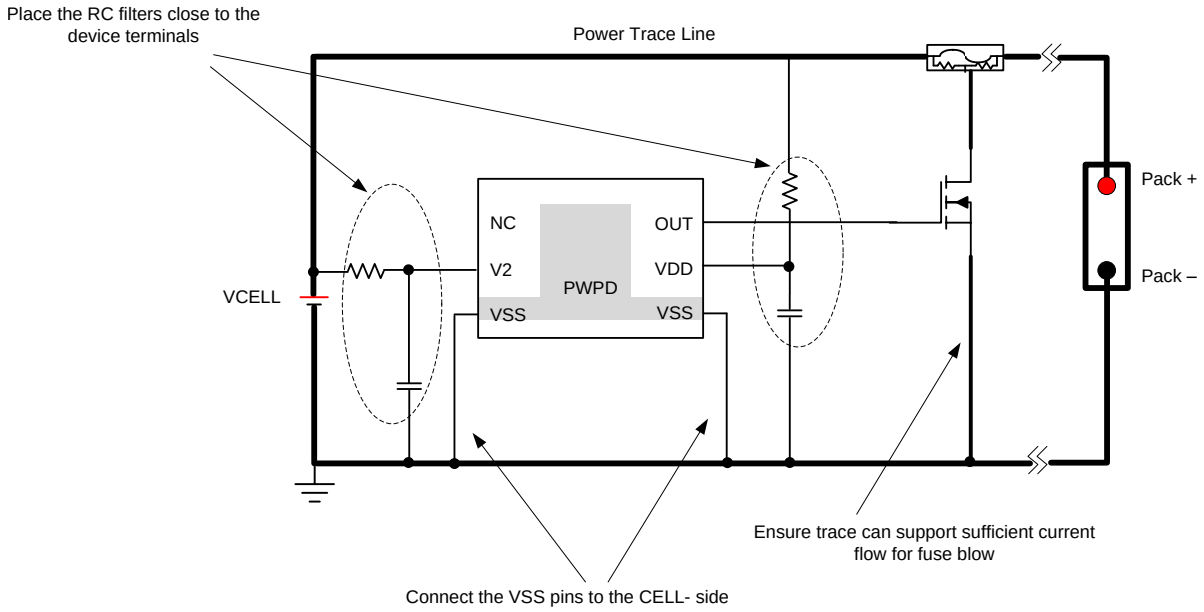

Figure 14. Layout Schematic

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq294502	Click here	Click here	Click here	Click here	Click here
bq294504	Click here	Click here	Click here	Click here	Click here
bq294512	Click here	Click here	Click here	Click here	Click here
bq294514	Click here	Click here	Click here	Click here	Click here
bq294515	Click here	Click here	Click here	Click here	Click here
bq294522	Click here	Click here	Click here	Click here	Click here
bq294524	Click here	Click here	Click here	Click here	Click here
bq294532	Click here	Click here	Click here	Click here	Click here
bq294562	Click here	Click here	Click here	Click here	Click here
bq294572	Click here	Click here	Click here	Click here	Click here
bq294582	Click here	Click here	Click here	Click here	Click here
bq294592	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ294502DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4502	Samples
BQ294502DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4502	Samples
BQ294504DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4504	Samples
BQ294504DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4504	Samples
BQ294512DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4512	Samples
BQ294512DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4512	Samples
BQ294515DRVR	PREVIEW	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4515	
BQ294515DRVT	PREVIEW	WSON	DRV	6		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4515	
BQ294522DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4522	Samples
BQ294522DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4522	Samples
BQ294524DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4524	Samples
BQ294524DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4524	Samples
BQ294532DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4532	Samples
BQ294532DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4532	Samples
BQ294582DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4582	Samples
BQ294582DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4582	Samples
BQ294592DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4592	Samples

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ294592DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4592	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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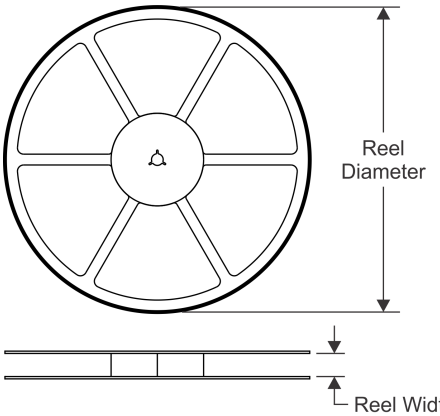
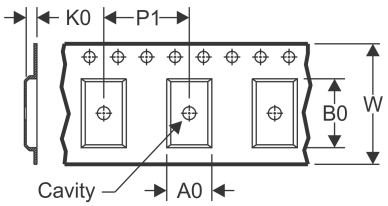
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

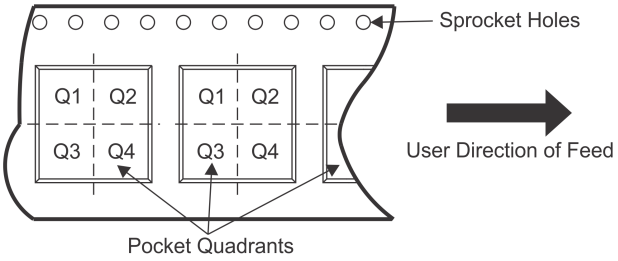


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294502DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294502DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294512DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294512DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294515DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294515DRVT	WSON	DRV	6	0	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294522DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294522DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294524DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294524DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294532DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294532DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

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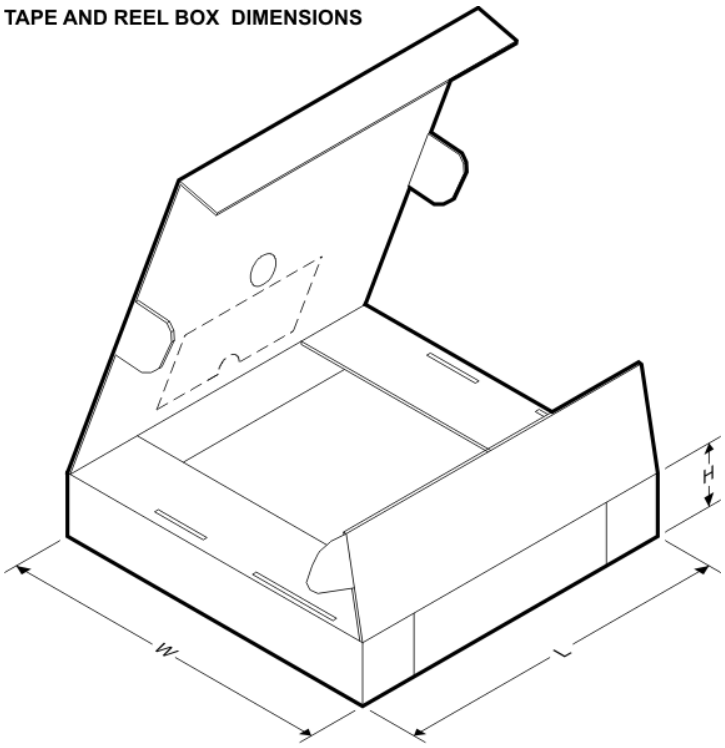
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294502DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294502DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294504DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294504DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294512DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294512DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294515DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294515DRVT	WSON	DRV	6	0	210.0	185.0	35.0
BQ294522DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294522DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294524DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294524DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294532DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294532DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294582DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294582DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294592DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294592DRVT	WSON	DRV	6	250	210.0	185.0	35.0

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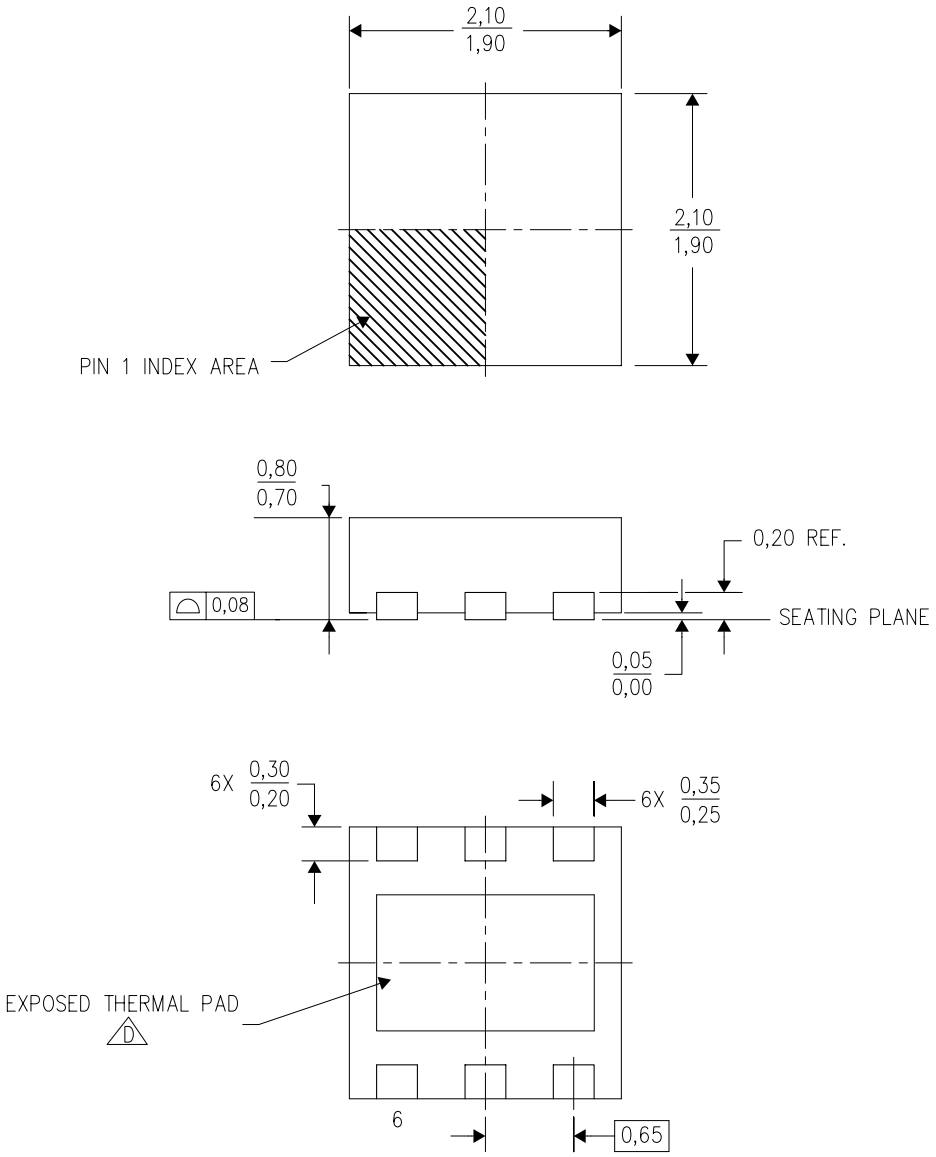
MECHANICAL DATA

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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THERMAL PAD MECHANICAL DATA

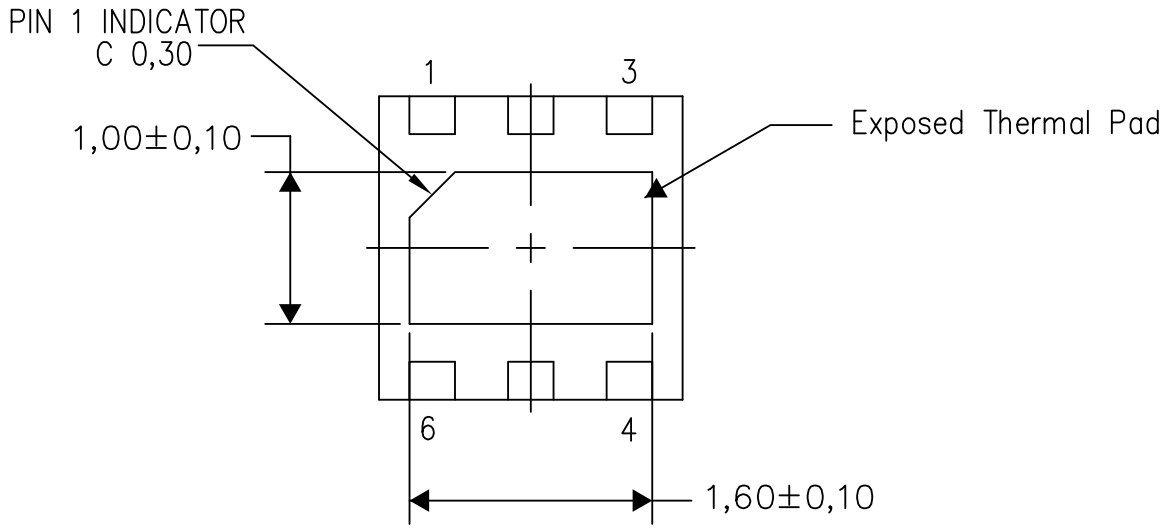
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

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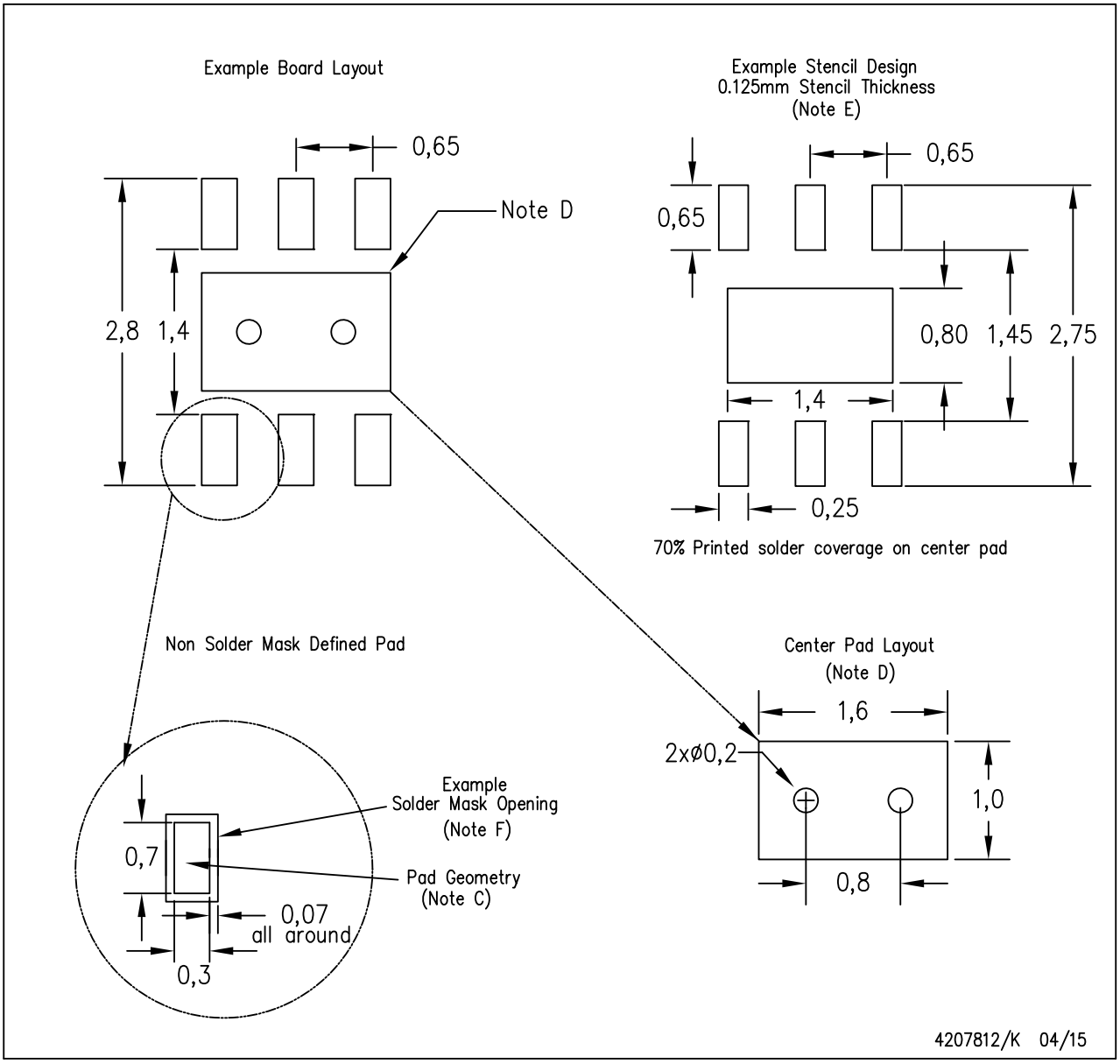
LAND PATTERN DATA

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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