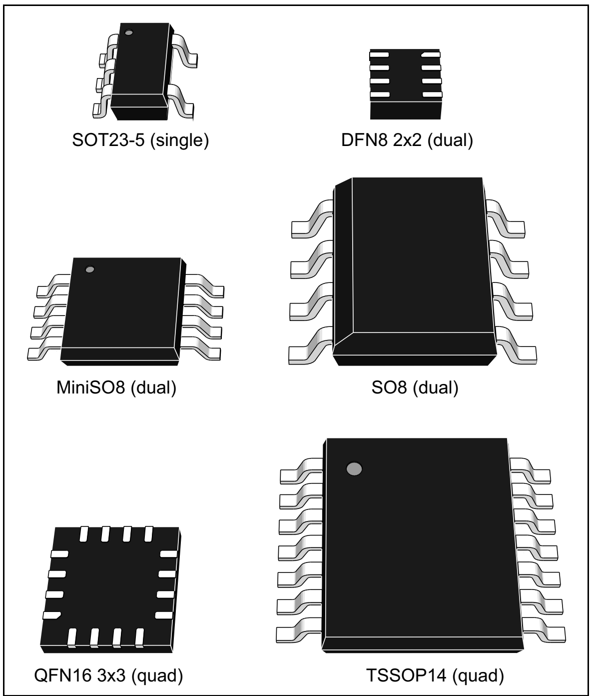
TSX561, TSX562, TSX564, TSX561A, TSX562A, TSX564A

Micropower, wide bandwidth (900 kHz), 16 V CMOS operational amplifiers

Datasheet - production data



Features

- Low power consumption: 235 µA typ. at 5 V
- Supply voltage: 3 V to 16 V
- Gain bandwidth product: 900 kHz typ.
- Low offset voltage
  - "A" version: 600 µV max.
  - Standard version: 1 mV max.
- Low input bias current: 1 pA typ.
- High tolerance to ESD: 4 kV
- Wide temperature range: -40 to +125 °C
- Automotive qualification
- Tiny packages available
  - SOT23-5
  - DFN8 2 mm x 2 mm, MiniSO8, SO8
  - QFN16 3 mm x 3 mm, TSSOP14

Benefits

- Power savings in power-conscious applications
- Easy interfacing with high impedance sensors

Related products

- See TSX63x series for reduced power consumption (45 µA, 200 kHz)
- See TSX92x series for higher gain bandwidth products (10 MHz)

Applications

- Industrial and automotive signal conditioning
- Active filtering
- Medical instrumentation
- High impedance sensors

Description

The TSX56x, TSX56xA series of operational amplifiers benefit from STMicroelectronics® 16 V CMOS technology to offer state-of-the-art accuracy and performance in the smallest industrial packages. The TSX56x, TSX56xA have pinouts compatible with industrial standards and offer an outstanding speed/power consumption ratio, 900 kHz gain bandwidth product while consuming only 250 µA at 16 V. Such features make the TSX56x, TSX56xA ideal for sensor interfaces and industrial signal conditioning. The wide temperature range and high ESD tolerance ease use in harsh automotive applications.

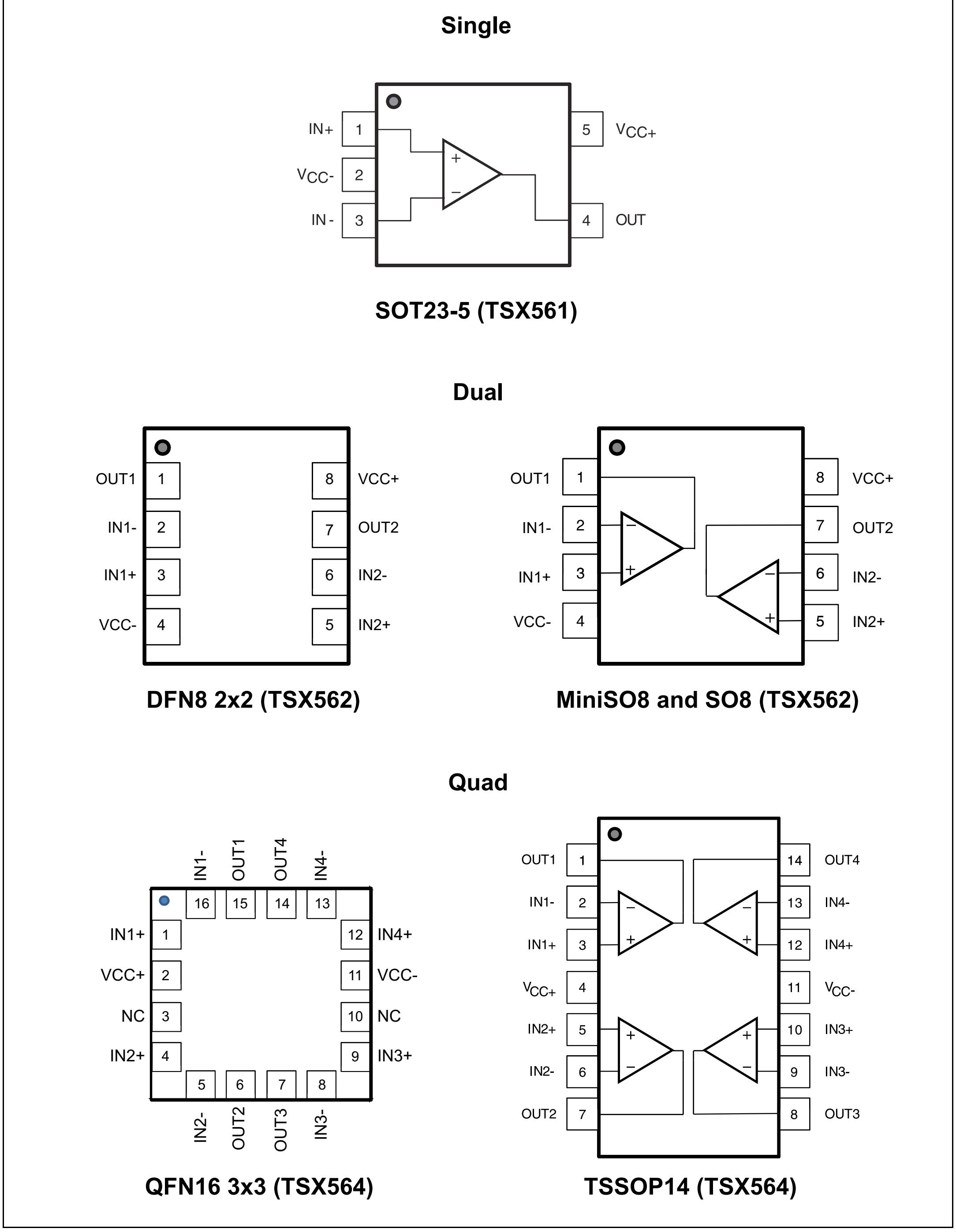
Table 1. Device summary

Version	Standard V_{io}	Enhanced V_{io}
Single	TSX561	TSX561A
Dual	TSX562	TSX562A
Quad	TSX564	TSX564A

Contents

1 Pin connections

Figure 1. Pin connections for each package (top view)



2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage[1]	18	V
V_{id}	Differential input voltage[2]	$\pm V_{CC}$	
V_{in}	Input voltage[3]	V_{CC-} - 0.2 to V_{CC+} + 0.2	
I_{in}	Input current[4]	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient[5][6] SOT23-5 DFN8 2x2 MiniSO8 SO8 QFN16 3x3 TSSOP14	 250 120 190 125 80 100	°C/W
R_{thjc}	Thermal resistance junction to case DFN8 2x2 QFN16 3x3	 33 30	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model[7]	4	kV
	MM: machine model for TSX561[8]	200	V
	MM: machine model for TSX562 and TSX564[8]	100	
	CDM: charged device model[9]	1.5	kV
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. V_{CC} - V_{in} must not exceed 18 V, V_{in} must not exceed 18 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 16	V
V_{icm}	Common mode input voltage range	V_{CC-} - 0.1 to V_{CC+} + 0.1	
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 4. Electrical characteristics at V_{CC+} = +3.3 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L=10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSX56xA, T = 25 °C			600	µV
		TSX56xA, -40 °C < T < 125 °C			1800	
		TSX56x, T = 25 °C			1	mV
		TSX56x, -40 °C < T < 125 °C			2.2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 125 °C(1)		2	12	µV/°C
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		1	100(2)	pA
		-40 °C < T < 125 °C		1	200(2)	
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		1	100(2)	
		-40 °C < T < 125 °C		1	200(2)	
CMR1	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC}-1.5 V, V_{out} = V_{CC}/2, R_L > 1 MΩ)	T = 25 °C	63	80		dB
		-40 °C < T < 125 °C	59			
CMR2	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC}+0.1 V, V_{out} = V_{CC}/2, R_L > 1 MΩ)	T = 25 °C	47	66		
		-40 °C < T < 125 °C	45			
A_{vd}	Large signal voltage gain (V_{out} = 0.5 V to (V_{CC} - 0.5 V), R_L > 1 MΩ)	T = 25 °C	85			
		-40 °C < T < 125 °C	83			
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{out})	T = 25 °C			70	mV
		-40 °C < T < 125 °C			100	
V_{OL}	Low level output voltage	T = 25 °C			70	
		-40 °C < T < 125 °C			100	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	4.3	5.3		mA
		-40 °C < T < 125 °C	2.5			
	I_{source} (V_{out} = 0 V)	T = 25 °C	3.3	4.3		
		-40 °C < T < 125 °C	2.5			
I_{CC}	Supply current (per channel, V_{out} = V_{CC}/2, R_L > 1 MΩ)	T = 25 °C		220	300	µA
		-40 °C < T < 125 °C			350	

Table 4. Electrical characteristics at V_{CC+} = +3.3 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 °C, and R_L=10 kΩ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	600	800		kHz
F_u	Unity gain frequency			690		kHz
Φ_m	Phase margin			55		Degree
G_m	Gain margin			9		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V		1		V/µs
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		16		μV_{pp}
e_n	Equivalent input noise voltage density	f = 1 kHz f = 10 kHz		55 29		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	Follower configuration, f_{in} = 1 kHz, R_L = 100 kΩ, V_{icm} = (V_{CC} -1.5 V)/2, BW = 22 kHz, V_{out} = 1 V_{pp}		0.004		%

1. See *Section 4.3: Input offset voltage drift over temperature on page 15*.
2. Guaranteed by design.

Table 5. Electrical characteristics at V_{CC+} = +5 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSX56xA, T = 25 °C			600	µV
		TSX56xA, -40 °C < T < 125 °C			1800	µV
		TSX56x, T = 25 °C			1	mV
		TSX56x, -40 °C < T < 125 °C			2.2	mV
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 125 °C(1)		2	12	µV/°C
ΔV_{io}	Long-term input offset voltage drift	T = 25 °C(2)		5		$\frac{nV}{\sqrt{month}}$
I_{io}	Input offset current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	pA
I_{ib}	Input bias current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	pA
CMR1	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC} - 1.5 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	66	84		dB
		-40 °C < T < 125 °C	63			dB
CMR2	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC} + 0.1 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	50	69		dB
		-40 °C < T < 125 °C	47			dB
A_{vd}	Large signal voltage gain (V_{out} = 0.5 V to (V_{CC} - 0.5 V), R_L > 1 MΩ)	T = 25 °C	85			dB
		-40 °C < T < 125 °C	83			dB
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{out})	R_L = 10 kΩ, T = 25 °C R_L = 10 kΩ, -40 °C < T < 125 °C			70 100	mV
V_{OL}	Low level output voltage	R_L = 10 kΩ, T = 25 °C R_L = 10 kΩ, -40 °C < T < 125 °C			70 100	mV
I_{out}	I_{sink}	V_{out} = V_{CC}, T = 25 °C	11	14		mA
		V_{out} = V_{CC}, -40 °C < T < 125 °C	8			mA
	I_{source}	V_{out} = 0 V, T = 25 °C	9	12		mA
		V_{out} = 0 V, -40 °C < T < 125 °C	7			mA
I_{CC}	Supply current (per channel, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C		235	350	µA
		-40 °C < T < 125 °C			400	µA

Table 5. Electrical characteristics at V_{CC+} = +5 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	700	850		kHz
F_u	Unity gain frequency			730		
Φ_m	Phase margin			55		Degree
G_m	Gain margin			9		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V		1.1		V/μs
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		15		μV_{pp}
e_n	Equivalent input noise voltage density	f = 1 kHz f = 10 kHz		55 29		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	Follower configuration, f_{in} = 1 kHz, R_L = 100 kΩ, V_{icm} = (V_{CC} - 1.5 V)/2, BW = 22 kHz, V_{out} = 2 V_{pp}		0.002		%

1. See *Section 4.3: Input offset voltage drift over temperature on page 15*.
2. Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.
3. Guaranteed by design.

Table 6. Electrical characteristics at V_{CC+} = +16 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSX56xA, T = 25 °C			600	µV
		TSX56xA, -40 °C < T < 125 °C			1800	µV
		TSX56x, T = 25 °C			1	mV
		TSX56x, -40 °C < T < 125 °C			2.2	mV
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 125 °C(1)		2	12	µV/°C
ΔV_{io}	Long-term input offset voltage drift	T = 25 °C(2)		1.6		$\frac{\mu V}{\sqrt{month}}$
I_{io}	Input offset current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	pA
I_{ib}	Input bias current (V_{out} = $V_{CC}/2$)	T = 25 °C		1	100(3)	pA
		-40 °C < T < 125 °C		1	200(3)	pA
CMR1	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC} - 1.5 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	76	95		dB
		-40 °C < T < 125 °C	72			dB
CMR2	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic}$ = -0.1 V to V_{CC} + 0.1 V, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C	60	78		dB
		-40 °C < T < 125 °C	56			dB
SVR	Common mode rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$) ($V_{CC}$ = 3 V to 16 V, V_{out} = V_{icm} = $V_{CC}/2$)	T = 25 °C	76	90		dB
		-40 °C < T < 125 °C	72			dB
A_{vd}	Large signal voltage gain (V_{out} = 0.5 V to (V_{CC} - 0.5 V), R_L > 1 MΩ)	T = 25 °C	85			dB
		-40 °C < T < 125 °C	83			dB
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{out})	R_L = 10 kΩ, T = 25 °C R_L = 10 kΩ, -40 °C < T < 125 °C			70 100	mV
V_{OL}	Low level output voltage	R_L = 10 kΩ, T = 25 °C R_L = 10 kΩ, -40 °C < T < 125 °C			70 100	mV
I_{out}	I_{sink}	V_{out} = V_{CC}, T = 25 °C	40	92		mA
		V_{out} = V_{CC}, -40 °C < T < 125 °C	35			mA
	I_{source}	V_{out} = 0 V, T = 25 °C	30	90		mA
		V_{out} = 0 V, -40 °C < T < 125 °C	25			mA
I_{CC}	Supply current (per channel, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C		250	360	µA
		-40 °C < T < 125 °C			400	µA

Table 6. Electrical characteristics at V_{CC+} = +16 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	750	900		kHz
F_u	Unity gain frequency			750		kHz
Φ_m	Phase margin			55		Degree
G_m	Gain margin			9		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V		1.1		V/μs
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		15		μV_{pp}
e_n	Equivalent input noise voltage density	f = 1 kHz f = 10 kHz		48 27		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise	Follower configuration, f_{in} = 1 kHz, R_L = 100 kΩ, V_{icm} = (V_{CC} - 1.5 V)/2, BW = 22 kHz, V_{out} = 5 V_{pp}		0.0005		%

1. See *Section 4.3: Input offset voltage drift over temperature on page 15*.
2. Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.
3. Guaranteed by design.

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

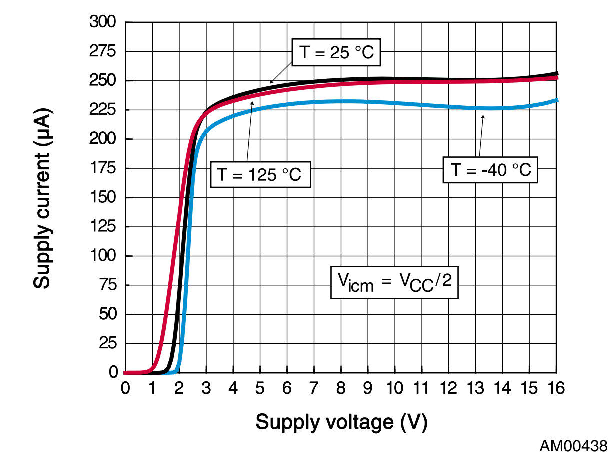


Figure 3. Input offset voltage distribution at V_{CC} = 16 V and V_{icm} = 8 V

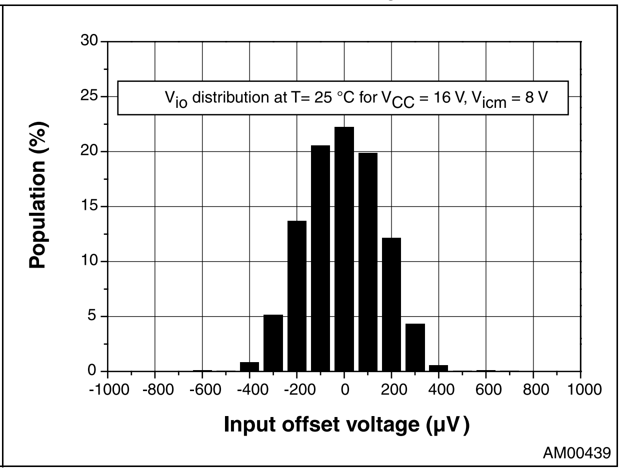


Figure 4. Input offset voltage temperature coefficient distribution at V_{CC} = 16 V, V_{icm} = 8 V

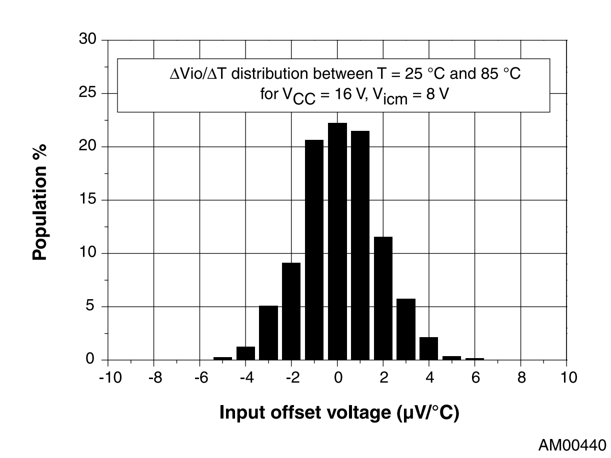


Figure 5. Input offset voltage vs. input common mode voltage at V_{CC} = 12 V

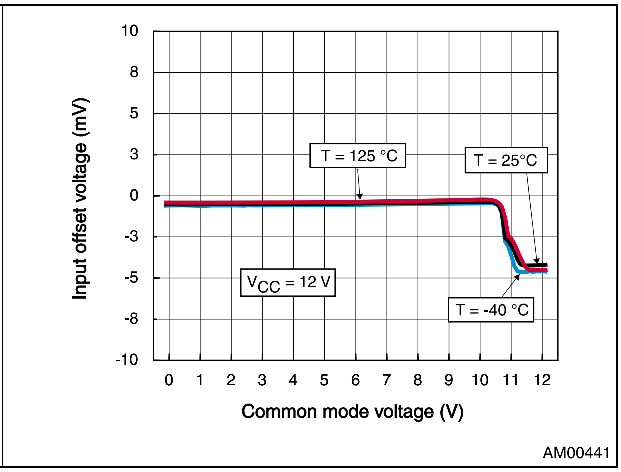


Figure 6. Input offset voltage vs. temperature at V_{CC} = 16 V

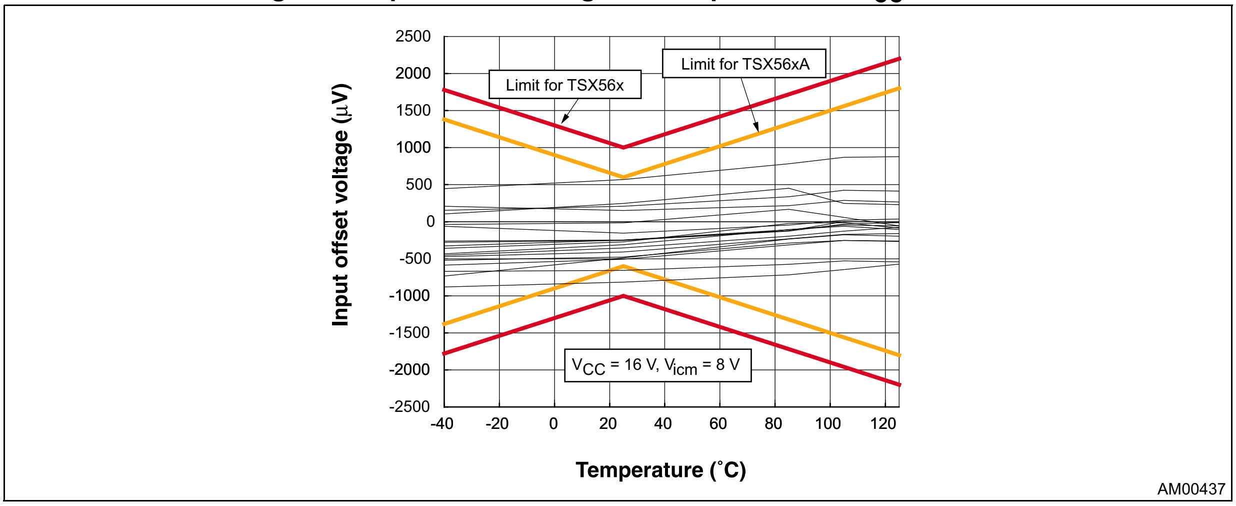


Figure 7. Output current vs. output voltage at V_{CC} = 3.3 V

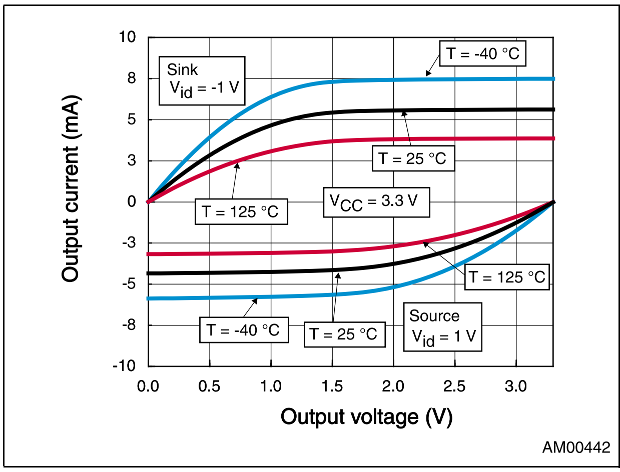


Figure 8. Output current vs. output voltage at V_{CC} = 5 V

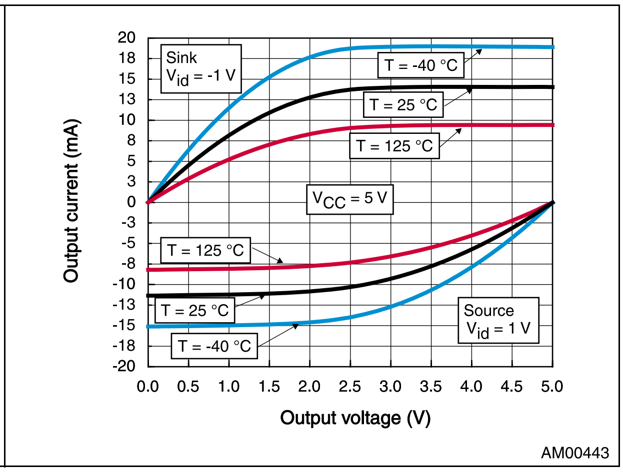


Figure 9. Output current vs. output voltage at V_{CC} = 16 V

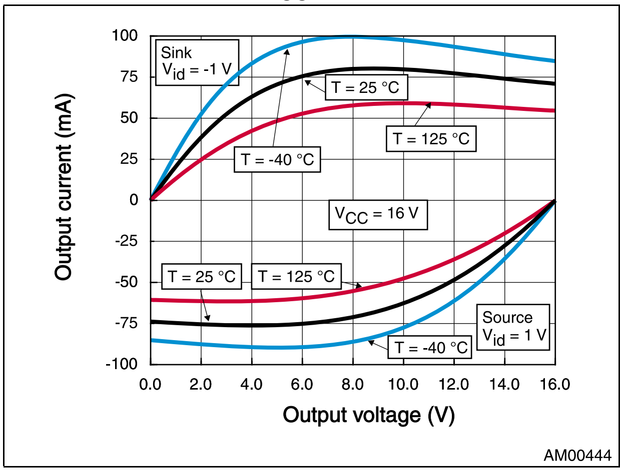


Figure 10. Bode diagram at V_{CC} = 3.3 V

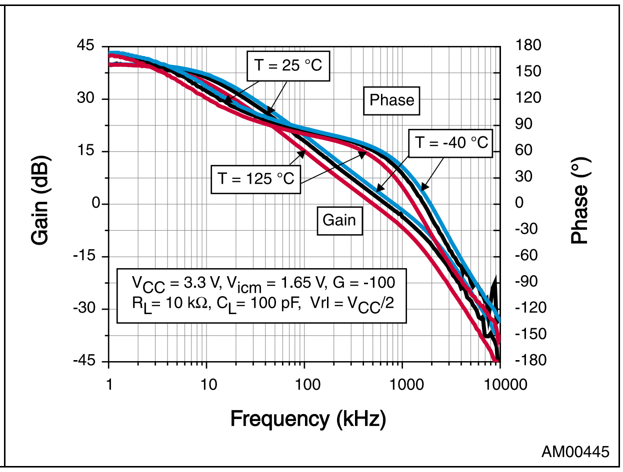


Figure 11. Bode diagram at V_{CC} = 5 V

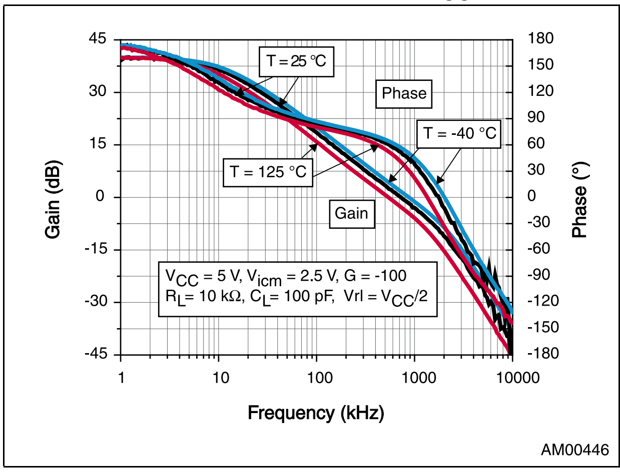


Figure 12. Bode diagram at V_{CC} = 16 V

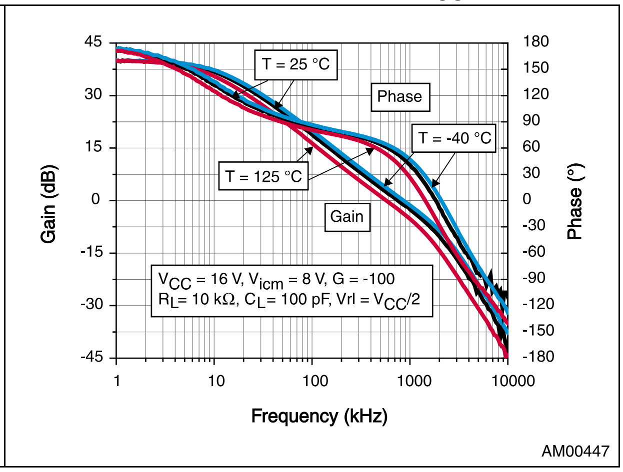


Figure 13. Phase margin vs. capacitive load at V_{CC} = 12 V

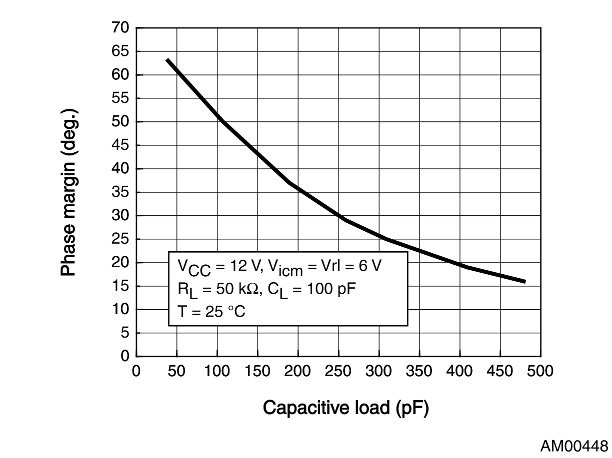


Figure 14. GBP vs. input common mode voltage at V_{CC} = 12 V

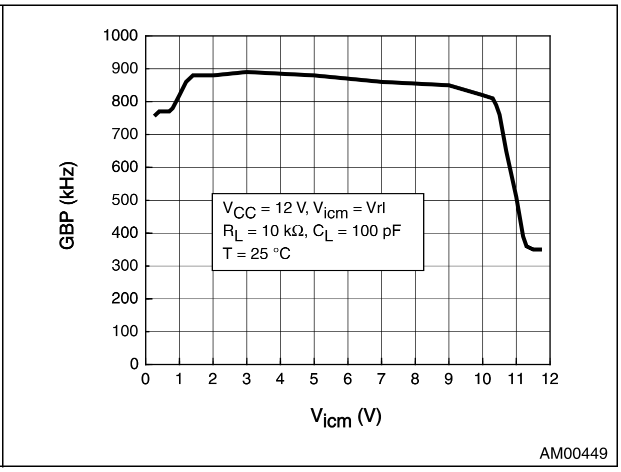


Figure 15. A_{vd} vs. input common mode voltage at V_{CC} = 12 V

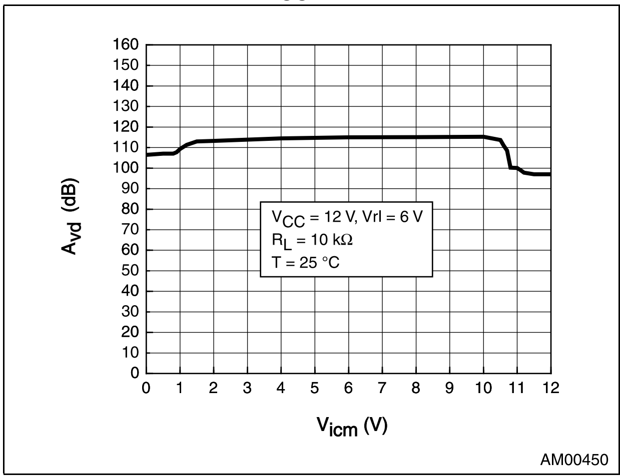


Figure 16. Slew rate vs. supply voltage

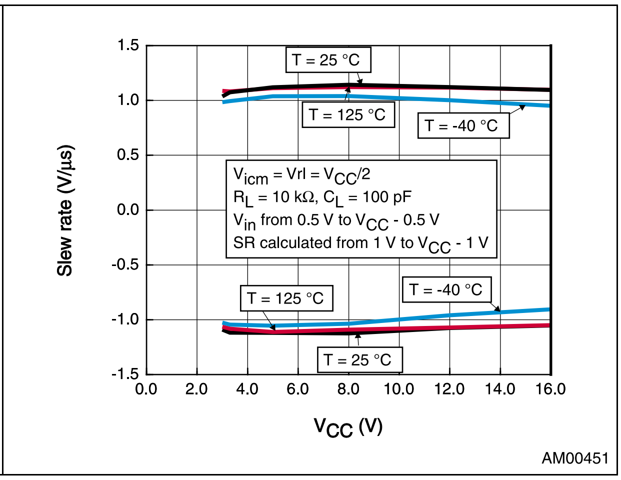


Figure 17. Noise vs. frequency at V_{CC} = 3.3 V

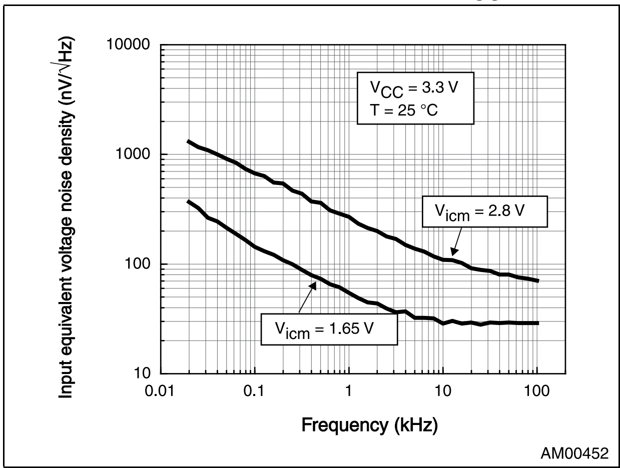


Figure 18. Noise vs. frequency at V_{CC} = 5 V

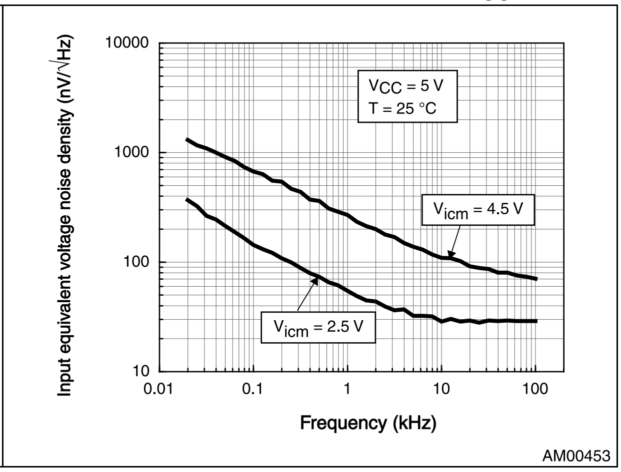


Figure 19. Noise vs. frequency at V_{CC} = 16 V

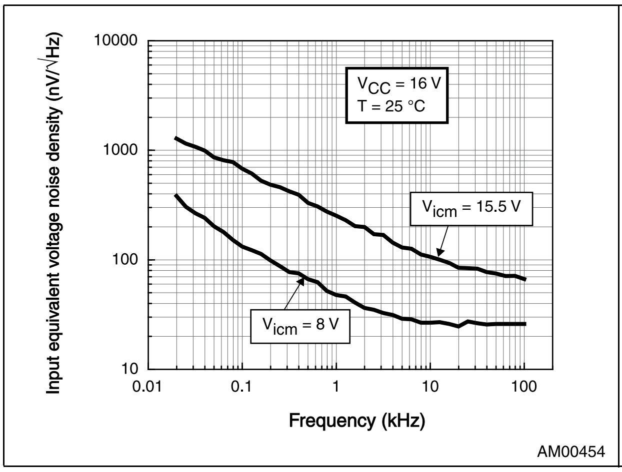


Figure 20. Distortion + noise vs. output voltage amplitude

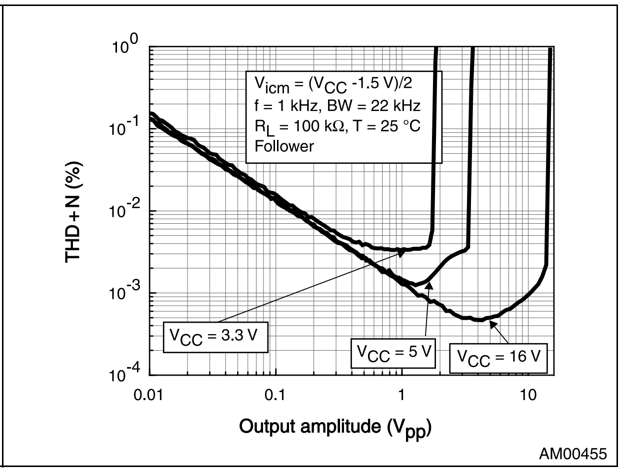


Figure 21. Distortion + noise vs. amplitude at V_{icm} = V_{CC}/2 and V_{CC} = 12 V

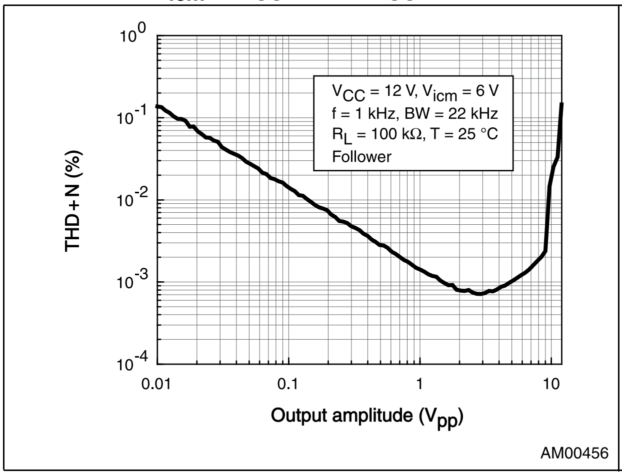
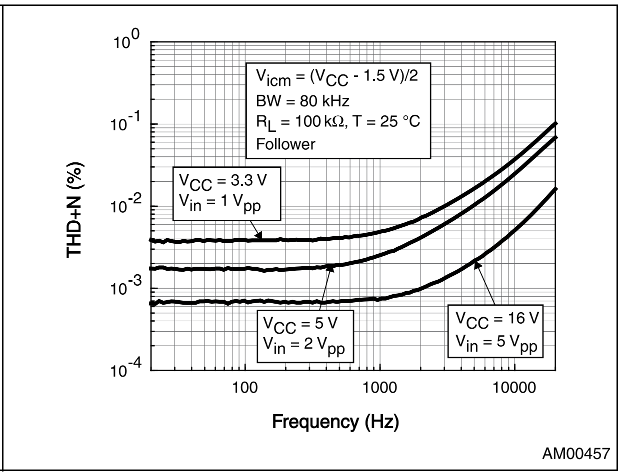


Figure 22. Distortion + noise vs. frequency



4 Application information

4.1 Operating voltages

The amplifiers of the TSX56x and TSX56xA series can operate from 3 V to 16 V. Their parameters are fully specified at 3.3 V, 5 V and 16 V power supplies. However, the parameters are very stable in the full V_{CC} range. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to +125 ° C.

4.2 Rail-to-rail input

The TSX56x and TSX56xA devices are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common mode range is extended from V_{CC-} - 0.1 V to V_{CC+} + 0.1 V.

However, the performance of these devices is clearly optimized for the PMOS differential pairs (which means from V_{CC-} - 0.1 V to V_{CC+} - 1.5 V).

Beyond V_{CC+} - 1.5 V, the operational amplifiers are still functional but with degraded performance, as can be observed in the electrical characteristics section of this datasheet (mainly V_{io} and GBP). These performances are suitable for a number of applications needing to be rail-to-rail.

The devices are designed to prevent phase reversal.

4.3 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effects of temperature variations.

The maximum input voltage drift over temperature is computed in *Equation 1*.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°\,C)}{T - 25°\,C}\right|$$

with T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 2.

4.4 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173 x 10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000\ \text{h} \times 12\ \text{months} / (24\ \text{h} \times 365.25\ \text{days})$$

To evaluate the op-amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

Equation 7

$$\Delta V_{io} = \frac{V_{io}\text{drift}}{\sqrt{(\text{months})}}$$

where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

4.5 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

4.6 Macromodel

Accurate macromodels of the TSX56x, TSX56xA devices are available on the STMicroelectronics' website at *www.st.com*. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSX56x and TSX56xA operational amplifiers. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, *but they do not replace on-board measurements*.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.1 SOT23-5 package information

Figure 23. SOT23-5 package mechanical drawing

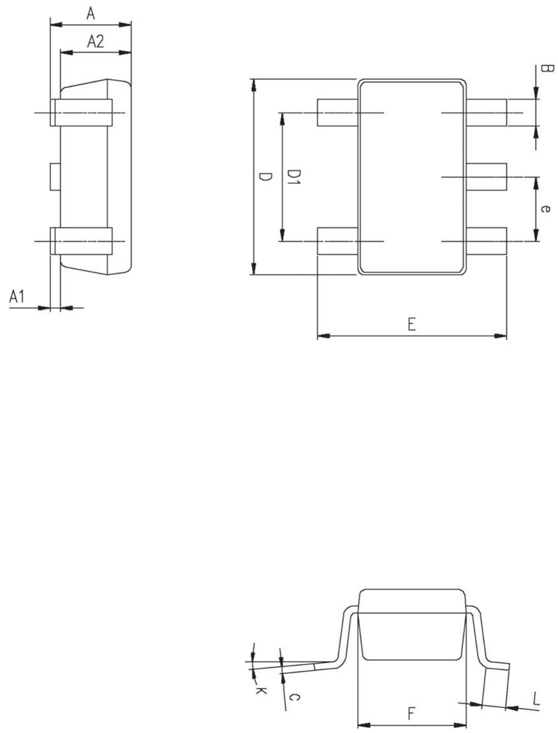


Table 7. SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0 °		10 °	0 °		10 °

5.2 DFN8 2x2 package information

Figure 24. DFN8 2x2 package mechanical drawing

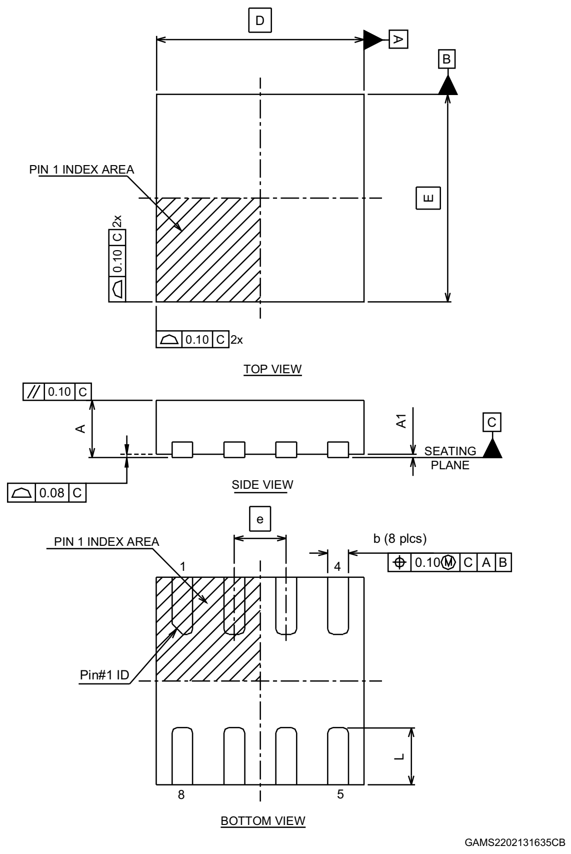


Table 8. DFN8 2x2 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		2.00			0.079	
E		2.00			0.079	
e		0.50			0.020	
L	0.045	0.55	0.65	0.018	0.022	0.026
N	8			8		

5.3 MiniSO8 package information

Figure 25. MiniSO8 package mechanical drawing

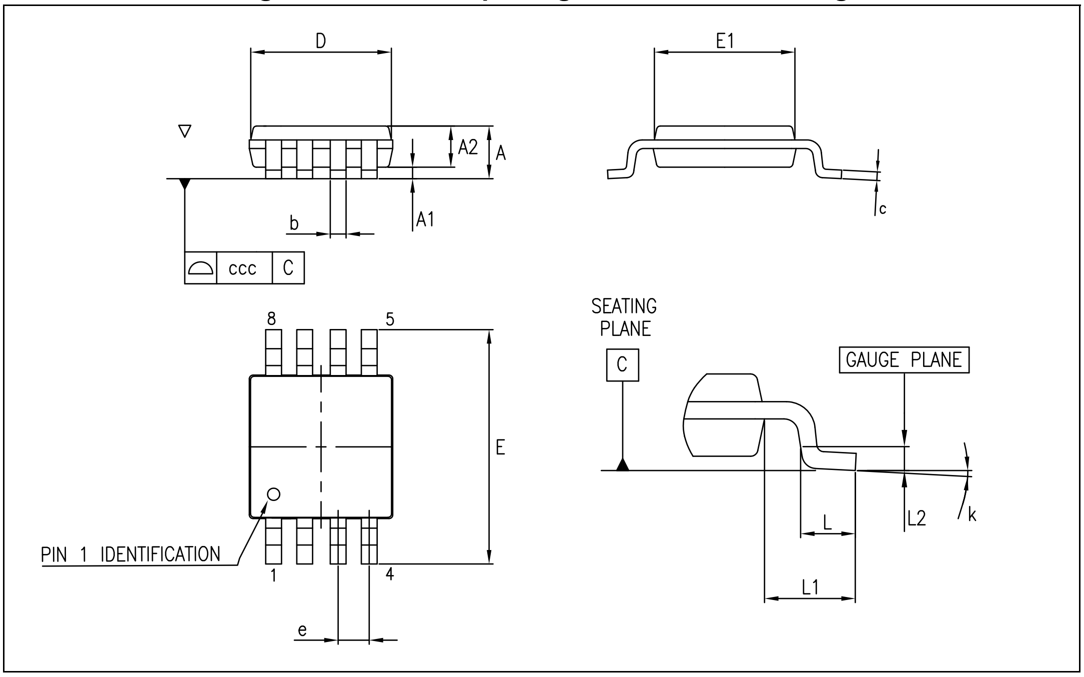


Table 9. MiniSO8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.10			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

5.4 SO8 package information

Figure 26. SO8 package mechanical drawing

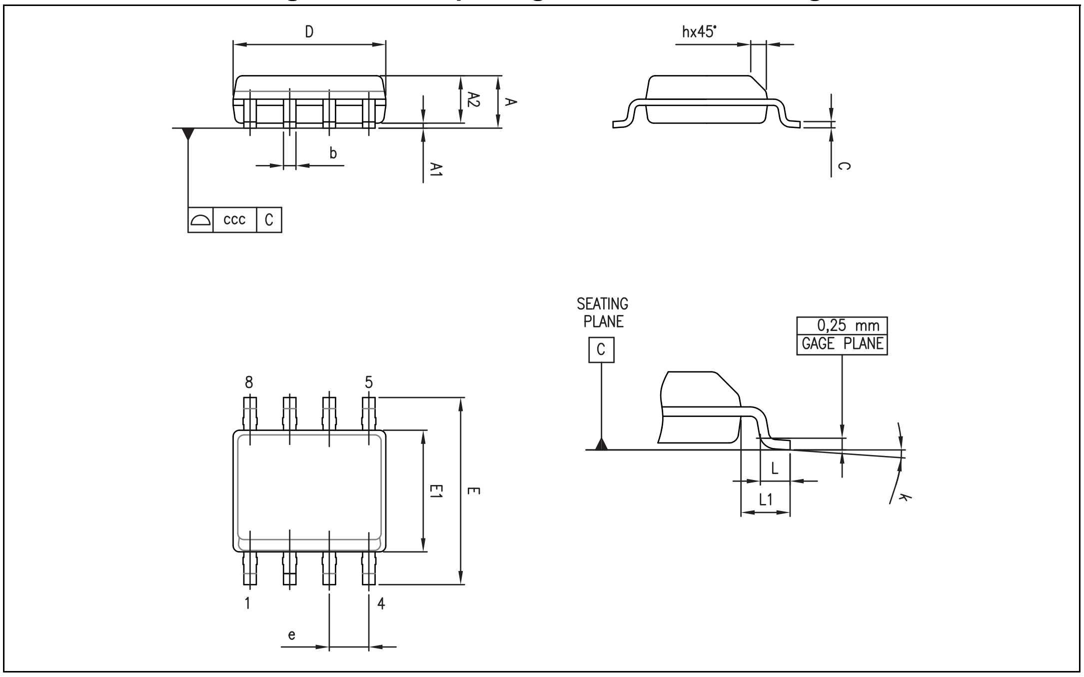


Table 10. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8 °	1 °		8 °
ccc			0.10			0.004

5.5 QFN16 3x3 package information

Figure 27. QFN16 3x3 package mechanical drawing

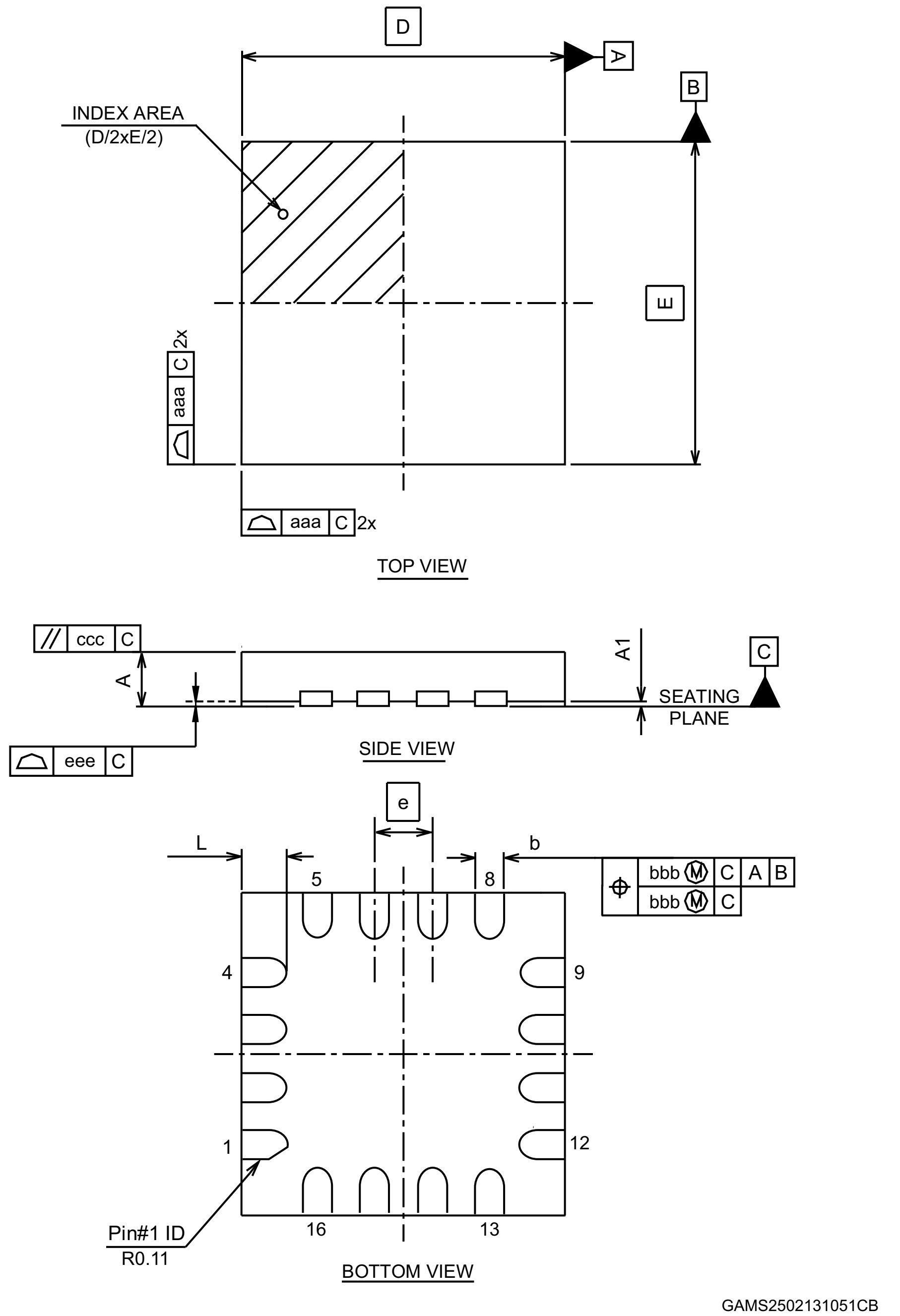


Table 11. QFN16 3x3 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50		0.65	0.020		0.026
A1	0		0.05	0		0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D		3.00			0.118	
E		3.00			0.118	
e		0.50			0.020	
L	0.30		0.50	0.012		0.020
aaa			0.15			0.006
bbb			0.10			0.004
ccc			0.10			0.004
ddd			0.05			0.002
eee			0.08			0.003

5.6 TSSOP14 package information

Figure 28. TSSOP14 package mechanical drawing

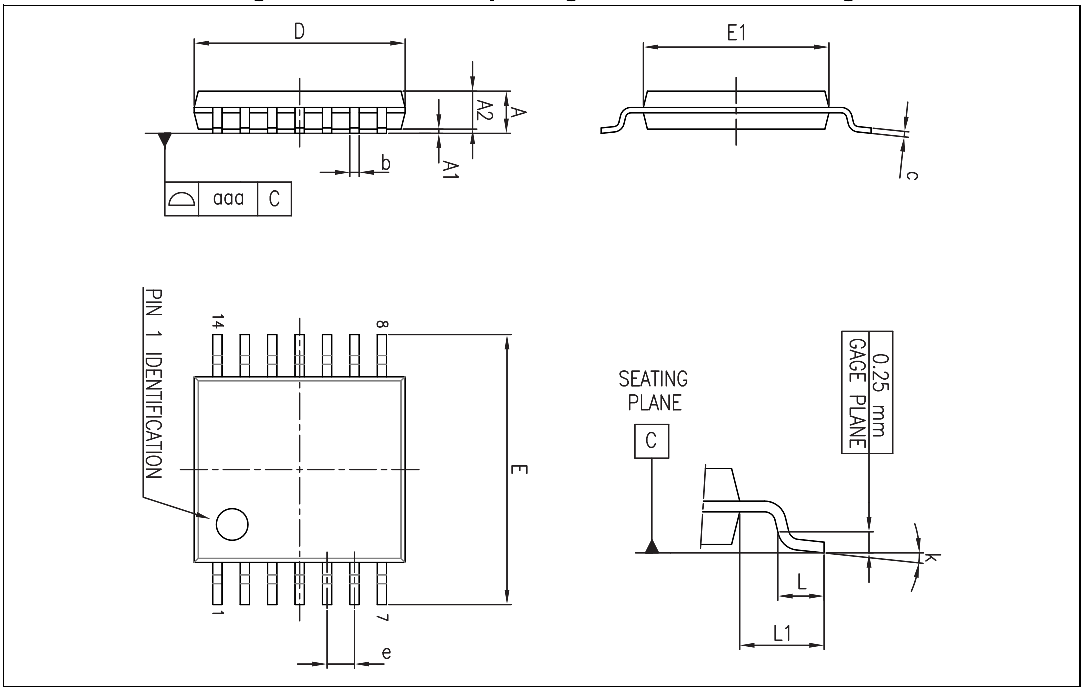


Table 12. TSSOP14 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256 BSC	
L	0.45	0.60	0.75			
L1		1.00				
k	0°		8°	0°		8°
aaa			0.10	0.018	0.024	0.030

6 Ordering information

Table 13. Order codes

Order code	Temperature range	Channel number	Package	Packaging	Marking
TSX561ILT	-40 to 125 °C	1	SOT23-5	Tape and reel	K23
TSX562IQ2T		2	DFN8 2 x 2		
TSX562IST			MiniSO8		
TSX562IDT			SO8		TSX562I
TSX564IQ4T		4	QFN16 3 x 3		K23
TSX564IPT			TSSOP14		TSX564I
TSX561IYLT[1]	-40 to 125 °C automotive grade	1	SOT23-5		K116
TSX562IYST[1]		2	MiniSO8		
TSX562IYDT[2]			SO8		TSX562Y
TSX564IYPT[1]		4	TSSOP14		TSX564IY
TSX561AILT	-40 to 125 °C	1	SOT23-5		K117
TSX562AIST		2	MiniSO8		
TSX562AIDT			SO8		TSX562AI
TSX564AIPT		4	TSSOP14		TSX564AI
TSX561AIYLT[1]	-40 to 125 °C automotive grade	1	SOT23-5		K118
TSX562AIYST[1]		2	MiniSO8		
TSX562AIYDT[2]			SO8		TSX562AY
TSX564AIYPT[1]		4	TSSOP14		TSX564AIY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent.
2. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent are ongoing.

7 Revision history

Table 14. Document revision history

Date	Revision	Changes
06-Jun-2012	1	Initial release.
18-Sep-2012	2	Added TSX562, TSX564, TSX562A, and TSX564A devices. Updated *Features*, *Description*, *Figure 1*, *Table 1* (added DFN8, MiniSO8, QFN16, and TSSOP14 package). Updated *Table 1* (updated ESD MM values). Updated *Table 4* and *Table 5* (added footnotes), *Section 5* (added *Figure 24* to *Figure 28* and *Table 8* to *Table 12*), *Table 13* (added dual and quad devices). Minor corrections throughout document.
23-May-2013	3	Replaced the silhouette, pinout, package diagram, and mechanical data of the DFN8 2x2 and QFN16 3x3 packages. Added *Benefits* and *Related products*. *Table 1*: updated R_{thja} values and added R_{thjc} values for DFN8 2x2 and QFN16 3x3. Updated *Section 4.3*, *Section 4.4*, and *Section 4.6* Replaced *Figure 23: SOT23-5 package mechanical drawing* and *Table 7: SOT23-5 package mechanical data*.
09-Aug-2013	4	Added SO8 package for dual version TSX562 and TSX562A. *Table 2*: updated for SO8 package *Table 13*: added order codes TSX562IDT, TSX562IYDT, TSX562AIDT, TSX562AIYDT; updated automotive grade status.

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