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IRF3515S

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International
IOR Rectifier

SMPS MOSFET

IRF3515S
IRF3515L

HEXFET® Power MOSFET

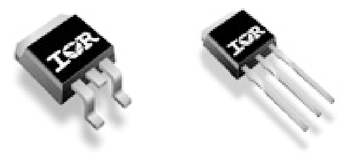
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High speed power switching

V_{DSS}	$R_{DS(on)}$ max	I_D
150V	**0.045Ω**	**41A**

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified (See AN 1001)



D^2Pak IRF3515S   TO-262 IRF3515L

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	41	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	29	
I_{DM}	Pulsed Drain Current ①	164	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	4.3	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Applicable Off Line SMPS Topologies

- Telcom 48V input DC/DC Active Clamp Reset Forward Converter

Notes ① through ⑤ are on page 10

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.21	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.045	Ω	V_{GS} = 10V, I_D = 25A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	——	4.5	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 150V, V_{GS} = 0V
		——	——	250		V_{DS} = 120V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	15	——	——	S	V_{DS} = 50V, I_D = 25A
Q_g	Total Gate Charge	——	——	107		I_D = 25A
Q_{gs}	Gate-to-Source Charge	——	——	23	nC	V_{DS} = 120V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	65		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	17	——		V_{DD} = 75V
t_r	Rise Time	——	120	——	ns	I_D = 25A
$t_{d(off)}$	Turn-Off Delay Time	——	34	——		R_G = 2.5Ω
t_f	Fall Time	——	63	——		R_D = 3.0Ω,See Fig. 10 ④
C_{iss}	Input Capacitance	——	2260	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	530	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	170	——	pF	f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	3330	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	230	——		V_{GS} = 0V, V_{DS} = 120V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	280	——		V_{GS} = 0V, V_{DS} = 0V to 120V ⑤

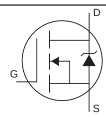
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	670	mJ
I_{AR}	Avalanche Current①	——	25	A
E_{AR}	Repetitive Avalanche Energy①	——	20	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	——	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	41	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	164		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	200	300	ns	T_J = 25°C, I_F = 25A
Q_{rr}	Reverse RecoveryCharge	——	1.6	2.4	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

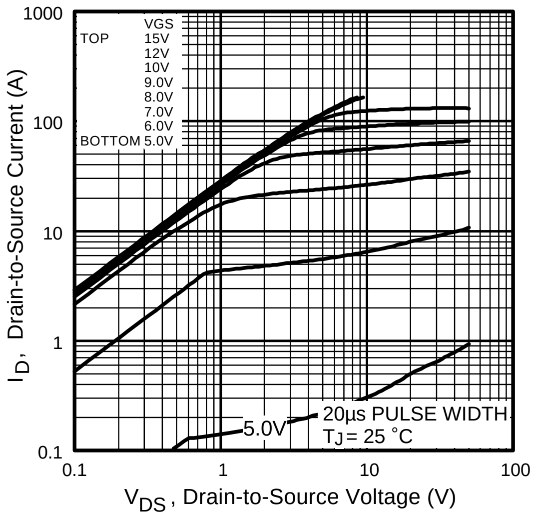


Fig 1. Typical Output Characteristics

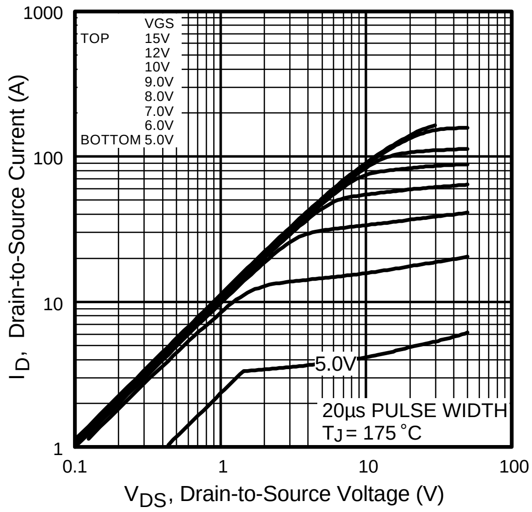


Fig 2. Typical Output Characteristics

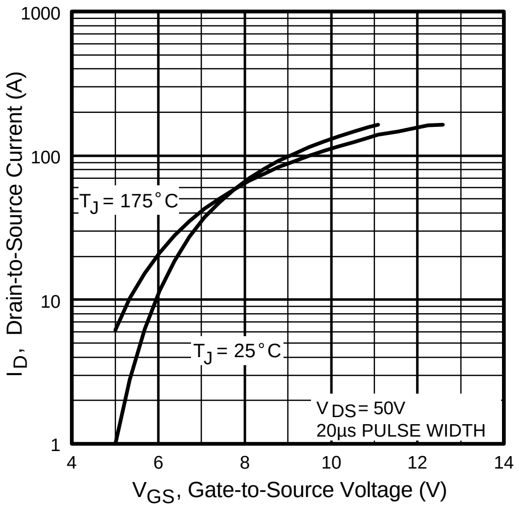


Fig 3. Typical Transfer Characteristics

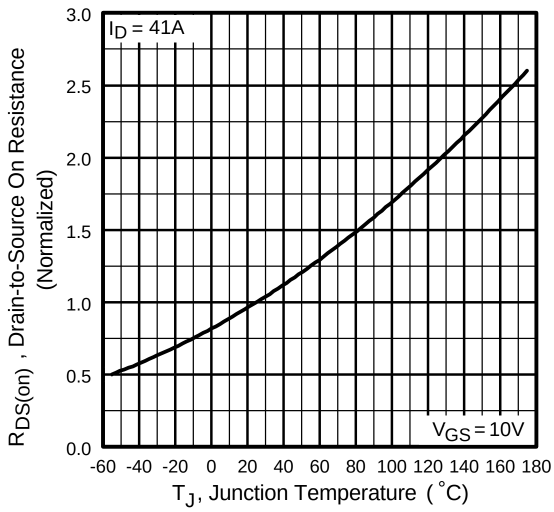


Fig 4. Normalized On-Resistance Vs. Temperature

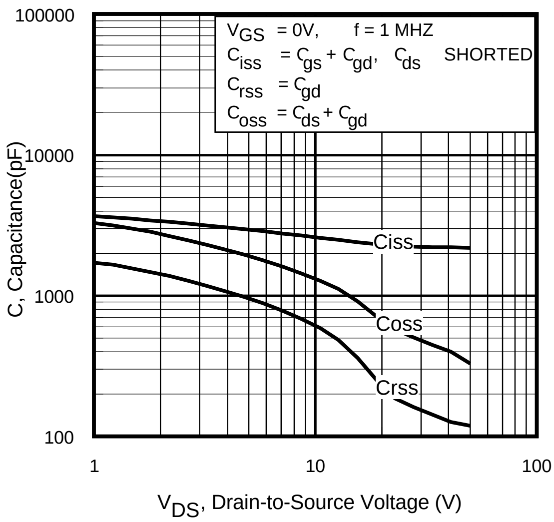


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

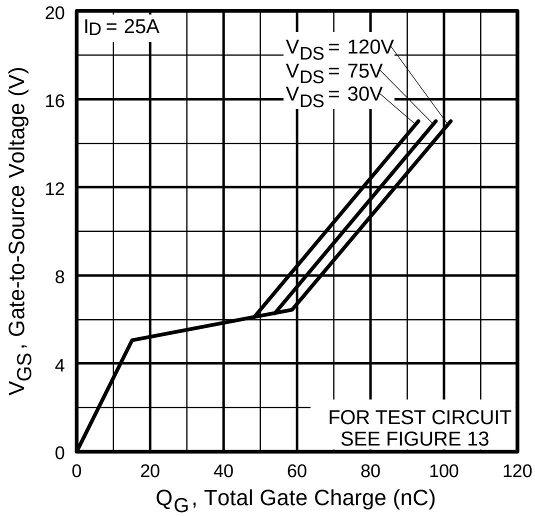


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

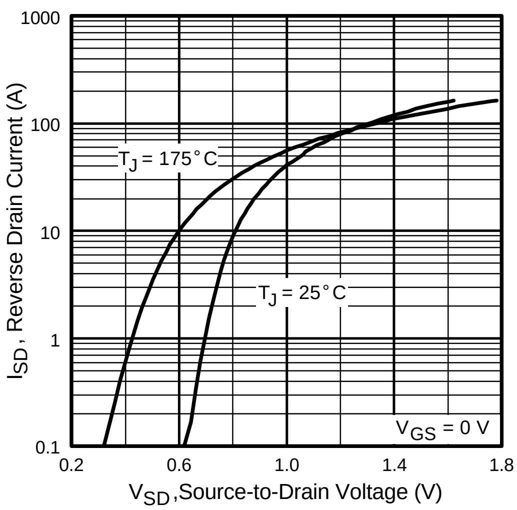


Fig 7. Typical Source-Drain Diode Forward Voltage

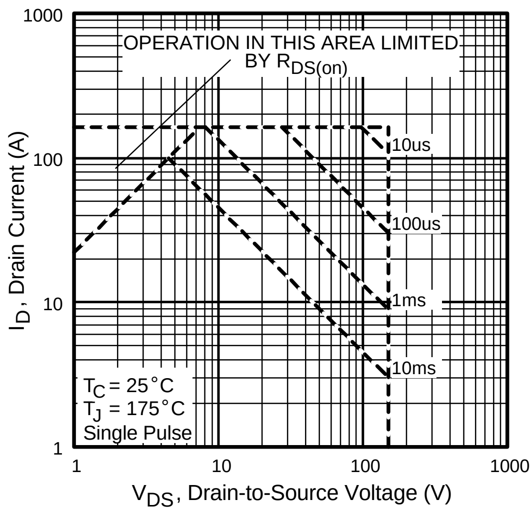


Fig 8. Maximum Safe Operating Area

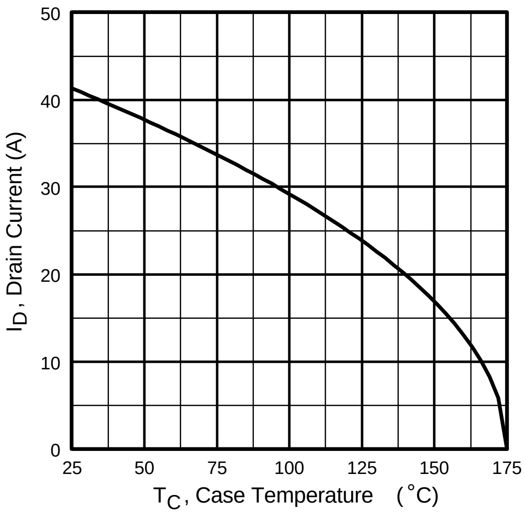


Fig 9. Maximum Drain Current Vs. Case Temperature

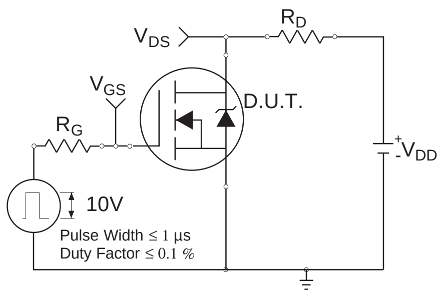


Fig 10a. Switching Time Test Circuit

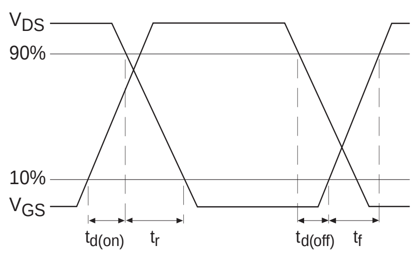


Fig 10b. Switching Time Waveforms

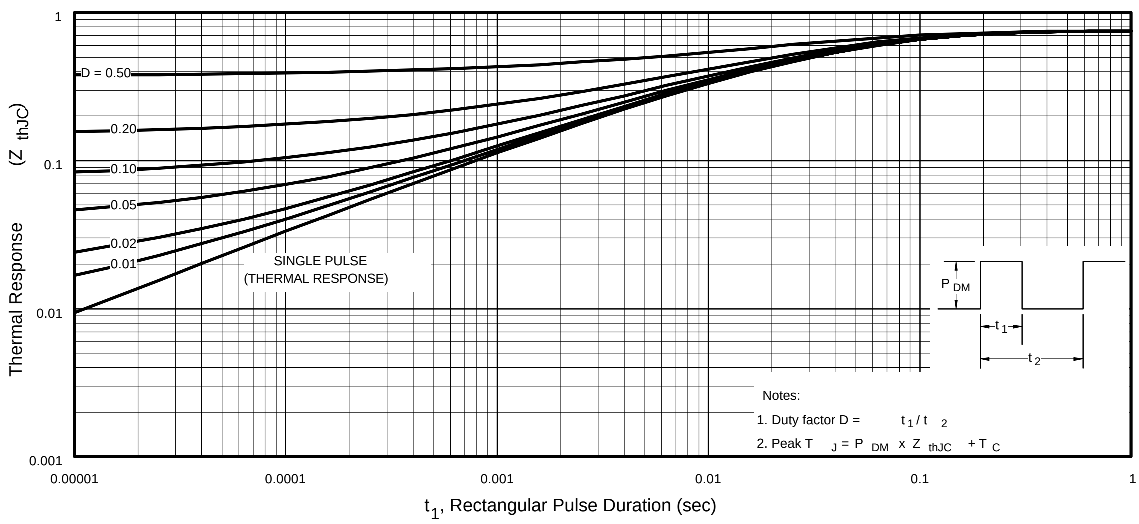


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

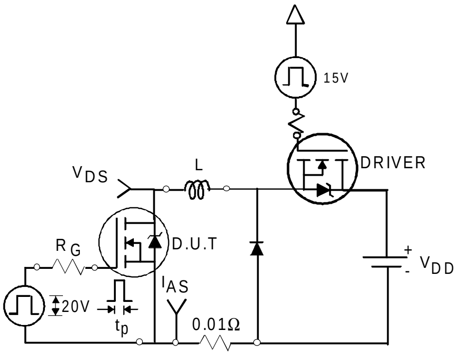


Fig 12a. Unclamped Inductive Test Circuit

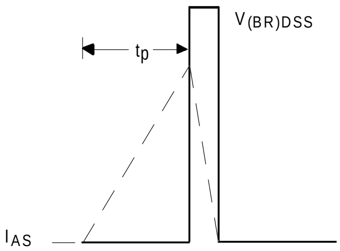


Fig 12b. Unclamped Inductive Waveforms

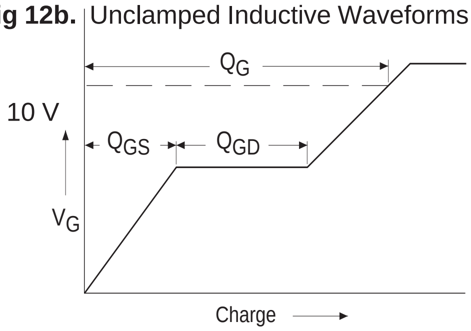


Fig 13a. Basic Gate Charge Waveform

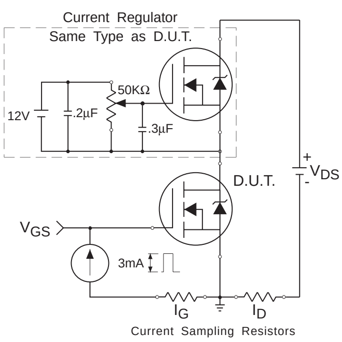


Fig 13b. Gate Charge Test Circuit

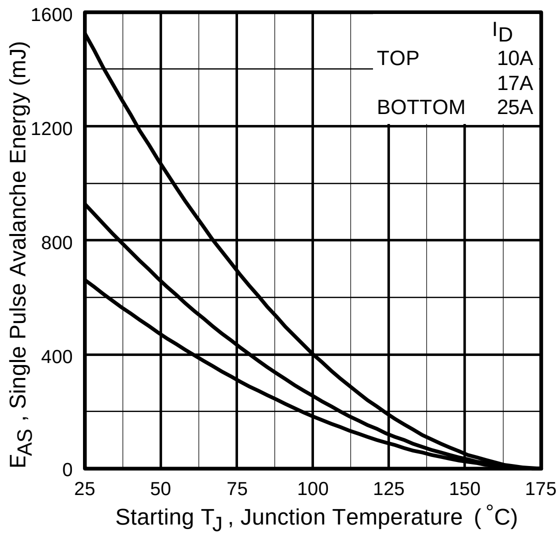
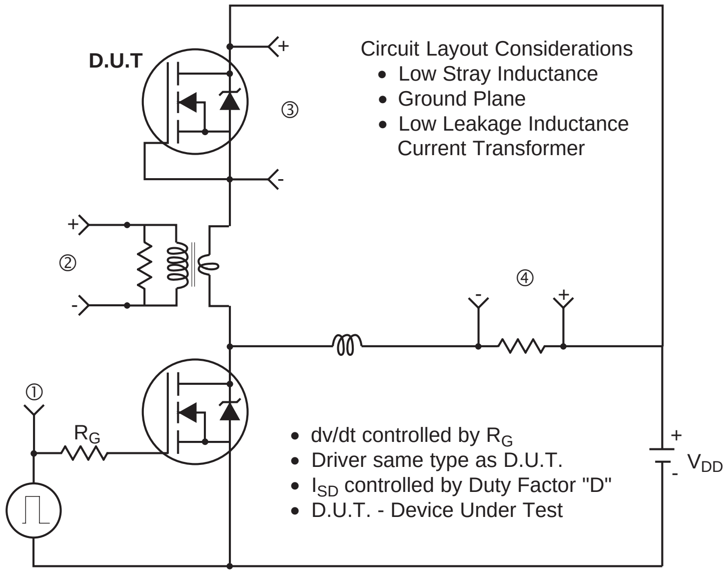
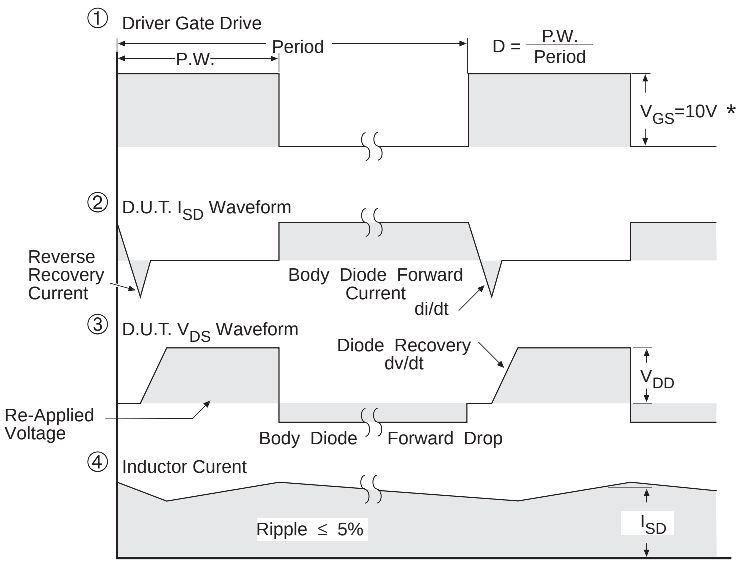


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Peak Diode Recovery dv/dt Test Circuit

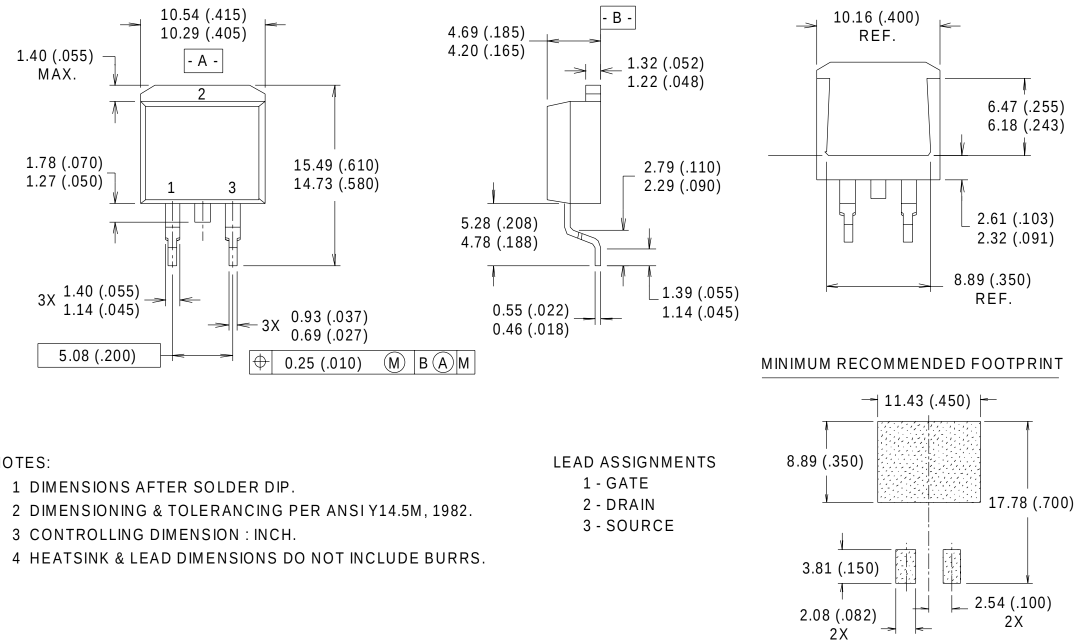




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETS

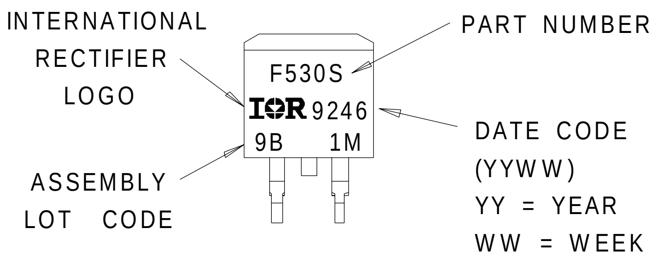
D2Pak Package Outline



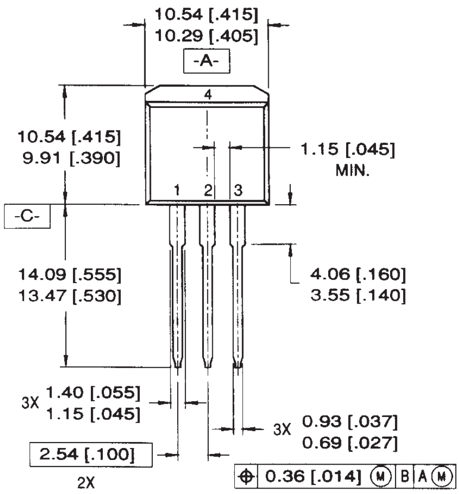
NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

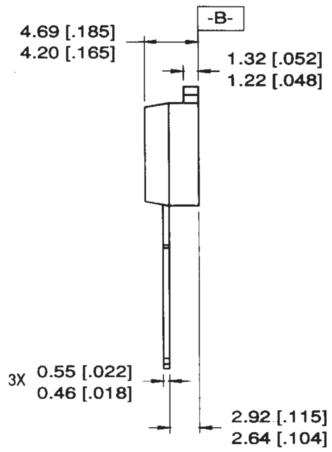
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

D2Pak Part Marking Information



TO-262 Package Outline





LEAD ASSIGNMENTS

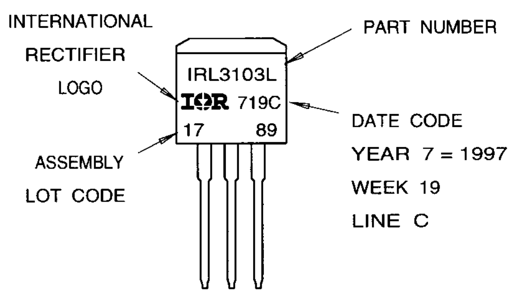
1 = GATE
2 = DRAIN
3 = SOURCE
4 = DRAIN

NOTES:

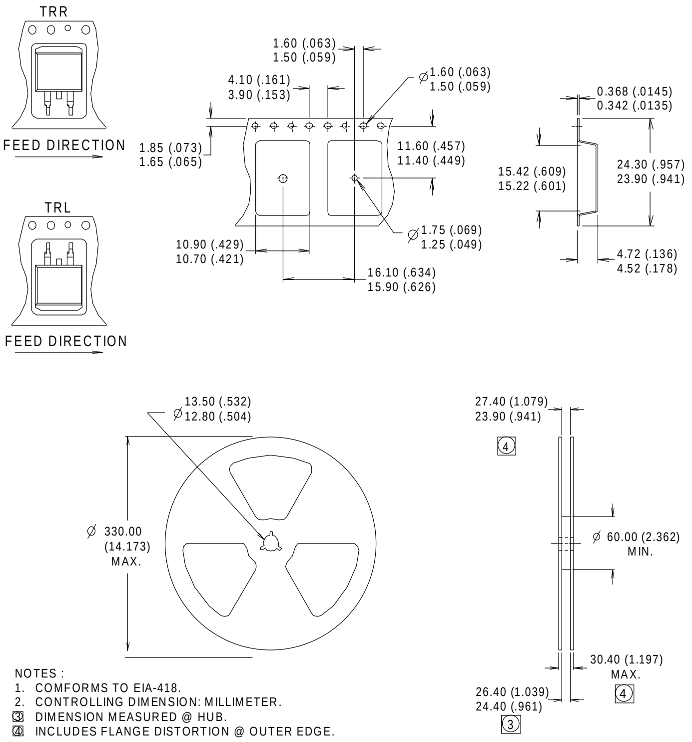
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D^2Pak Tape & Reel Information



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25°C$, $L = 2.2mH$ $R_G = 25\Omega$, $I_{AS} = 25A$. (See Figure 12)

③ $I_{SD} \leq 5.0A$, $di/dt \leq 330A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

* When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.

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Data and specifications subject to change without notice. 10/99

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/