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[International Rectifier \(Infineon Technologies Americas Corp.\)  
IRF6215S](#)

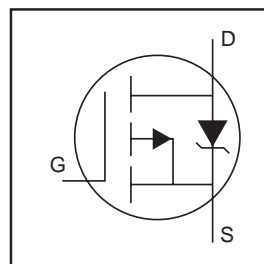
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# IRF6215S/L

HEXFET® Power MOSFET

- Advanced Process Technology
- Surface Mount (IRF6215S)
- Low-profile through-hole (IRF6215L)
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated



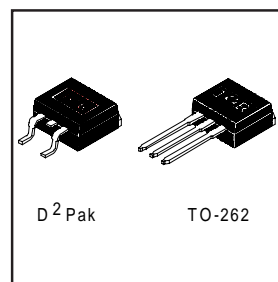
$V_{DSS} = -150V$
$R_{DS(on)} = 0.29\Omega$
$I_D = -13A$

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF6215L) is available for low-profile applications.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$ ⑤	-13	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$ ⑤	-9.0	
$I_{DM}$	Pulsed Drain Current ①⑤	-44	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②⑤	310	mJ
$I_{AR}$	Avalanche Current①	-6.6	A
$E_{AR}$	Repetitive Avalanche Energy①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	-5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mounted,steady-state)**	—	40	

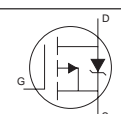
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## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-150	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	-0.20	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1mA <sup>⑤</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.29	Ω	V <sub>GS</sub> = -10V, I <sub>D</sub> = -6.6A <sup>④</sup>
		—	—	0.58		V <sub>GS</sub> = -10V, I <sub>D</sub> = -6.6A <sup>④</sup> T <sub>J</sub> = 150°C
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
g <sub>fs</sub>	Forward Transconductance	3.6	—	—	S	V <sub>DS</sub> = -25V, I <sub>D</sub> = -6.6A <sup>⑤</sup>
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-25	μA	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V
		—	—	-250		V <sub>DS</sub> = 120V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = 20V
Q <sub>g</sub>	Total Gate Charge	—	—	66	nC	I <sub>D</sub> = -6.6A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	8.1		V <sub>DS</sub> = -120V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	35		V <sub>GS</sub> = -10V, See Fig. 6 and 13 <sup>④⑤</sup>
t <sub>d(on)</sub>	Turn-On Delay Time	—	14	—		V <sub>DD</sub> = -75V
t <sub>r</sub>	Rise Time	—	36	—	V <sub>GS</sub> = -10V, See Fig. 6 and 13 <sup>④⑤</sup>	I <sub>D</sub> = -6.6A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	53	—		R <sub>G</sub> = 6.8Ω
t <sub>f</sub>	Fall Time	—	37	—		R <sub>D</sub> = 12Ω, See Fig. 10 <sup>④⑤</sup>
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		nH
C <sub>iss</sub>	Input Capacitance	—	860	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	220	—		V <sub>DS</sub> = -25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz, See Fig. 5 <sup>⑤</sup>

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	-44		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.6	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -6.6A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	160	240	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -6.6A
Q <sub>rr</sub>	Reverse Recovery Charge	—	1.2	1.7	μC	di/dt = -100A/μs <sup>④⑤</sup>
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting T<sub>J</sub> = 25°C, L = 14mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = -6.6A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ -6.6A, di/dt ≤ -620A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Uses IRF6215 data and test conditions

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material ).

For recommended footprint and soldering techniques refer to application note #AN-994.

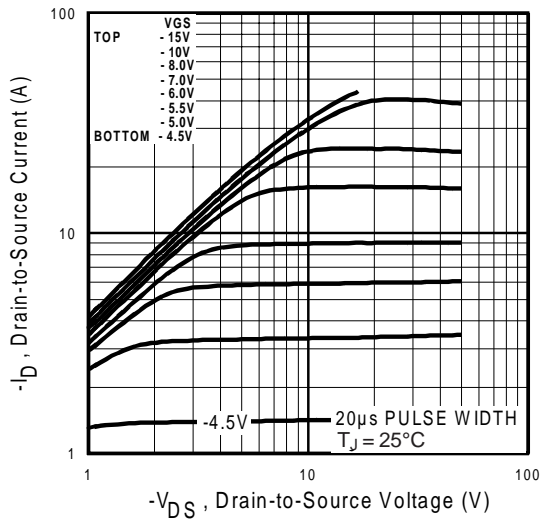


Fig 1. Typical Output Characteristics

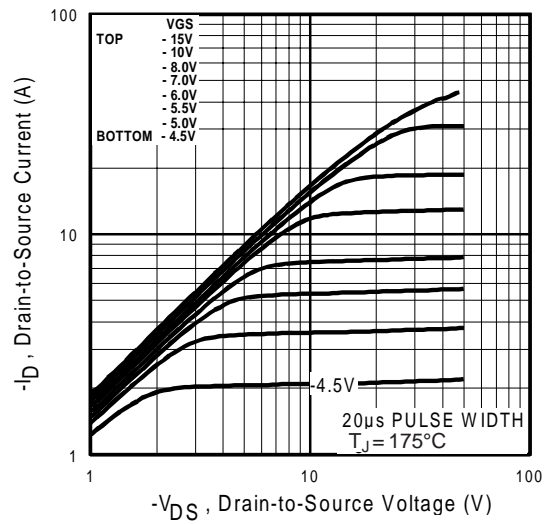


Fig 2. Typical Output Characteristics

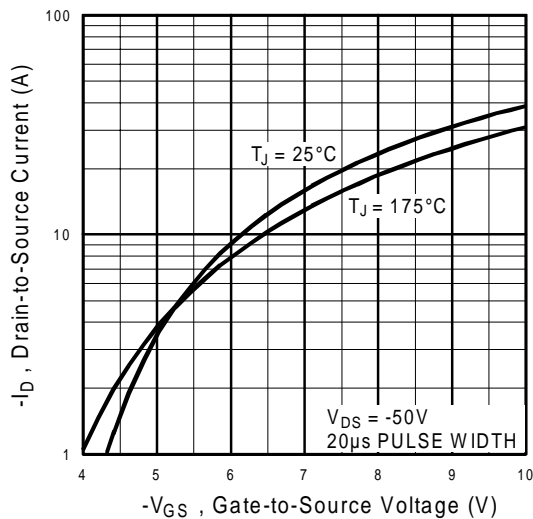


Fig 3. Typical Transfer Characteristics

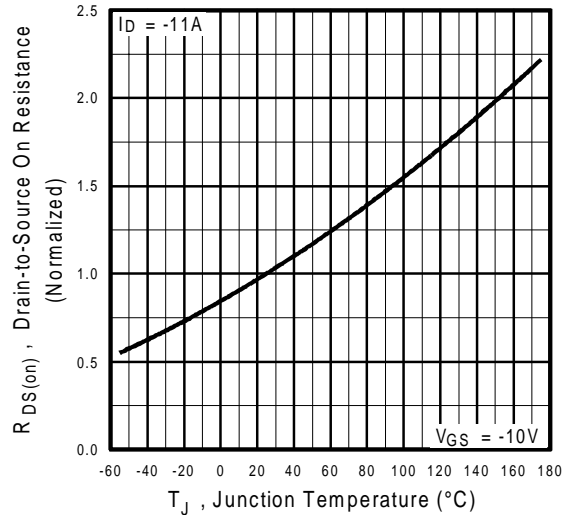
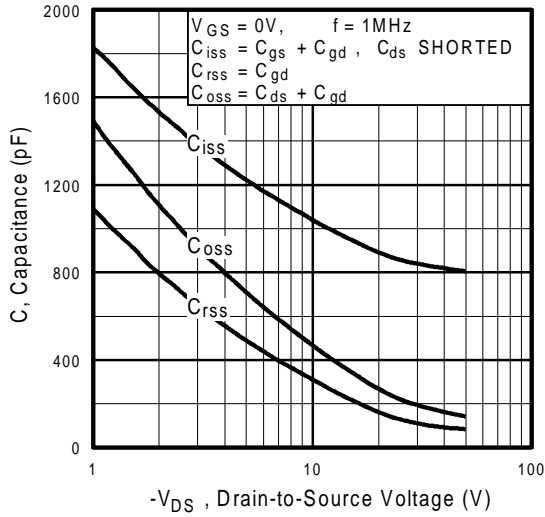


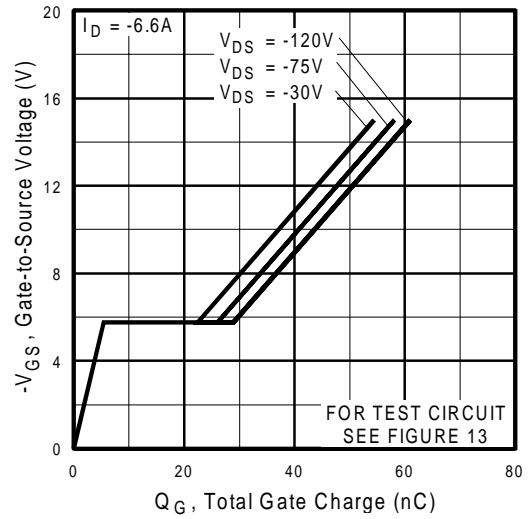
Fig 4. Normalized On-Resistance Vs. Temperature

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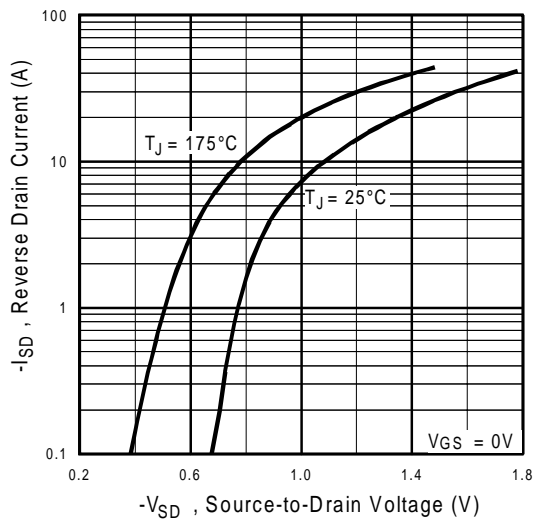
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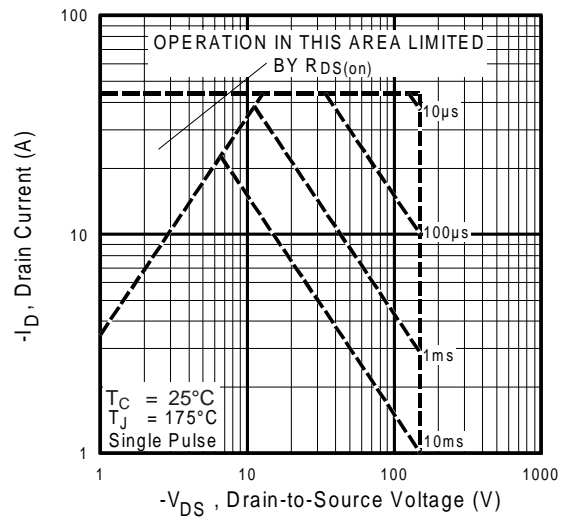
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



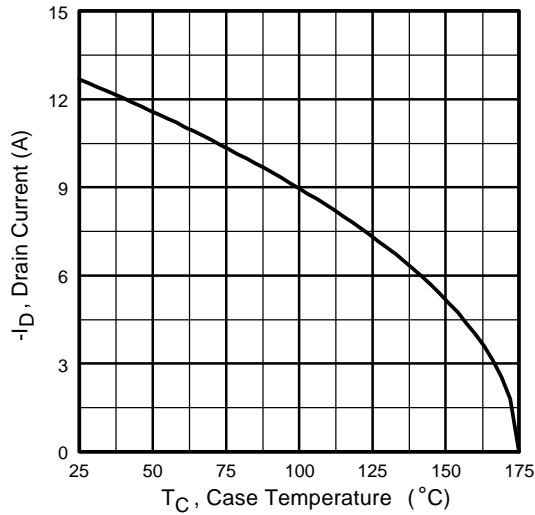
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



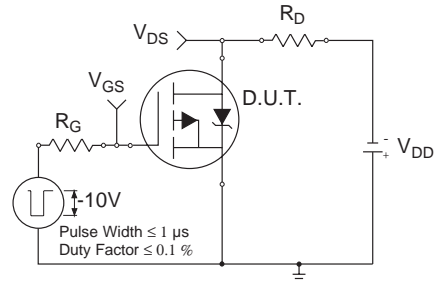
**Fig 7.** Typical Source-Drain Diode Forward Voltage



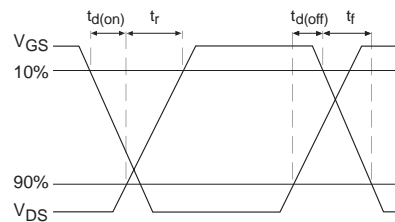
**Fig 8.** Maximum Safe Operating Area



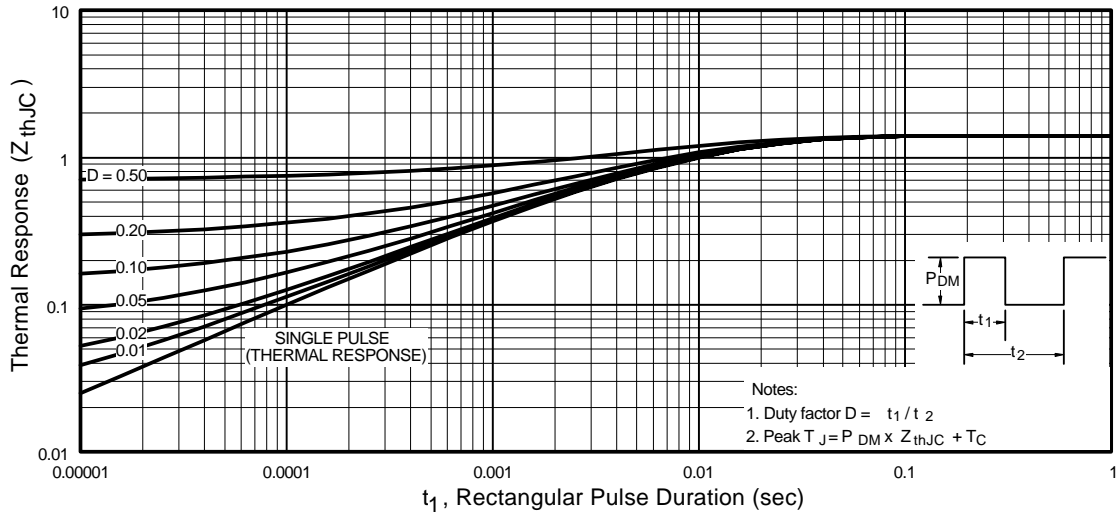
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



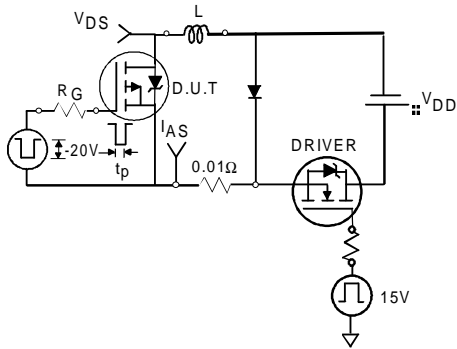
**Fig 10b.** Switching Time Waveforms



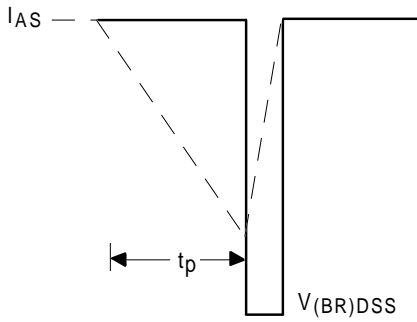
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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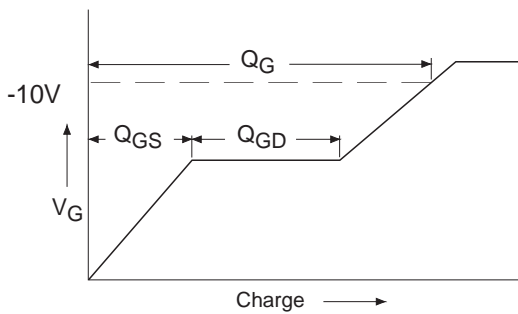
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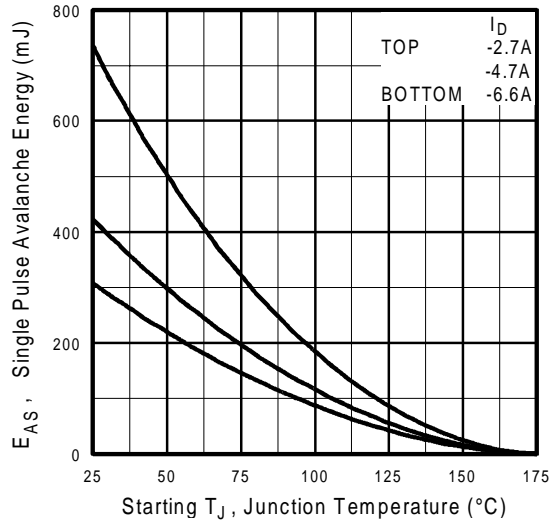
**Fig 12a.** Unclamped Inductive Test Circuit



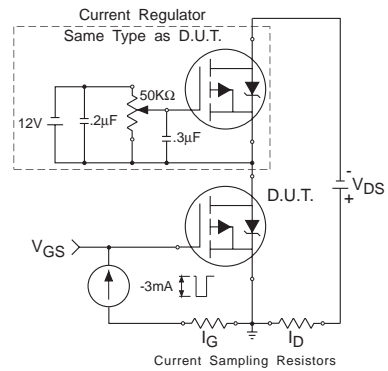
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

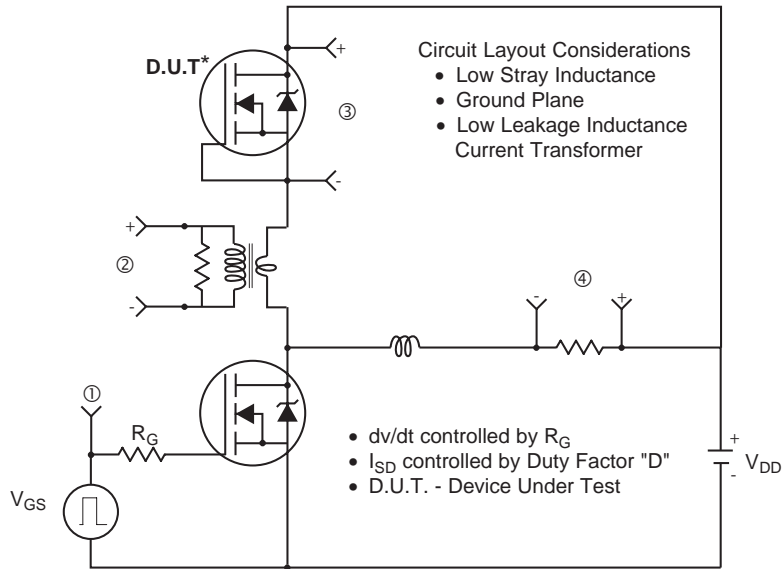


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

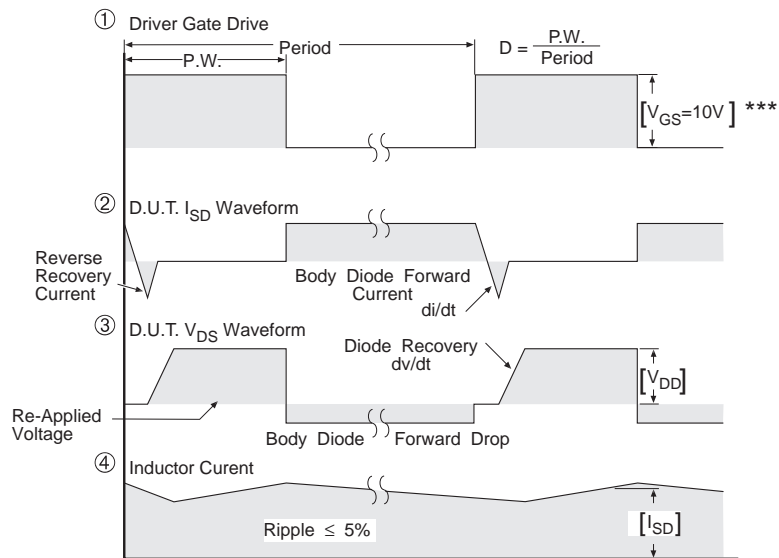


**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



\* Reverse Polarity of D.U.T. for P-Channel



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

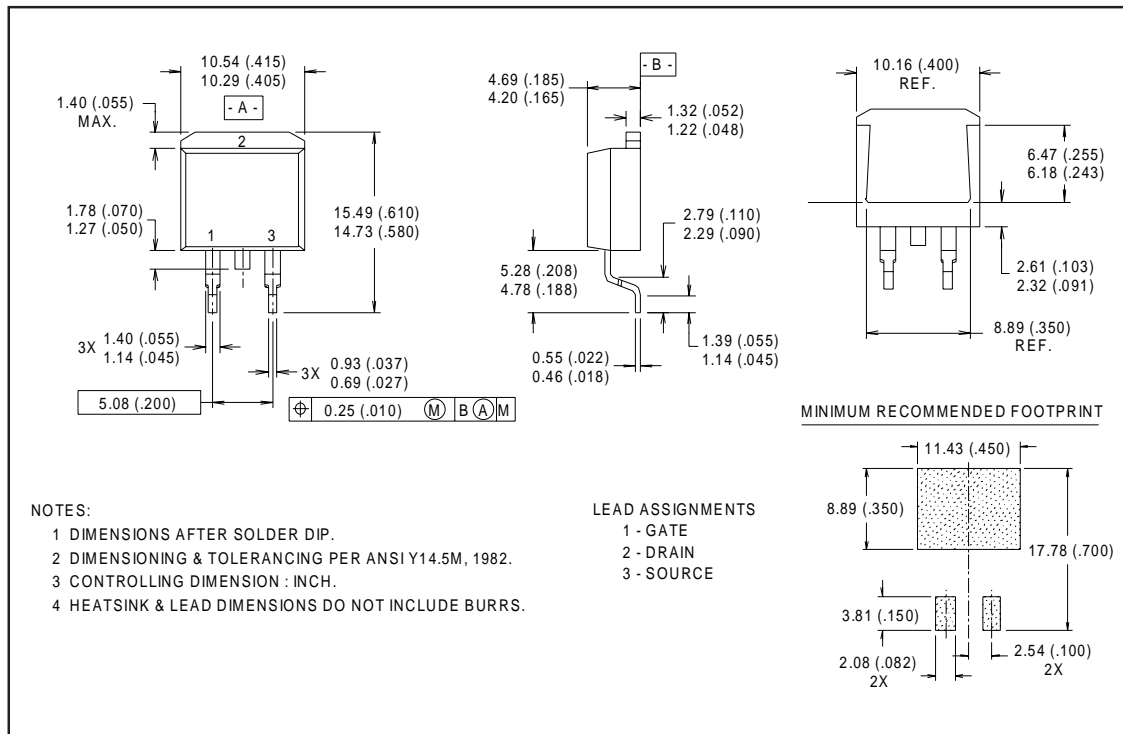
**Fig 14.** For P-Channel HEXFETS



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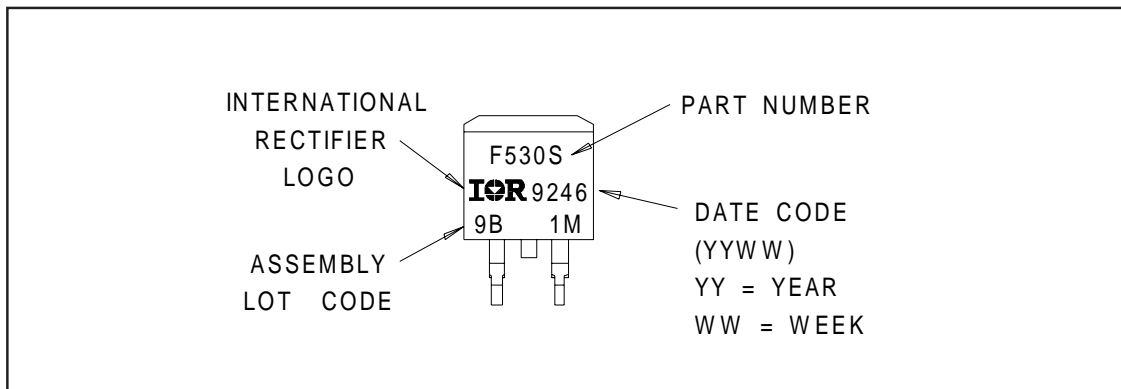
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## D<sup>2</sup>Pak Package Outline



## Part Marking Information

D<sup>2</sup>Pak

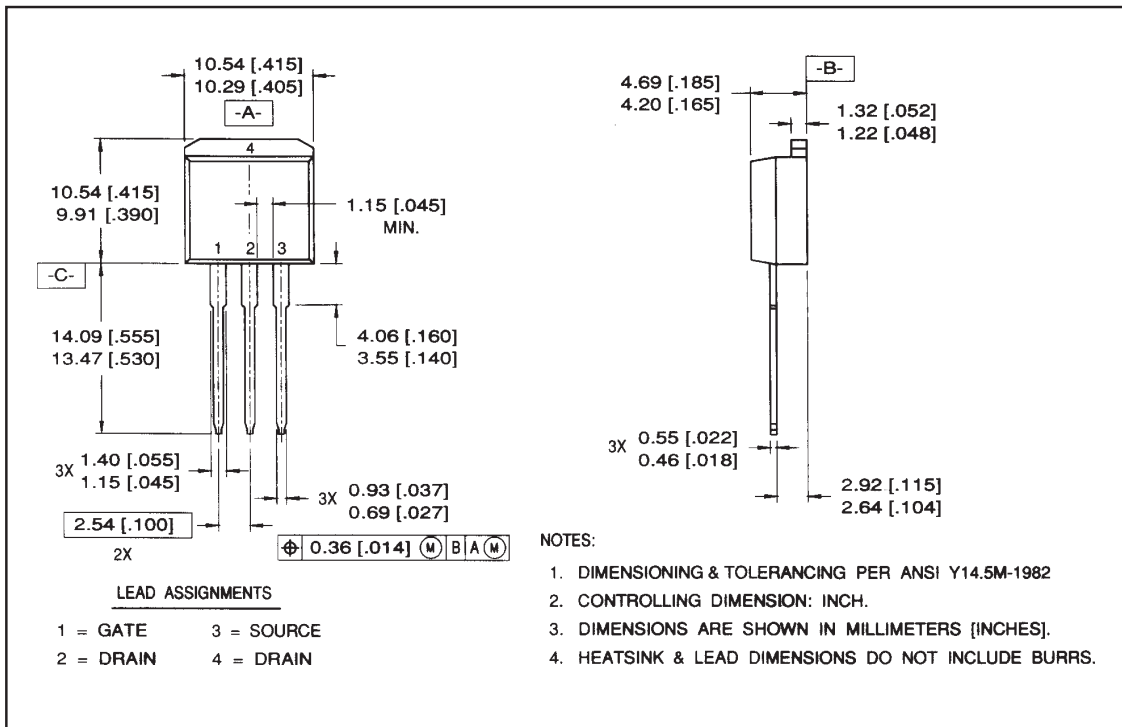


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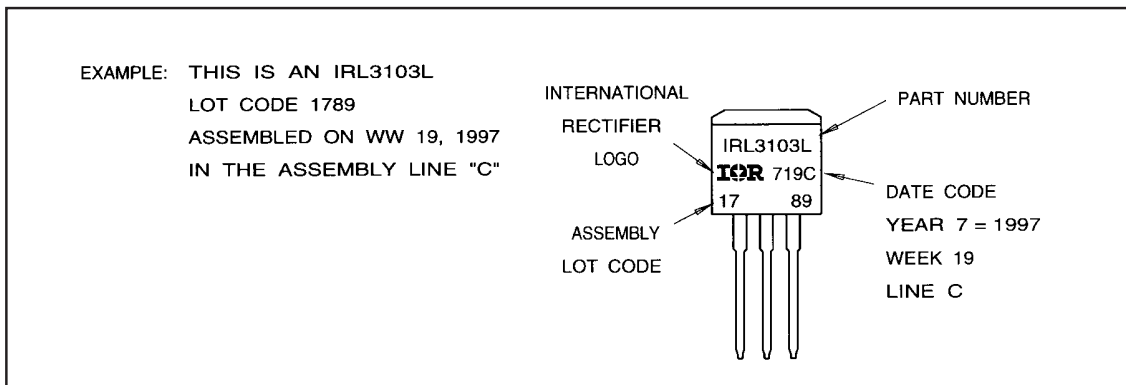
**Package Outline**

TO-262 Outline



**Part Marking Information**

TO-262

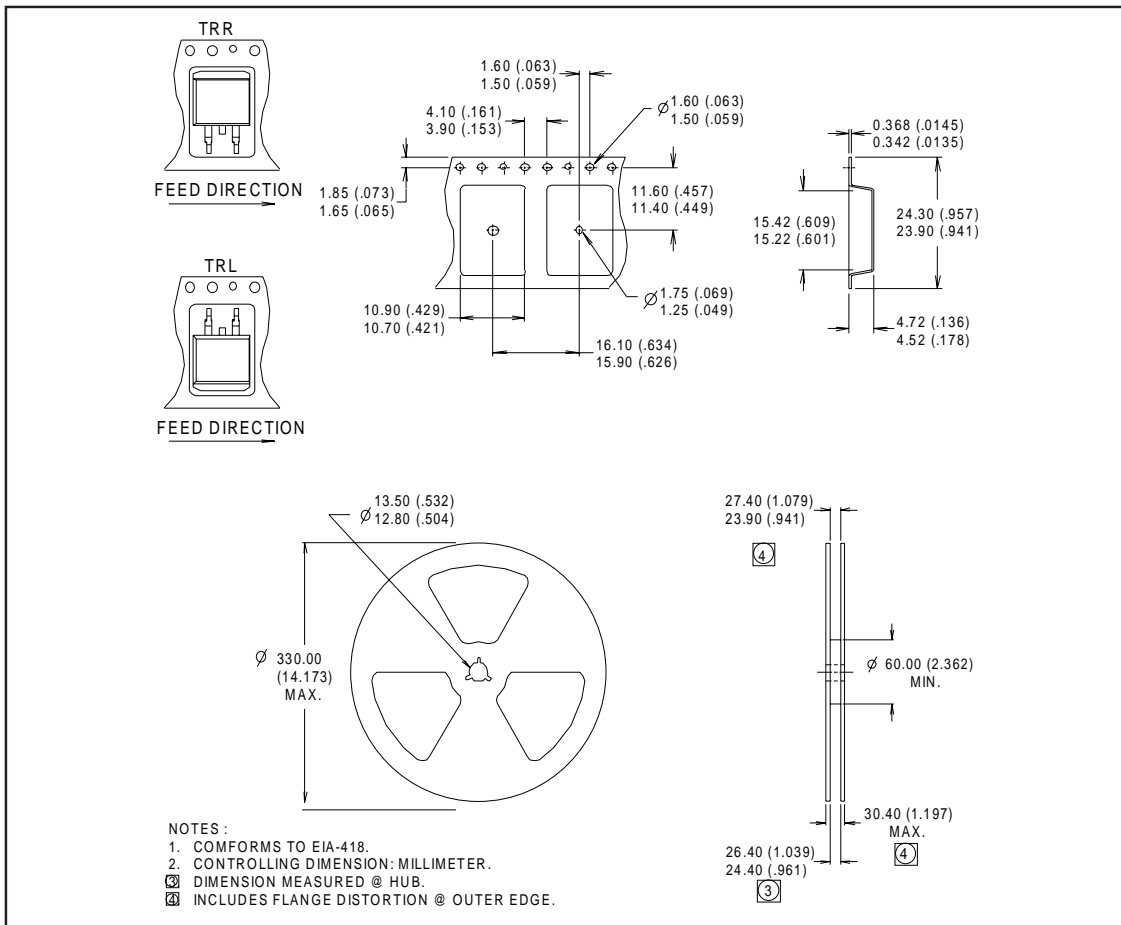


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## Tape & Reel Information

D<sup>2</sup>Pak



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