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PSMN1R8-40YLC

N-channel 40 V 1.8 mΩ logic level MOSFET in LPAK using NextPower technology

22 August 2012

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads
- Ultra low R_{dson} and low parasitic inductance

1.3 Applications

- DC-to-DC converters
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	-	40	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 1	[1]	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2	-	-	272	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 12	-	1.8	2.1	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12	-	1.5	1.8	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 25 A; V _{DS} = 20 V; Fig. 15 ; Fig. 14	-	10.9	-	nC



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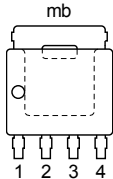
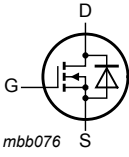
N-channel 40 V 1.8 mΩ logic level MOSFET in LPAK using NextPower technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(\text{tot})}$	total gate charge	$V_{GS} = 4.5 \text{ V}$; $I_D = 25 \text{ A}$; $V_{DS} = 20 \text{ V}$; Fig. 15 ; Fig. 14	-	45	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R8-40YLC	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$25 \text{ °C} \leq T_j \leq 175 \text{ °C}$	-	40	V	
V_{DGR}	drain-gate voltage	$25 \text{ °C} \leq T_j \leq 175 \text{ °C}$; $R_{GS} = 20 \text{ k}\Omega$	-	40	V	
V_{GS}	gate-source voltage		-20	20	V	
I_D	drain current	$V_{GS} = 10 \text{ V}$; $T_{mb} = 25 \text{ °C}$; Fig. 1	[1]	-	100	A
		$V_{GS} = 10 \text{ V}$; $T_{mb} = 100 \text{ °C}$; Fig. 1	[1]	-	100	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10 \text{ }\mu\text{s}$; $T_{mb} = 25 \text{ °C}$; Fig. 4	-	1128	A	
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ °C}$; Fig. 2	-	272	W	
T_{stg}	storage temperature		-55	175	°C	
T_j	junction temperature		-55	175	°C	
$T_{sld(M)}$	peak soldering temperature		-	260	°C	

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Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	890	-	V
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	1128	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped; Fig. 3	-	248	mJ

[1] Continuous current is limited by package.

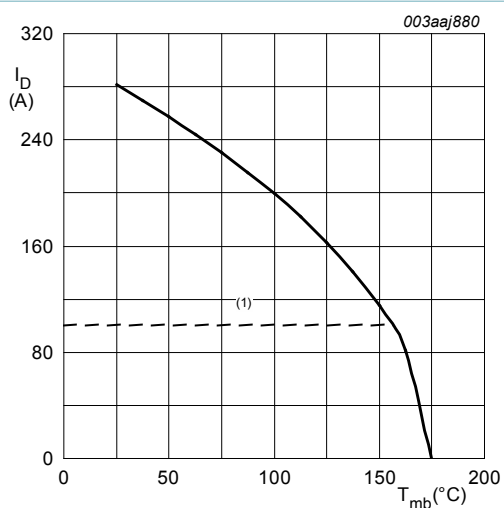


Fig. 1. Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10\text{ V}$
 (1) Capped at 100 A due to package.

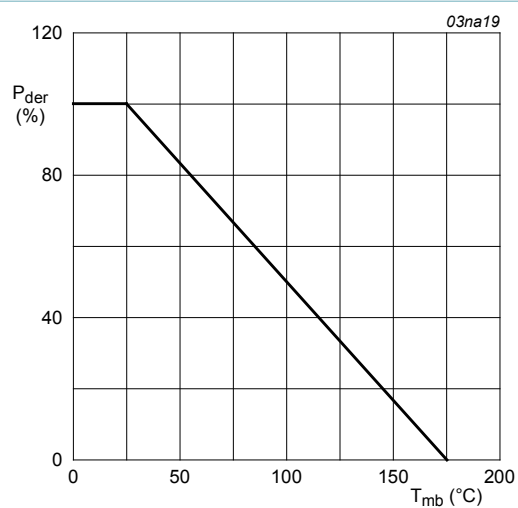


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ °C})}} \times 100\%$$

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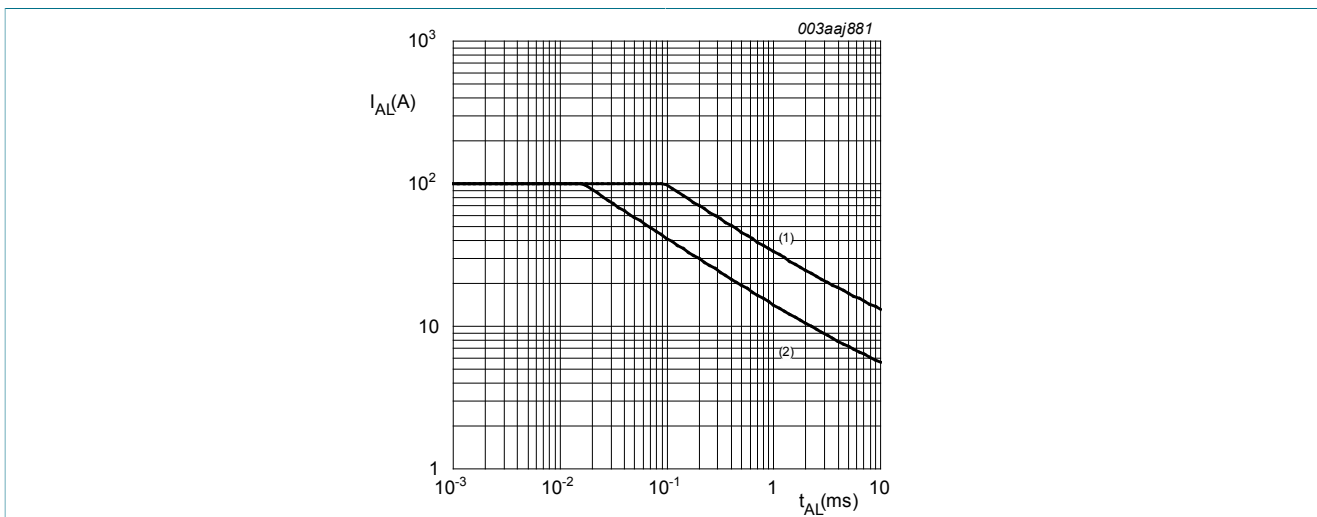


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (init)} = 25^{\circ}C$; (2) $T_{j (init)} = 100^{\circ}C$

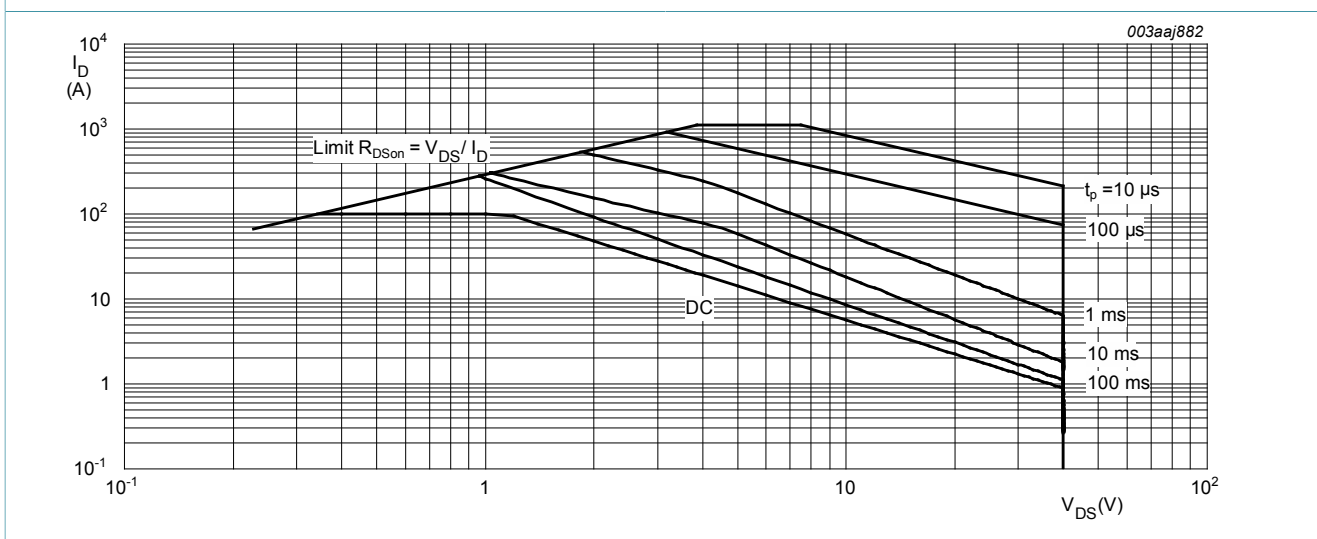


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.55	K/W

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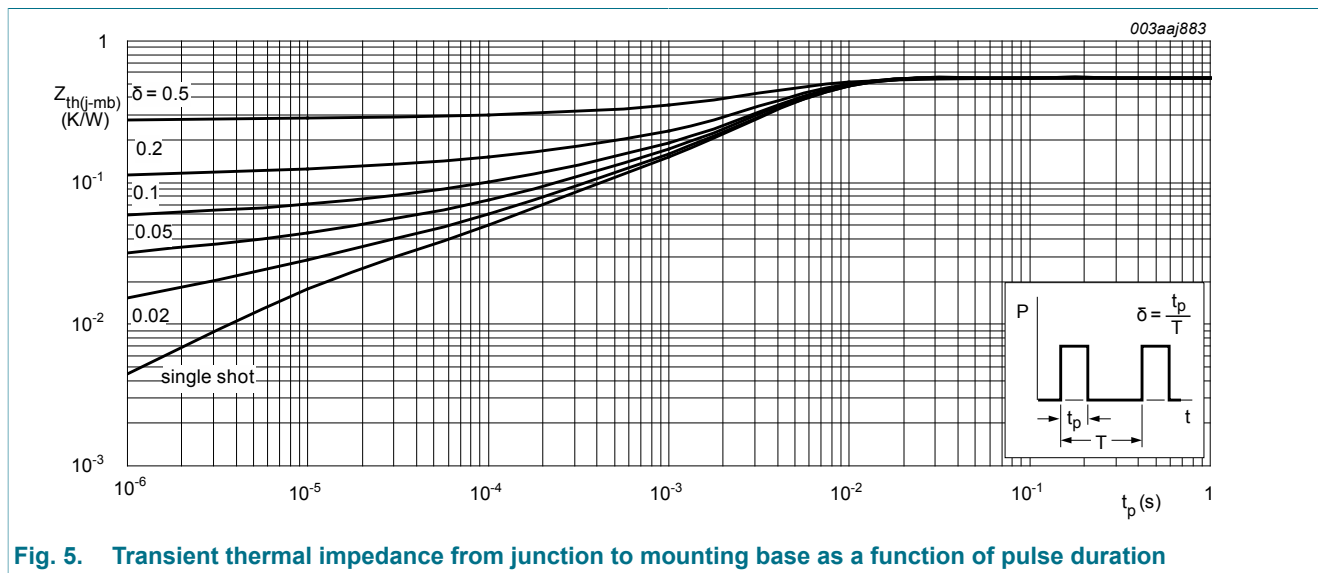


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	40	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; Fig. 10	1.05	1.45	1.95	V
		I _D = 10 mA; V _{DS} = V _{GS} ; T _J = 150 °C; Fig. 11	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; Fig. 11	-	-	2.25	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _J = 25 °C	-	-	1	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _J = 150 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _J = 25 °C	-	-	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _J = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _J = 25 °C; Fig. 12	-	1.8	2.1	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _J = 150 °C; Fig. 12; Fig. 13	-	-	3.6	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12	-	1.5	1.8	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 150 °C; Fig. 12; Fig. 13	-	-	3.25	mΩ

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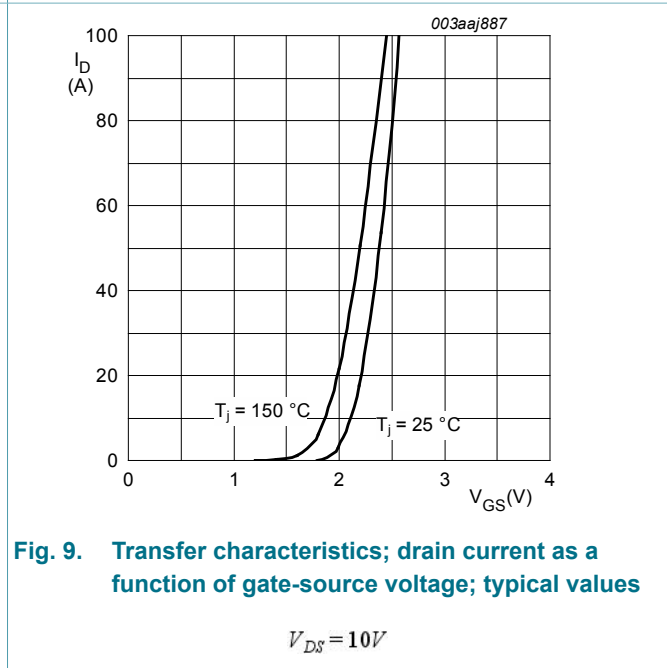
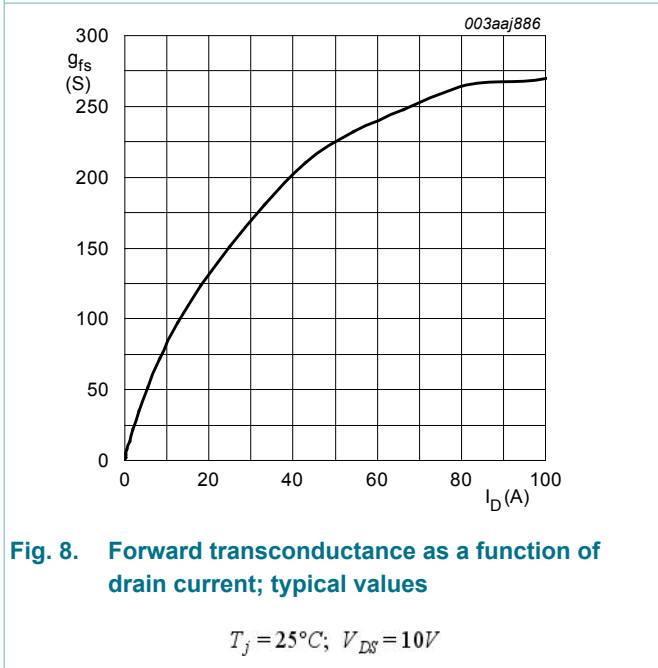
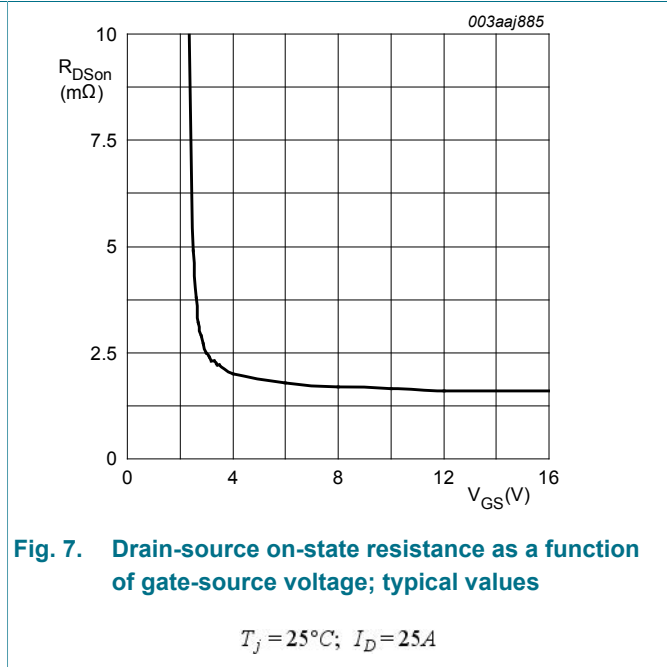
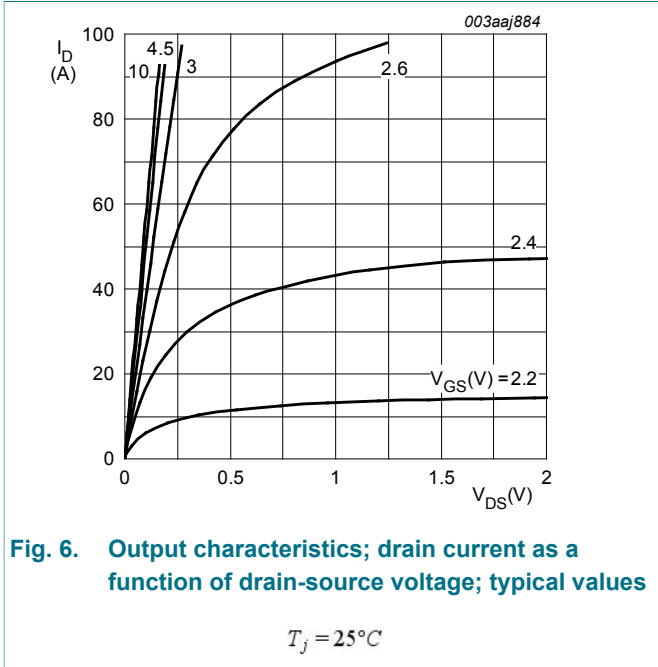
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_G	gate resistance	$f = 1 \text{ MHz}$	0.5	1	2	Ω
Dynamic characteristics						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14 ; Fig. 15	-	96	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 15 ; Fig. 14	-	45	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	88	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 15 ; Fig. 14	-	15.5	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge		-	8.4	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge		-	7.1	-	nC
Q_{GD}	gate-drain charge		-	10.9	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V};$ Fig. 15 ; Fig. 14	-	2.7	-	V
C_{iss}	input capacitance	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 16	-	6680	-	pF
C_{oss}	output capacitance		-	825	-	pF
C_{rss}	reverse transfer capacitance		-	310	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 20 \text{ V}; R_L = 0.8 \text{ } \Omega; V_{GS} = 4.5 \text{ V};$ $R_{G(\text{ext})} = 5 \text{ } \Omega$	-	32.2	-	ns
t_r	rise time		-	37	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	62.5	-	ns
t_f	fall time		-	31.7	-	ns
Q_{oss}	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C}$	-	30	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 17	-	0.77	1.1	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V}$	-	37	-	ns
Q_r	recovered charge		-	43	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0 \text{ V}; I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s};$ $V_{DS} = 20 \text{ V};$ Fig. 18	-	21	-	ns
t_b	reverse recovery fall time		-	16	-	ns

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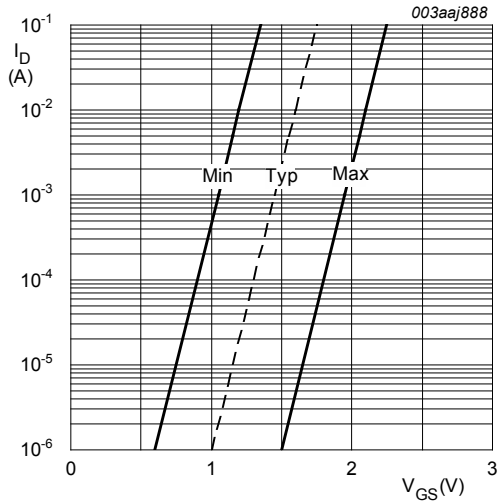


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

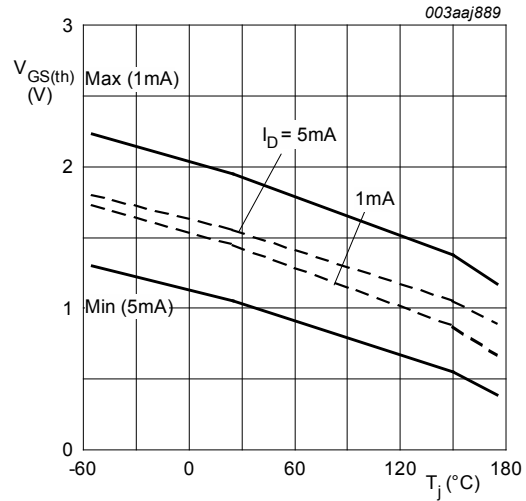


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$V_{DS} = V_{GS}$

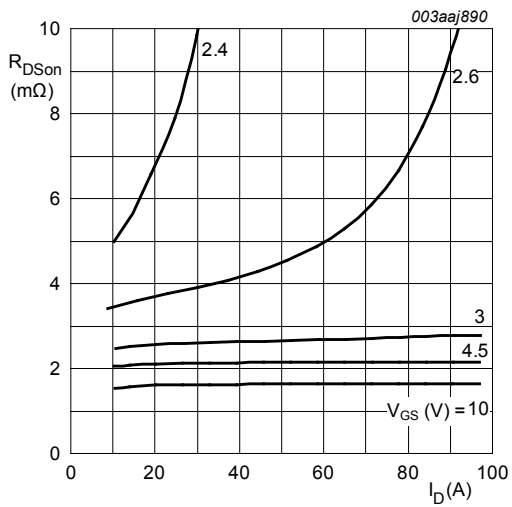


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

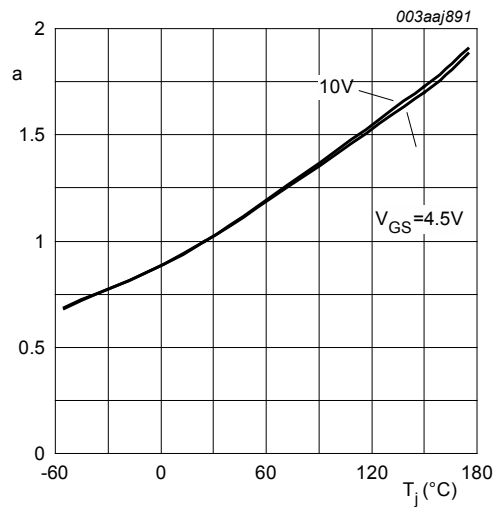


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

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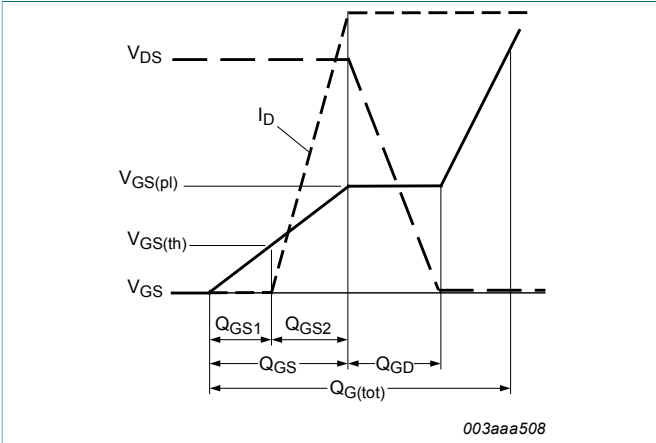


Fig. 14. Gate charge waveform definitions

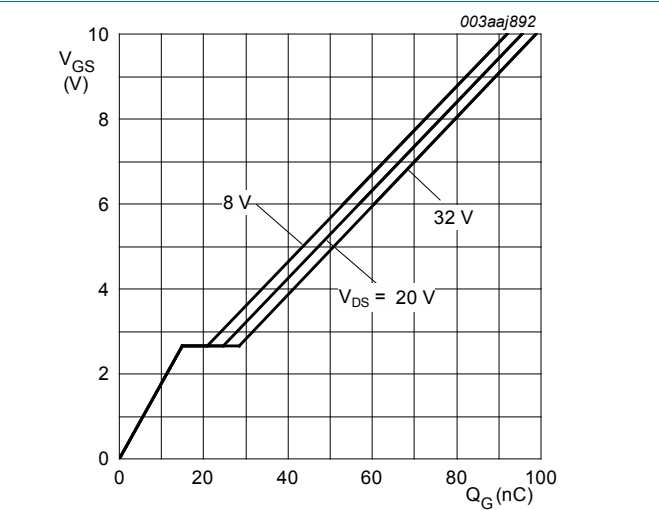


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

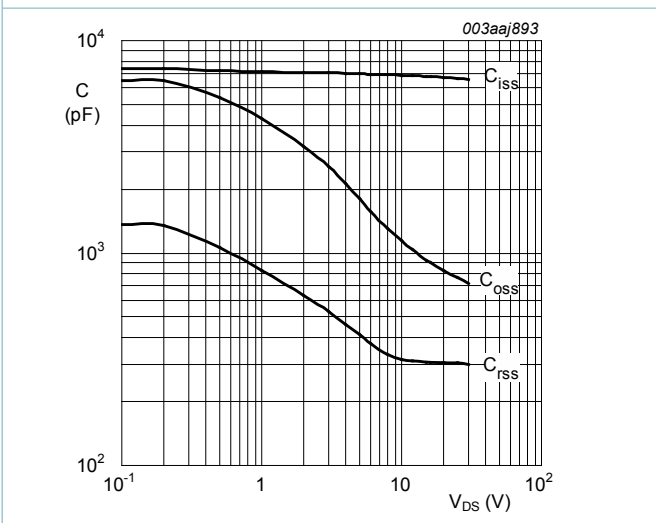


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{V}; f = 1\text{MHz}$

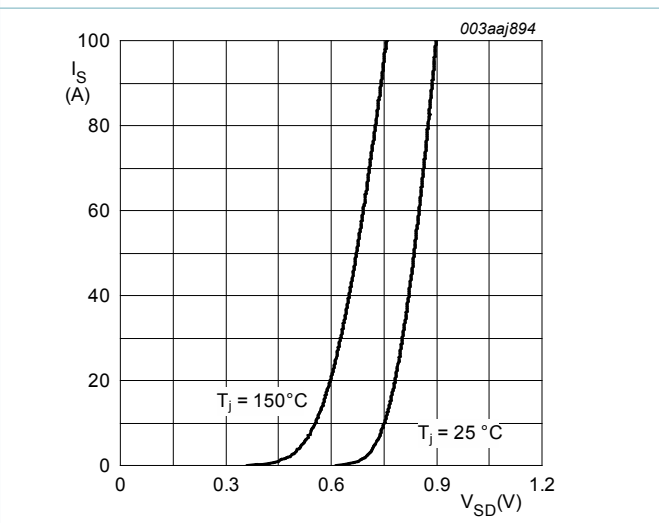


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{V}$

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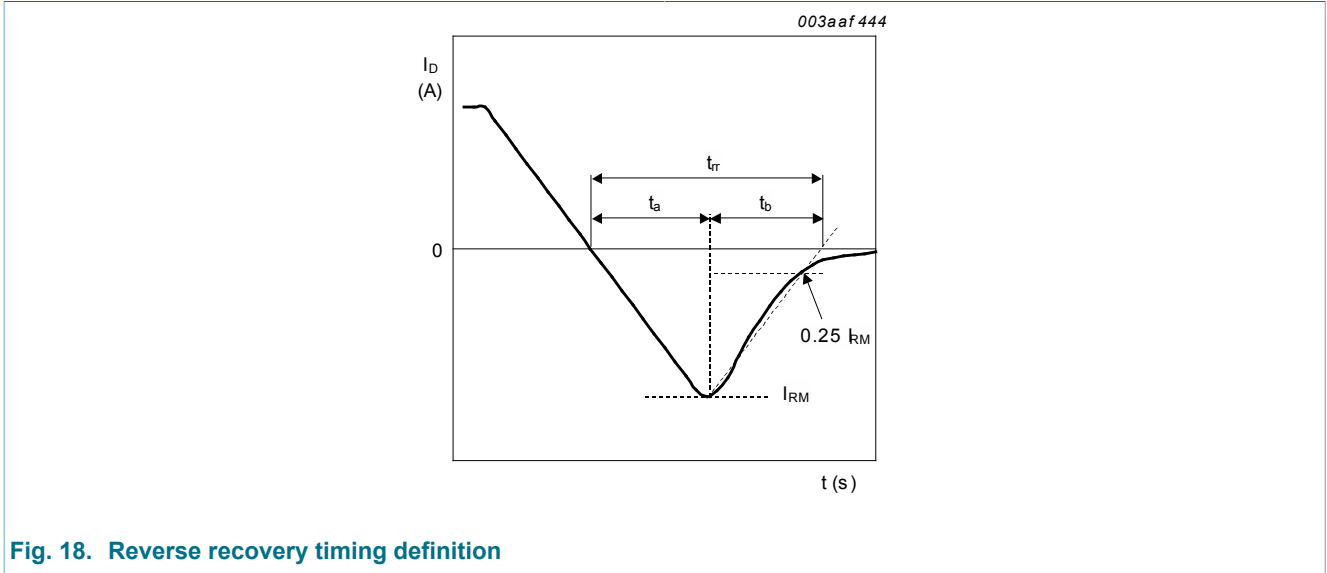


Fig. 18. Reverse recovery timing definition

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7. Package outline

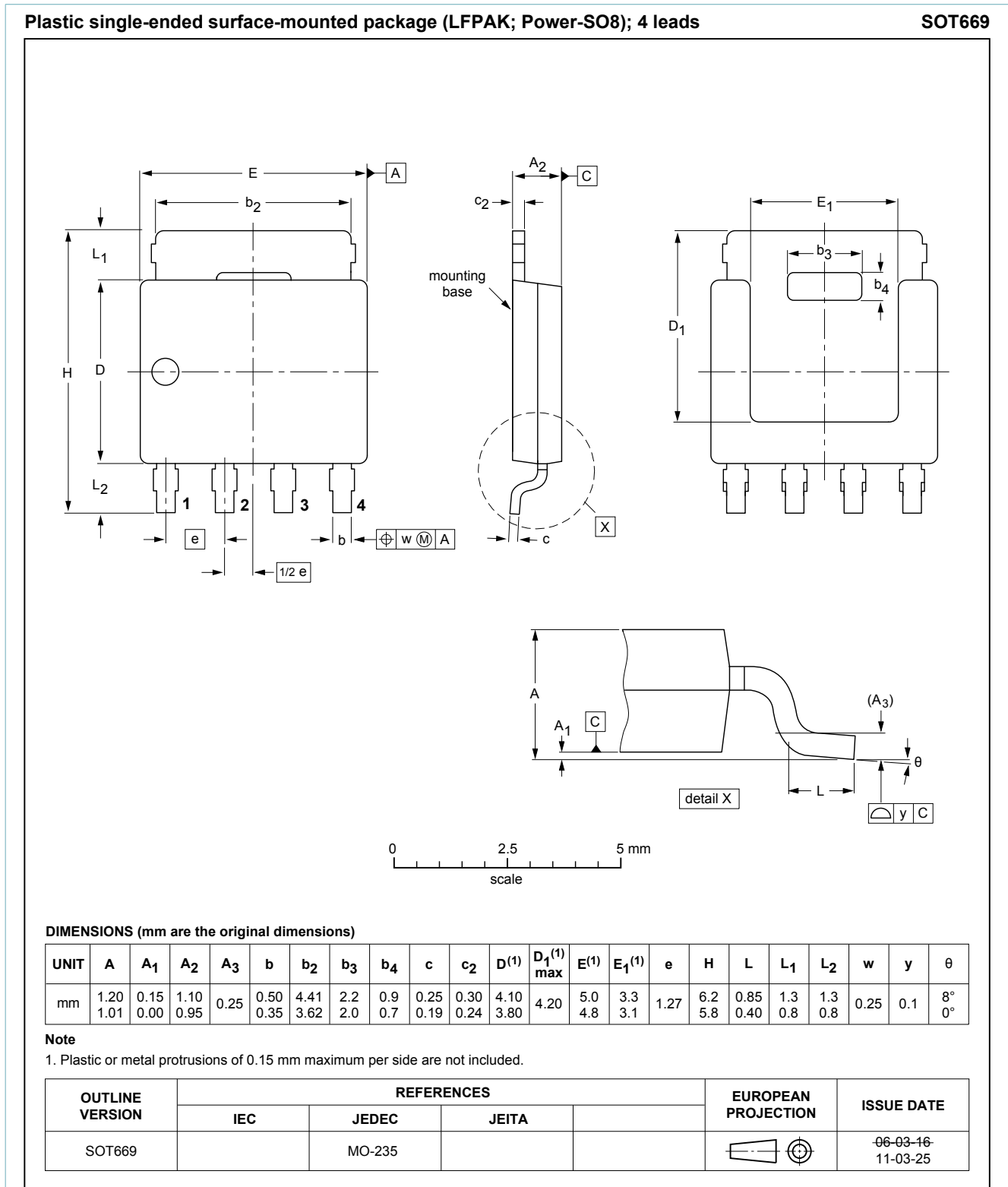


Fig. 19. Package outline LPAK; Power-SO8 (SOT669)

8. Legal information

8.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
 [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 22 August 2012