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LM1971 Overture™ Audio Attenuator Series Digitally Controlled 62 dB Audio Attenuator with/Mute

Check for Samples: LM1971

FEATURES

- **3-Wire Serial Interface**
- **Mute Function**
- **Click and Pop Free Attenuation Changes**
- **8-Pin Plastic PDIP and SOIC Packages Available**

APPLICATIONS

- **Communication Systems**
- **Cellular Phones and Pagers**
- **Personal Computer Audio Control**
- **Electronic Music (MIDI)**
- **Sound Reinforcement Systems**
- **Audio Mixing Automation**

KEY SPECIFICATIONS

- **Total Harmonic Distortion 0.0008 % (Typ)**
- **Frequency Response > 200 kHz (−3 dB) (Typ)**
- **Attenuation Range (Excluding Mute) 62 dB (Typ)**
- **Dynamic Range 115 dB (Typ)**
- **Mute Attenuation 102 dB (Typ)**

DESCRIPTION

The LM1971 is a digitally controlled single channel audio attenuator fabricated on a CMOS process. Attenuation is variable in 1 dB steps from 0 dB to −62 dB. A mute function disconnects the input from the output, providing over 100 dB of attenuation.

The performance of the device is exhibited by its ability to change attenuation levels without audible clicks or pops. In addition, the LM1971 features a low Total Harmonic Distortion (THD) of 0.0008%, and a Dynamic Range of 115 dB, making it suitable for digital audio needs. The LM1971 is available in both 8-pin plastic PDIP or SOIC packages.

The LM1971 is controlled by a TTL/CMOS compatible 3-wire serial digital interface. The active low LOAD line enables the data input registers while the CLOCK line provides system timing. Its DATA pin receives serial data on the rising edge of each CLOCK pulse, allowing the desired attenuation setting to be selected.

Typical Application

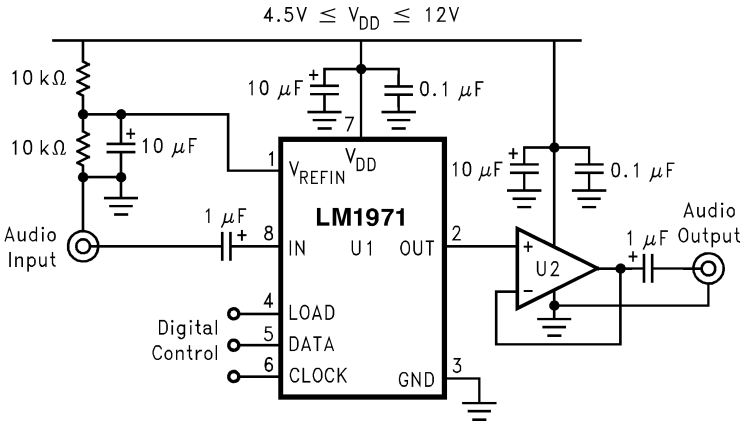

Figure 1. Typical Audio Attenuator Application Circuit

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Connection Diagram

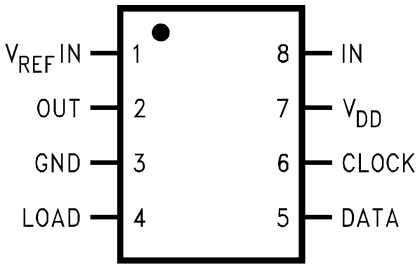


Figure 2. Dual-In-Line Plastic or Surface Mount Package- Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage, V_{DD}			15V
Voltage at any pin			(GND −0.2V) to (V_{DD} +0.2V)
ESD Susceptibility(4)			3000V
Soldering Information	P Package (10s)		260°C
	D Package	Vapor Phase (60s)	215°C
		Infrared (15s)	220°C
Power Dissipation(5)			150 mW
Junction Temperature			150°C
Storage Temperature			−65°C to +150°C

(1) All voltages are measured with respect to the GND pin (pin 3), unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_D = (T_{JMAX} – T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM1971N and LM1971M, T_{JMAX} = +150°C, and the typical junction-to-ambient thermal resistance, θ_{JA}, when board mounted is 102° C/W and 167° C/W, respectively.

Operating Ratings(1)(2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ +85°C
Thermal Resistance	D0008A Package, θ_{JA}	167°C/W
	P0008E Package, θ_{JA}	102°C/W
Supply Voltage		4.5V to 12V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the GND pin (pin 3), unless otherwise specified.

Electrical Characteristics (1)(2)

The following specifications apply for V_{DD} = +12V (V_{REF}IN = +6V), V_{IN} = 5.5 V_{pk}, and f = 1 kHz, unless otherwse specified. Limits apply for T_A = 25°C. Digital inputs are TTL and CMOS compatible.

Symbol	Parameter	Conditions	LM1971		Units (Limits)
			Typical (3)	Limit (4)	
I_S	Supply Current	Digital Inputs Tied to 6V	1.8	3	mA (max)
THD	Total Harmonic Distortion	V_{IN} = 0.5V_{pk}@ 0 dB Attenuation	0.0008	0.003	% (max)
e_{IN}	Noise	Input is AC Grounded @ −12 dB Attenuation A-Weighted (5)	4.0		µV
DR	Dynamic Range	Referenced to Full Scale = +6 V_{pk}	115		dB
A_M	Mute Attenuation		102	96	dB (min)
	Attenuation Step Size Error	0 dB to −62 dB	0.009	0.2	dB (max)
	Absolute Attenuation	Attenuation @ 0 dB Attenuation @ −20 dB Attenuation @ −40 dB Attenuation @ −60 dB Attenuation @ −62 dB	0.1 −20.3 −40.5 −60.6 −62.6	0.5 −19.0 −38.0 −57.0 −59.0	dB (min) dB (min) dB (min) dB (min) dB (min)
I_{LEAK}	Analog Input Leakage Current	Input is AC Grounded	5.8	100	nA (max)
	Frequency Response	20 Hz–100 kHz	±0.1		dB
R_{IN}	AC Input Impedance	Pin 8, V_{IN} = 1.0 V_{pk}, f = 1 kHz	40	20 60	kΩ (min) kΩ (max)
I_{IN}	Input Current	@ Pins 4, 5, 6 @ 0V < V_{IN} < 5V	1.0	100	nA (max)
f_{CLK}	Clock Frequency		3	2	MHz (max)
V_{IH}	High-Level Input Voltage	@ Pins 4, 5, 6		2.0	V (min)
V_{IL}	Low-Level Input Voltage	@ Pins 4, 5, 6		0.8	V (max)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the GND pin (pin 3), unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specifications that all parts are tested in production to meet the stated values.
(5) Due to production test limitations, there is no limit for the Noise test. Please refer to Figure 5 and Figure 8 in Typical Performance Characteristics.

Pin Descriptions

V_{REF}IN (1): The V_{REF}IN pin provides the reference for the analog input signal. This pin should be biased at half of the supply voltage, V_{DD}, as shown in Figure 1 and Figure 19.

OUT (2): The attenuated analog output signal comes from this pin.

GND (3): The GND pin references the digital input signals and is the lower voltage reference for the IC. Typically this pin would be labeled "V_{SS}" but the ground reference for the digital logic input control is tied to this same point. With a higher pin-count there would generally be separate pins for these functions; V_{SS} and Logic Ground. It is intended that the LM1971 always be operated using a single voltage supply configuration, for which pin 3 (GND) should always be at system ground. If a bipolar or split-supply configuration are desired, level shifting circuitry is needed for the digital logic control pins as they would be referenced through pin 3 which would be at the negative supply. It is highly recommended, however, that the LM1971 be used in a unipolar or single-supply configuration.

LOAD (4): The LOAD input accepts a TTL or CMOS level signal. This is the enable pin of the device, allowing data to be clocked in while this input is low (0V). The GND pin is the reference for this signal.

DATA (5): The DATA input accepts a TTL or CMOS level signal. This pin is used to accept serial data from a microcontroller that will be latched and decoded to change the channel's attenuation level. The GND pin is the reference for this signal.

CLOCK (6): The CLOCK input accepts a TTL or CMOS level signal. The clock input is used to load data into the internal shift register on the rising edge of the input clock waveform. The GND pin is the reference for this signal.

V_{DD} (7): The positive voltage supply should be placed to this pin.

IN (8): The analog input signal should be placed to this pin.

Typical Performance Characteristics

Supply Current vs Supply Voltage

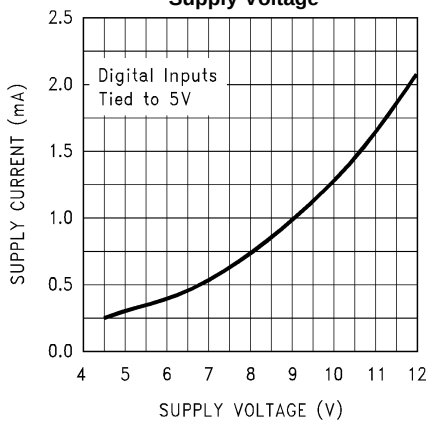


Figure 3.

Supply Current vs Temperature

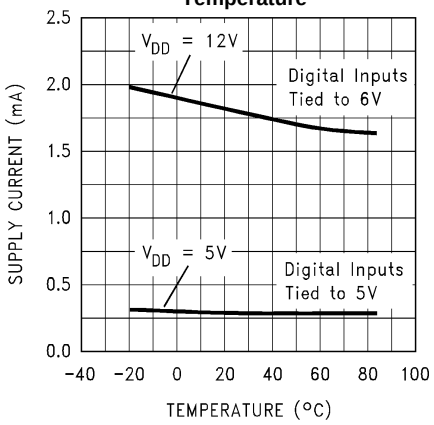


Figure 4.

Noise Floor Analog Measurement

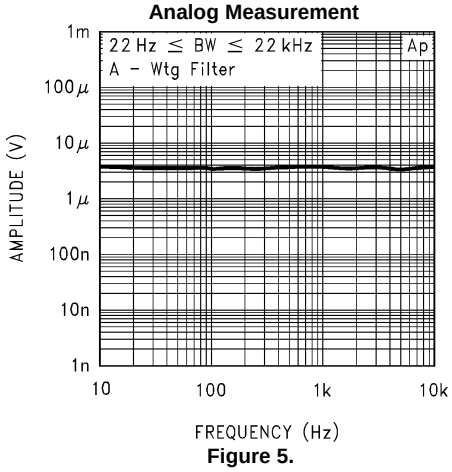


Figure 5.

THD + N vs Freq and Amp

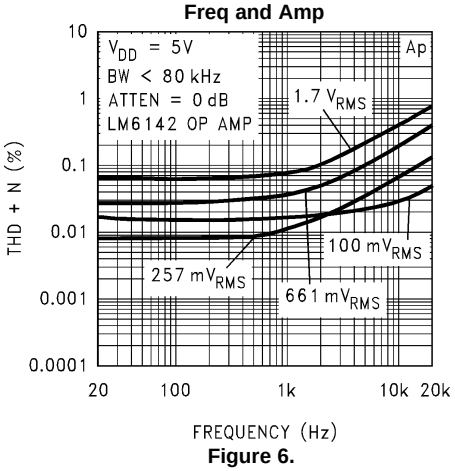


Figure 6.

THD + N vs Freq and Amp

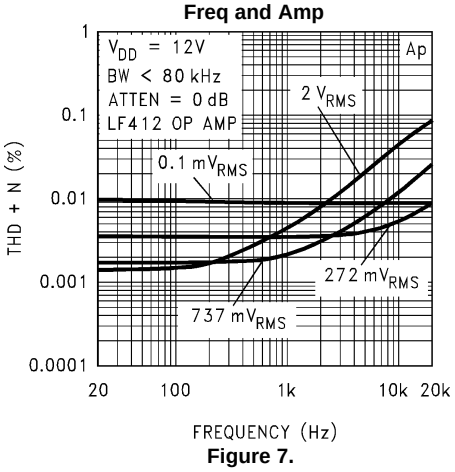


Figure 7.

Noise Floor Spectrum by FFT

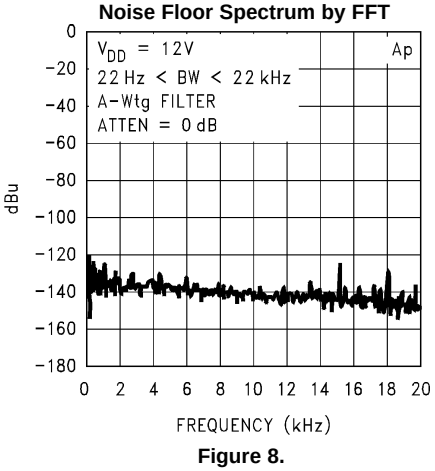


Figure 8.

Typical Performance Characteristics (continued)

THD + N vs Amplitude

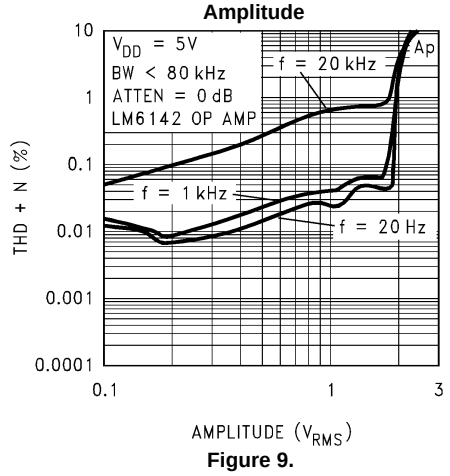


Figure 9.

THD + N vs Amplitude

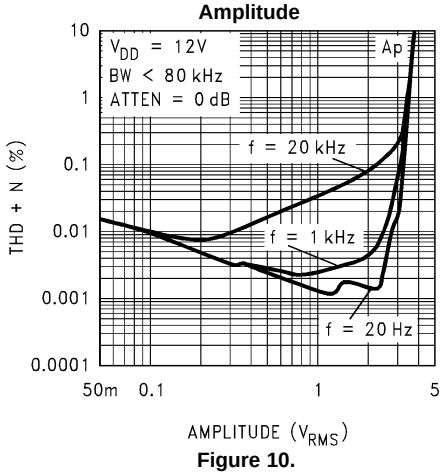


Figure 10.

Mute Attenuation vs Frequency

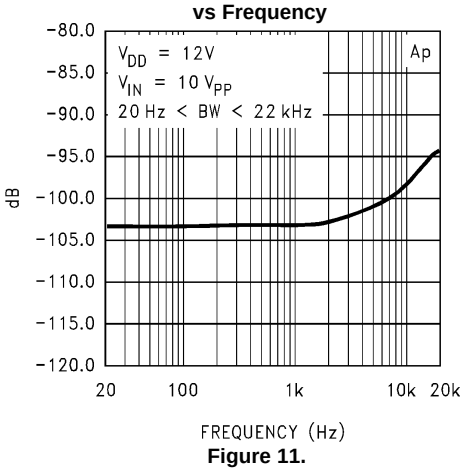


Figure 11.

THD vs Freq by FFT

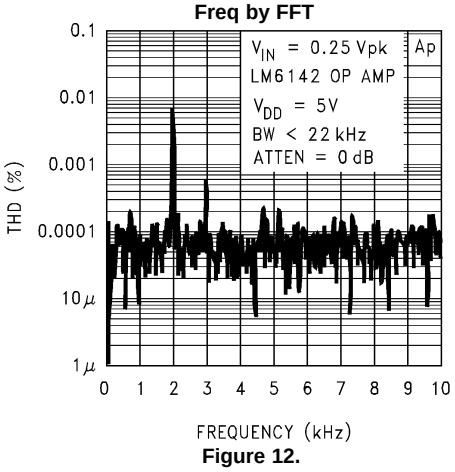


Figure 12.

THD vs Freq by FFT

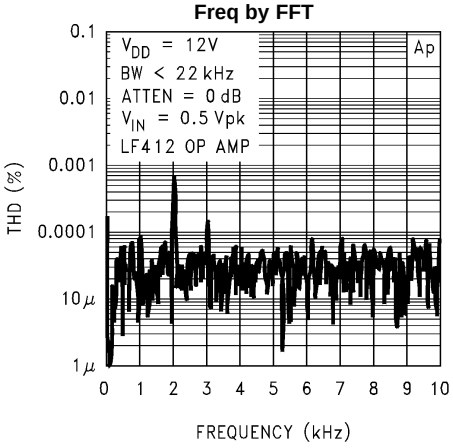


Figure 13.

Output Impedance vs Attenuation Level

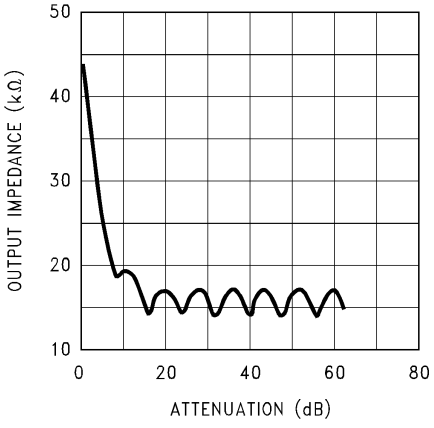


Figure 14.

APPLICATION INFORMATION

SERIAL DATA FORMAT

The LM1971 uses a 3-wire serial communication format that is easily controlled by a microcontroller. The timing for the 3-wire set, comprised of DATA, CLOCK, and LOAD is shown in Figure 15. As depicted in Figure 15, the LOAD line is to go low at least 150 ns before the rising edge of the first clock pulse and is to remain low throughout the transmission of the 16 data bits. The serial data is composed of an 8-bit address, which must always be set to 0000 0000 to select the single audio channel, and 8 bits for attenuation setting. For both address data and attenuation setting data, the MSB is sent first with the address data preceding the attenuation data. Please refer to Figure 16 to confirm the serial data format transfer process.

Table 1 shows the various Address and Data byte values for different attenuation settings. Note that Address bytes other than 0000 0000 are ignored.

µPOT SYSTEM ARCHITECTURE

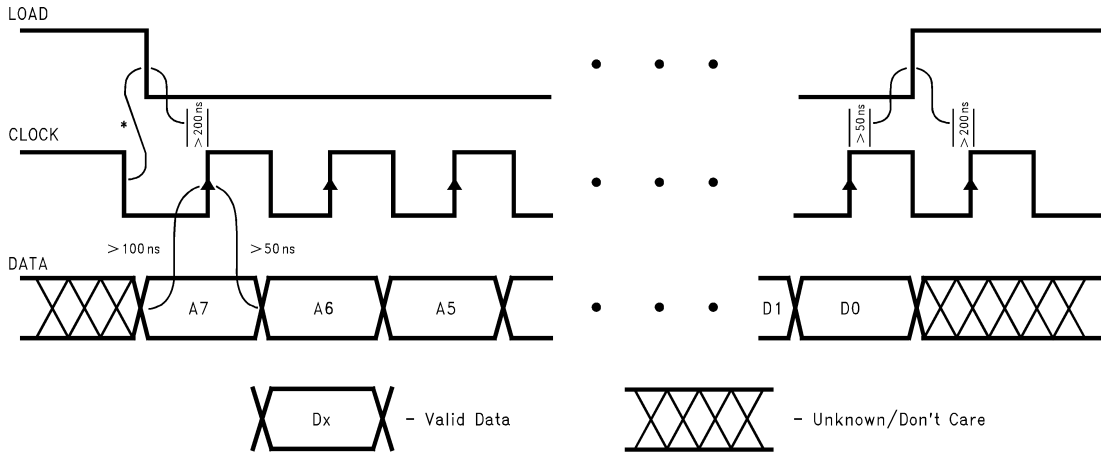
The µPot's digital interface is essentially a shift register where serial data is shifted in, latched, and then decoded. Once new data is shifted in, the LOAD line goes high, latching in the new data. The data is then decoded and the appropriate switch is activated to set the desired attenuation level. This process is continued each and every time an attenuation change is made. When the µPot is powered up, it is placed into the Mute mode.

µPOT DIGITAL COMPATIBILITY

The µPot's digital interface section is compatible with TTL or CMOS logic. The shift register inputs act upon a threshold of two diode drops above the ground level (Pin 3) or approximately 1.4V.

Table 1. Attenuator Register Set Description

Address Register (Byte 0)	
MSB LSB A7–A0	
0000 0000	Channel 1
0000 0001	Ignored
0000 0010	Ignored
Data Register (Byte 1)	
Contents	**Attenuation (dB)**
MSB LSB D7–D0	
0000 0000	0.0
0000 0001	1.0
0000 0010	2.0
0000 0011	3.0
:::::	::
0001 0000	16.0
0001 0001	17.0
0001 0010	18.0
0001 0011	19.0
:::::	::
0011 1101	61.0
0011 1110	62.0
0011 1111	96 (Mute)
0100 0000	96 (Mute)
:::::	::
1111 1110	96 (Mute)
1111 1111	96 (Mute)



***Note:** Load and clock falling edges can be coincident, however, the clock falling edge cannot be delayed more than 20 ns from the falling edge of load. It is preferrable that the falling edge of clock occurs before the falling edge of load.

Figure 15. Timing Diagram

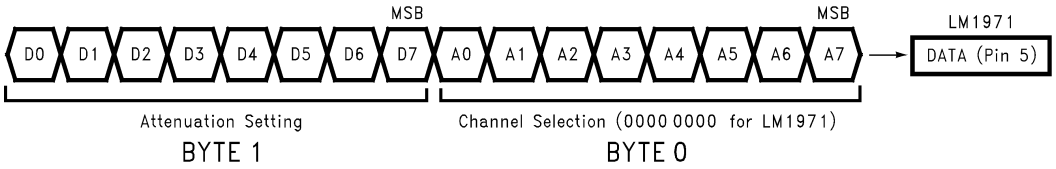


Figure 16. Serial Data Format Transfer Process

µPOT LADDER ARCHITECTURE

The µPot contains a chain of R1/R2 resistor dividers in a ladder form, as shown in Figure 17. Each R1 is actually a series of 8 resistors, with a CMOS switch that taps into the resistor chain according to the attenuation level chosen. For any given attenuation setting, there is only one CMOS switch closed (no paralleling of ladders). The input impedance therefore remains constant, while the output impedance changes as the attenuation level changes. It is important to note that the architecture is a series of resistor dividers, and not a straight, tapped resistor, so the µPot is not a variable resistor; it is a variable voltage divider.

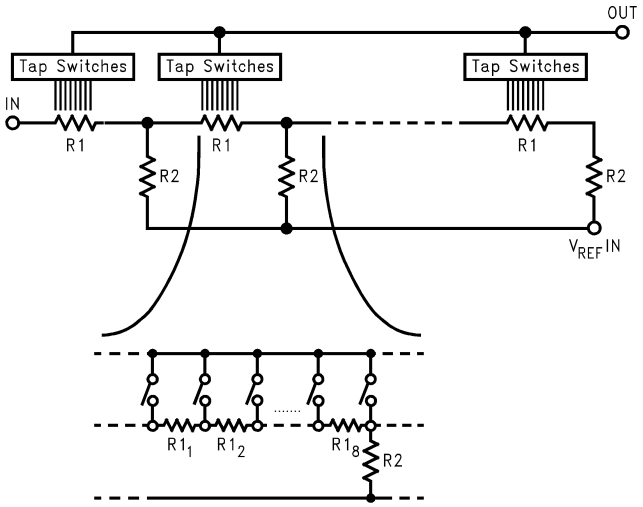


Figure 17. Resistor Ladder Architecture

ATTENUATION STEP SCHEME

The fundamental attenuation step scheme for the LM1971 is shown in Figure 18. It is also possible to obtain any integer value attenuation step through programming, in addition to the 2 dB and 4 dB steps shown in Figure 18. All higher attenuation step schemes can have clickless and popless performance. Although it is possible to "skip" attenuation points by not sending all of the data, clickless and popless performance will suffer. It is highly recommended that all of the data points should be sent for each attenuation level. This ensures flawless operation and performance when making steps larger than 1 dB.

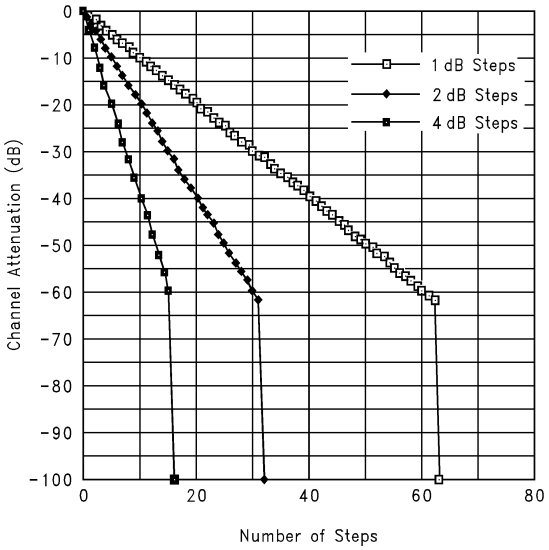


Figure 18. LM 1971 Channel Attenuation vs Digital Step Value (1 dB, 2 dB, and 4 dB Steps)

INPUT IMPEDANCE

The input impedance of a µPot is constant at a nominal 40 kΩ. Since the LM1971 is a single-supply operating device, it is necessary to have both input and output coupling caps as shown in Figure 1. To ensure full low-frequency response, a 1 µF coupling cap should be used.

OUTPUT IMPEDANCE

The output impedance of a µPot varies typically between 25 kΩ and 35 kΩ and changes nonlinearly with step changes. Since a µPot is made up of a resistor ladder network with logarithmic attenuation, the output impedance is nonlinear. Due to this configuration, a µPot cannot be considered as a linear potentiometer; it is a logarithmic attenuator.

The linearity of a µPot cannot be measured directly without a buffer because the input impedance of most measurement systems is not high enough to provide the required accuracy. The lower impedance of the measurement system would load down the output and an incorrect reading would result. To prevent loading, a JFET input op amp should be used as the buffer/amplifier.

OUTPUT BUFFERING

There are two performance issues to be aware of that are related to a µPot's output stage. The first concern is to prevent audible clicks with attenuation changes, while the second is to prevent loading and subsequent linearity errors. The output stage of a µPot needs to be buffered with a low input bias current op amp to keep DC shifts inaudible. Additionally, the output of µPot needs to see a high impedance to keep linearity errors low.

Attenuation level changes cause changes in the output impedance of a µPot. Output impedance changes in the presence of a large input bias current for a buffer/amplifier will cause a DC shift to occur. Neglecting amplifier gains and speaker sensitivities, the audibility of a DC shift is dependent upon the output impedance change times the required input bias current. As an example, a 5 kΩ impedance change times a 1 µA bias current results in a 5 mV DC shift; a level that is barely audible without any music material in the system. An op amp with a bias current of 200 pA for the same 5 kΩ change results in an inaudible 1 µV DC shift. Since the worst case output impedance changes are on the order of several kΩ, a bias current much less than 1 µA is required for highest performance. In order to further quantify DC shifts, please refer to Figure 14 in Typical Performance Characteristics and relate worst case impedance changes to the selected buffer/amplifier input bias current.

Without the use of a high input impedance (> 1 MΩ) op amp for the buffer/amplifier, loading will occur that causes linearity errors in the signal. To ensure the highest level of performance, a JFET or CMOS input high input impedance op amp is required.

One common application that requires gain at the output of a µPot is input signal volume control. Depending upon the input source material, the LM1971 provides a means of controlling the input signal level. With a supply voltage range of 4.5V to 12V, the LM1971 has the ability of controlling fairly inconsistent input source signal levels. Using an op amp with gain at the µPot's output, as shown in Figure 20, will also allow the system dynamic range to be increased. JFET op amps like the LF351 and the LF411 are well suited for this application. If active half-supply buffering is also desired, dual op amps like the LF353 and the LF412 could be used.

For low voltage supply applications, op amps like the CMOS LMC6041 are preferred. This part has a supply operating range from 4.5V–15.5V and also comes in a surface mount package.

µPOT HALF-SUPPLY REFERENCING

The LM1971 operates off of a single supply, with half-supply biasing supplied at the V_{REF}IN terminal (Pin 1). The easiest and most cost effective method of providing this half-supply is a simple resistor divider and bypass capacitor network shown in Figure 1. The capacitor not only stabilizes the half-supply node by “holding” the voltage nearly constant, but also decouples high frequency signals on the supply to ground. Signal feedthrough, power supply ripple and fluctuations that are not properly filtered could cause the performance of the LM1971 to be degraded.

A more stable half-supply node can be obtained by actively buffering the resistor divider network with a voltage follower as shown in Figure 19. Supply fluctuations are then isolated by the high input impedance/low output impedance mismatch associated with effective filtering. Since the LM1971 is a single channel device, using a dual JFET input op amp is optimum for both output buffering and half-supply biasing.

A 10 µF capacitor or larger is recommended for better half-supply stabilization. For added rejection of higher frequency power supply fluctuations, a smaller capacitor (0.01 µF–0.1 µF) could be added in parallel to the 10 µF capacitor.

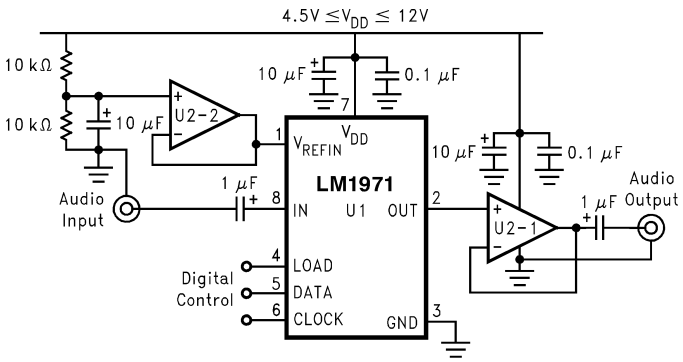


Figure 19. Higher Performance Active Half-Supply Buffering

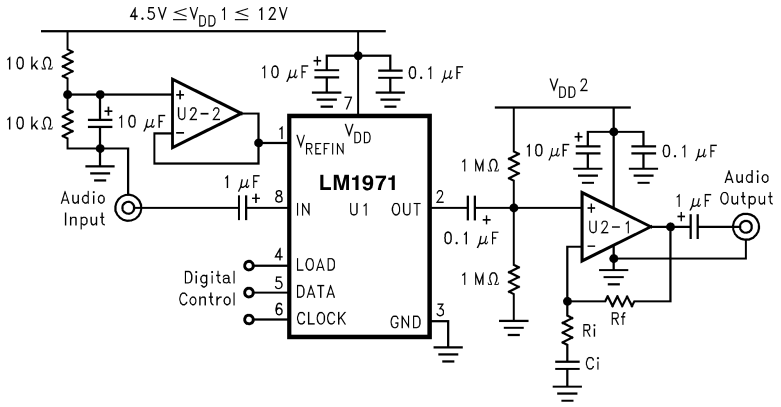


Figure 20. Active Reference with Active Gain Buffering

LOGARITHMIC GAIN AMPLIFIER

The µPot is capable of being used in the feedback loop of an op amp to create a gain controlled amplifier as shown in Figure 21. In this configuration the attenuation levels from Table 1 become gain levels with the largest possible gain value being 62 dB. For most applications, 62 dB of gain will cause signal clipping to occur. However, this can be controlled through programming. It is important to note that when in mute mode the input is disconnected from the output, thus placing the amplifier in open-loop gain state. In this mode, the amplifier will behave as a comparator. Care should be taken with the programming and design of this type of circuit. To provide the best overall performance, a high input impedance, low input bias current op amp should be used.

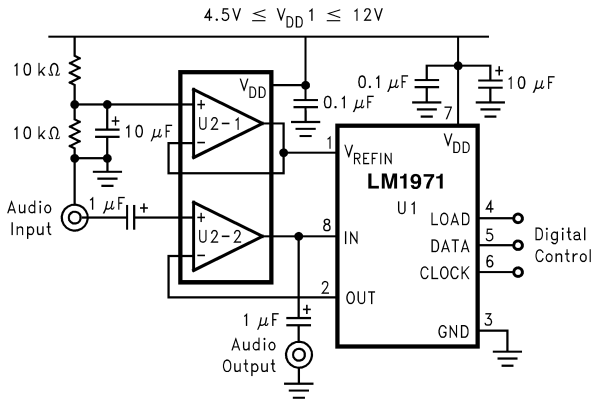


Figure 21. Logarithmic Gain Amplifier Circuit

MUTE FUNCTION

A major feature of the LM1971 is its ability to mute the input signal to an attenuation level of 102 dB. This is accomplished internally by physically disconnecting the output from the input while also grounding the output pin through approximately 2 kΩ.

The mute function is obtained during power-up of the device or by sending any binary data of 0011 1111 and above serially to the device. The device may be placed into mute at any time during operation, allowing the designer to make the mute command accessible to the end-user.

DC INPUTS

Although the µPot was designed to be used as an attenuator for signals within the audio spectrum, it is also capable of tracking and attenuating an input DC voltage. The device will track voltages to either supply rail.

One point to remember about DC tracking is that with a buffer at the output of the µPot, the resolution of DC tracking will depend upon the gain configuration of that output buffer and its supply voltage. Also, the output buffer's supply voltage does not have to be the same as the µPot's supply voltage. Giving the buffer some gain can provide more resolution when tracking small DC voltages.

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM1971M	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM19 71M	Samples
LM1971M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM19 71M	Samples
LM1971MX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LM19 71M	Samples
LM1971MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM19 71M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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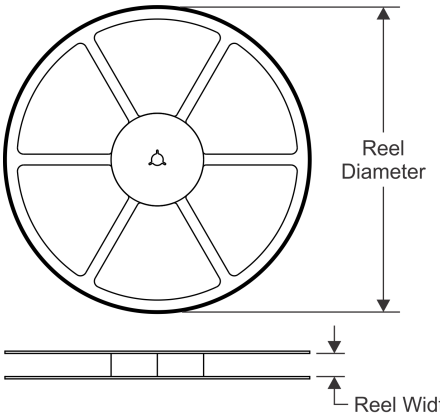
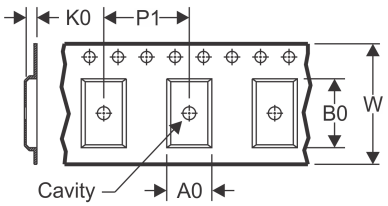
TAPE AND REEL INFORMATION

REEL DIMENSIONS

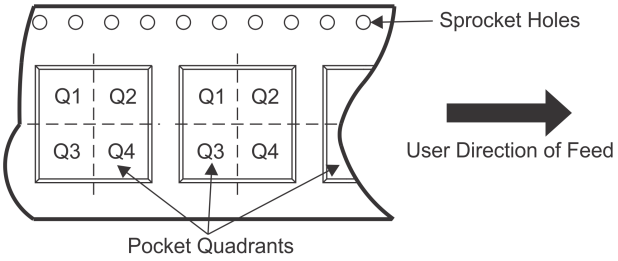


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

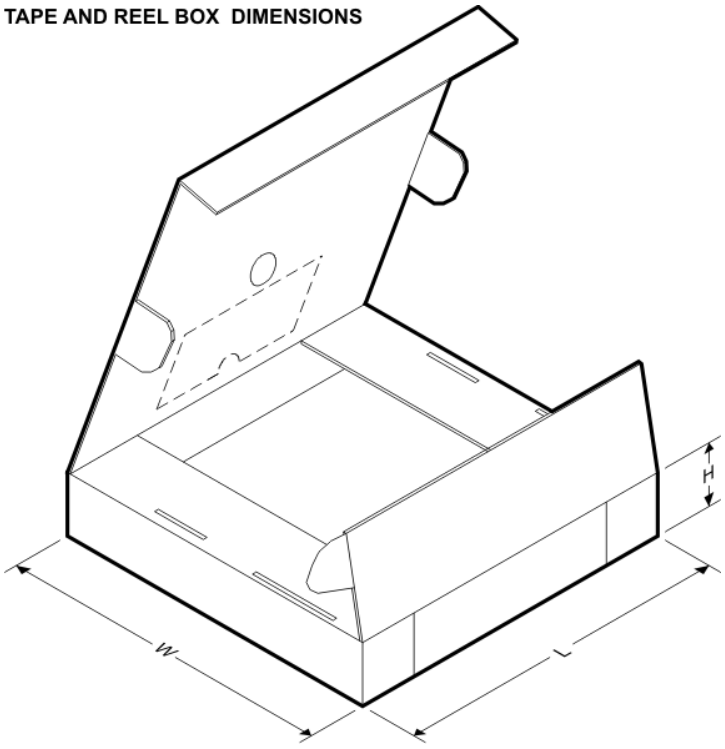


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM1971MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM1971MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

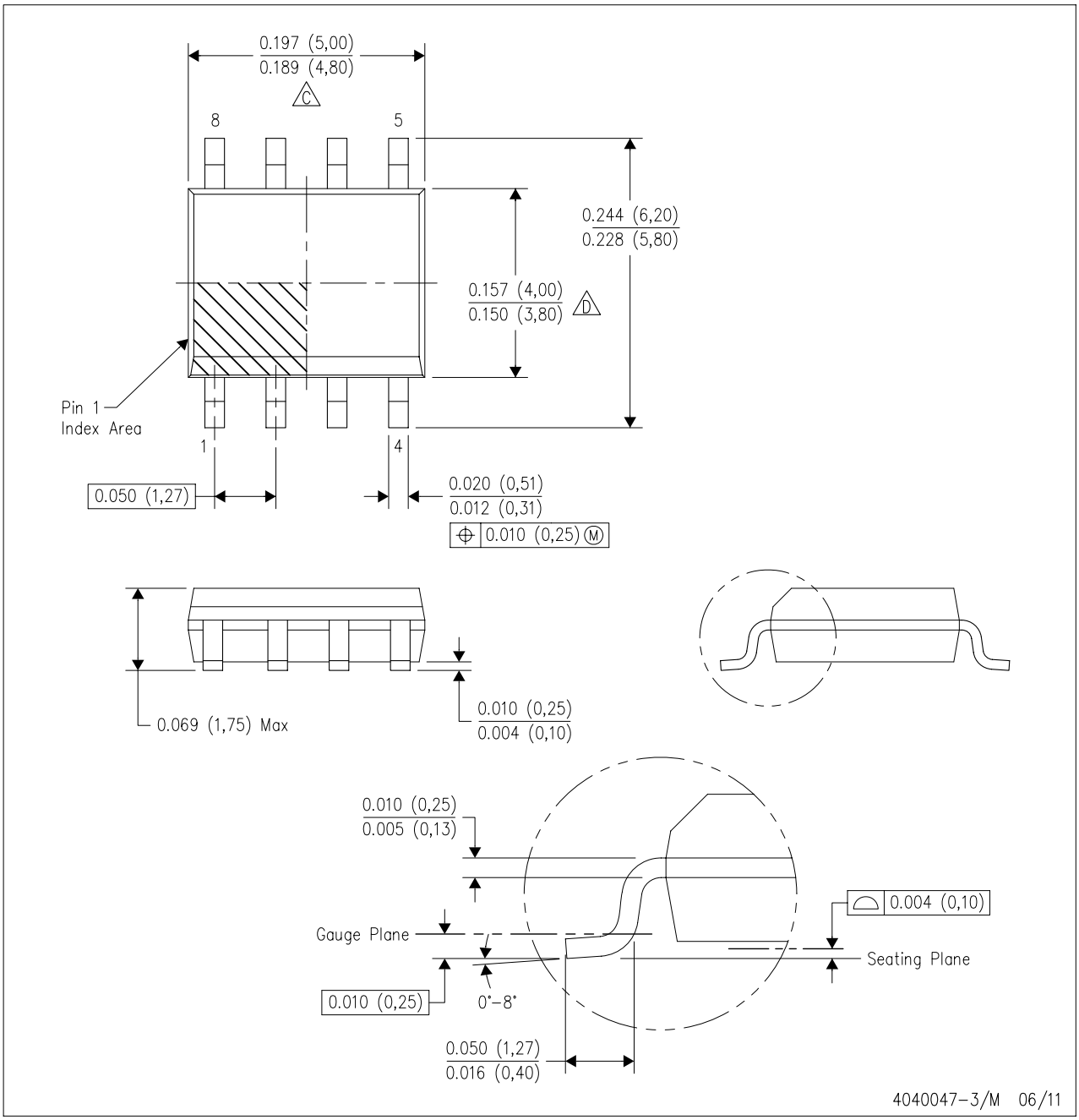


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM1971MX	SOIC	D	8	2500	367.0	367.0	35.0
LM1971MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

MECHANICAL DATA

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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