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CLC5958 14-Bit, 52 MSPS A/D Converter

Check for Samples: CLC5958

FEATURES

- **Ultra-wide Dynamic Range**
- **Excellent Performance to Nyquist**
- **IF Sampling Capability**
- **Very Small Package: 48-pin PLGA**
- **Programmable Output Levels: 3.3V to 5V**

KEY SPECIFICATIONS

- **Sample Rate 52 MSPS**
- **SFDR 90 dB**
- **Noise Floor −72 dBFS**

APPLICATIONS

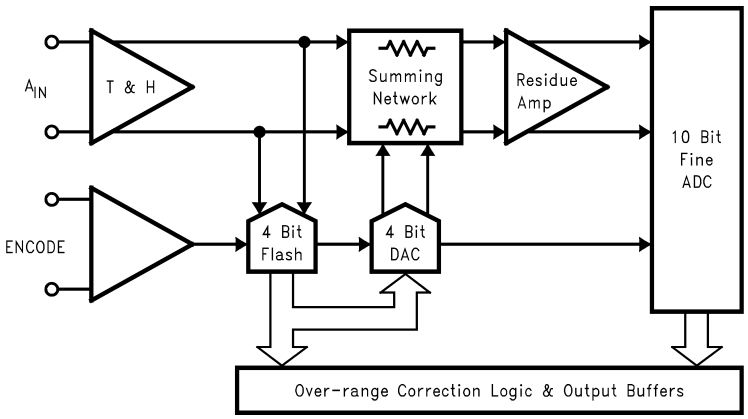
- **Multi-channel Basestations**
- **Multi-standard Basestations:**
  - **GSM, WCDMA, DAMPS, etc.**
- **Smart Antenna Systems**
- **Wireless Local Loop**
- **Wideband Digital Communications**

DESCRIPTION

The CLC5958 is a monolithic 14-bit, 52 MSPS analog-to-digital converter. The ultra-wide dynamic range and high sample rate of the device make it an excellent choice for wideband receivers found in multi-channel base-stations. The CLC5958 integrates a low distortion track-and-hold amplifier and a 14-bit multi-stage quantizer on a single die. Other features include differential analog inputs, low jitter differential clock inputs, an internal bandgap voltage reference, and CMOS/TTL compatible outputs. The CLC5958 is fabricated on the ABIC-V 0.8 micron BiCMOS process.

The CLC5958 features a 90 dB spurious free dynamic range (SFDR) and 70 dB signal-to-noise ratio (SNR). The balanced differential analog inputs ensure low even-order distortion, while the differential clock inputs permit the use of balanced clock signals to minimize clock jitter. The 48-pin PLGA package provides an extremely small footprint for applications where space is a critical consideration. The package also provides a very low thermal resistance to ambient. The CLC5958 may be operated with a single +5V power supply. Alternatively, an additional supply may be used to program the digital output levels over the range of +3.3V to +5V. Operation over the industrial temperature range of −40°C to +85°C is ensured. National Semiconductor tests each part to verify compliance with the ensured specifications.

Block Diagram



Pin Configuration

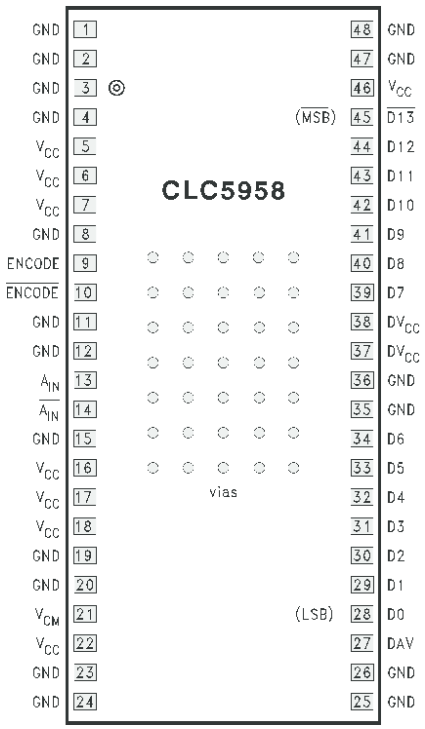


Figure 1. 48 Pin PLGA
See Package Number NPB

PIN DESCRIPTIONS

Pin Name	Pin No.	Description
A_{IN}, $\overline{A_{IN}}$	13, 14	Differential inputs. Self biased at a common mode voltage of +3.25V. The ADC full scale input is 2.048 V_{PP} differential.
ENCODE, $\overline{\text{ENCODE}}$	9, 10	Differential clock inputs. ENCODE initiates a new data conversion cycle on each rising edge. Clock signals may be sinusoidal or square waves with PECL encode levels. The falling edge of ENCODE clocks internal pipeline stages.
D0–$\overline{\text{D13}}$	28–34, 39–45	Digital data outputs. CMOS and TTL compatible. D0 is the LSB and $\overline{\text{D13}}$ is the inverted MSB. Output coding is two's complement.
DAV	27	Data valid. The rising edge of this signal occurs when output data is valid and may be used to latch data into following circuitry.
V_{CM}	21	Internal analog input common mode voltage reference. Nominally +3.25V. Can be used to establish the analog input common mode voltage for DC coupled applications (DC coupling not recommended, see CLC5958 Application Information).
GND	1–4, 8, 11, 12, 15, 19, 20, 23–26, 35, 36, 47, 48 and vias	Circuit ground.
V_{CC}	5–7, 16–18, 22, 46	+5V power supply. Bypass each group of supply pins to ground with a 0.01 µF capacitor.
DV_{CC}	37, 38	+3.3V to +5V power supply for the digital outputs. Establishes the high output level for the digital outputs. Bypass to ground with a 0.1 µF capacitor.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Positive Supply Voltage (V_{CC})		−0.5V to +6V
Differential Voltage between any Two Grounds		<200 mV
Analog Input Voltage Range		GND to V_{CC}
Digital Input Voltage Range		−0.5V to +V_{CC}
Output Short Circuit Duration (one-pin to ground)		Infinite
Junction Temperature		175°C
Storage Temperature Range		−65°C to +150°C
Lead Solder Duration (+240°C)		5 sec.
ESD tolerance	human body model	2000V
	machine model	200V

(1) "Absolute Maximum Ratings" are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

Positive Supply Voltage (V_{CC})	+5V ±5%
Analog Input Voltage Range	2.048 V_{PP} diff.
Input Coupling	AC
Operating Temperature Range	−40°C to +85°C
Digital Output Supply Voltage (DV_{CC})	+3.3V ±5%
Analog Input Common Mode Voltage	V_{CM} ±0.025V

Package Thermal Resistance

Package	θ_{JA}	θ_{JC}
48-Pin PLGA	39°C/W	5°C/W

Reliability Information

Transistor Count	10,000

Converter Electrical Characteristics

The following specifications apply for V_{CC} = +5V, DV_{CC} = +3.3V, 52 MSPS. **Boldface limits apply for T_A = T_{min} = −40°C to T_{max} = +85°C,** all other limits T_A = 25°C(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	RESOLUTION(2)(3)			14		Bits
	DIFFERENTIAL INPUT VOLTAGE RANGE			2.048		V
	MAXIMUM CONVERSION RATE(2)(3)		**52**	65		MSPS
SNR	Signal-to-Noise Ratio(2)	f_{IN} = 10 MHz, A_{IN} = −0.6 dBFS	69	71		dBFS
SFDR	Spurious-Free Dynamic Range(2)	f_{IN} = 10 MHz, A_{IN} = −0.6 dBFS	80	90		dB
	SFDR Excluding 2nd and 3rd Harmonics(2)	f_{IN} = 10 MHz, A_{IN} = −0.6 dBFS	85	92		dB
	NO MISSING CODES(2)	f_{IN} = 10 MHz, A_{IN} = −0.6 dBFS	Specified			
NOISE AND DISTORTION						
	Noise Floor(4)	f_{IN} = 5 MHz, A_{IN} = −1 dBFS		−71.0		dBFS
		f_{IN} = 5 MHz, A_{IN} = −20 dBFS		−72.0		dBFS

(1) Typical specifications are based on the mean test values of deliverable converters from the first three diffusion lots.
(2) These parameters are 100% tested at 25°C.
(3) These parameters are sample tested at full temperature range.
(4) Harmonics and clock spurious are removed in noise measurements.

Converter Electrical Characteristics (continued)

The following specifications apply for V_{CC} = +5V, DV_{CC} = +3.3V, 52 MSPS. **Boldface limits apply for T_A = T_{min} = −40°C to T_{max} = +85°C,** all other limits T_A = 25°C(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	2nd and 3rd Harmonic Distortion (w/o dither)	f_{IN} = 5 MHz, A_{IN} = −1 dBFS		−90		dBFS
		f_{IN} = 20 MHz, A_{IN} = −1 dBFS		−87		dBFS
		f_{IN} = 70 MHz, A_{IN} −3 dBFS		−78		dBFS
	Next Worst Harmonic Distortion (w/o dither)(5)	f_{IN} = 5 MHz, A_{IN} = −1 dBFS		−92		dBFS
		f_{IN} = 20 MHz, A_{IN} = −1 dBFS		−90		dBFS
		f_{IN} = 70 MHz, A_{IN} −3 dBFS		−90		dBFS
	Worst Harmonic Distortion (with dither)(6)	f_{IN} = 5 MHz, A_{IN} = −6 dBFS		−95		dBFS
		f_{IN} = 20 MHz, A_{IN} = −6 dBFS		−95		dBFS
		f_{IN} = 70 MHz, A_{IN} −6 dBFS		−82		dBFS
		f_{IN} = 70 MHz (2nd and 3rd excluded), A_{IN} −6 dBFS		−95		dBFS
IMD	2-Tone IM Distortion (w/o dither)	f_{IN1} = 12 MHz, f_{IN2} = 15 MHz, A_{IN1} = A_{IN2} = −7 dBFS		−100		dBFS
SINAD	Signal-to-Noise and Distortion (w/o dither)	f_{IN} = 5 MHz, A_{IN} = −1 dBFS		69		dB
CLOCK RELATED SPURIOUS TONES						
	fs/8, fs/4			−95		dBFS
	Next Worst Clock Spur(7)			−100		dBFS
	Calibration Side-band Coefficient(8)			100e−6		
DC ACCURACY AND PERFORMANCE						
DNL	Differential Non-Linearity			±0.3		LSB
INL	Integral Non-Linearity			±1.5		LSB
	Offset Error			±2.0		mV
	Gain Error			2		% of FS
DYNAMIC PERFORMANCE						
BW	Large-Signal Bandwidth			210		MHz
t_{AJ}	Aperture Jitter			0.5		ps(rms)
ANALOG INPUT CHARACTERISTICS						
R_{IN} (SE)	Single Ended Input Resistance			500		Ω
C_{IN} (SE)	Single Ended Capacitance			3.6		pF
ENCODE INPUT CHARACTERISTICS						
V_{IH}	Logic Input High Voltage(9)(10)		**3.9**		**4.5**	V
V_{IL}	Logic Input Low Voltage(9)(10)		**3.0**		**3.8**	V
	Differential Input Swing(9)		**0.2**			V
I_{IL}	Logic Input Low Current			2		µA
I_{IH}	Logic Input High Current			25		µA
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Logic Output High Voltage(11)	I_{OH} = 50 µA	3.2			V
V_{OL}	Logic Output Low Voltage(11)	I_{OL} = 50 µA			0.1	V
TIMING (C_L = 7pF DATA; 18pF DAV)						
	Max conversion rate (ENCODE)(11)(12)		**52**			MSPS

(5) 4th or higher harmonic.
(6) Low frequency dither injected in the DC to 500 kHz band.
(7) Next worst clock spur is a subharmonic of fs, but not fs/8 or fs/4. See text on Harmonics and Clock Spurious.
(8) See text on calibration sidebands in the CLC5958 Application Information section.
(9) Values specified based on characterization and simulation.
(10) Encode levels are referenced to V_{CC}, i.e., the minimum V_{IH} value is 1.1V below V_{CC}, and the maximum V_{IH} value is 0.5V below V_{CC}.
(11) These parameters are 100% tested at 25°C.
(12) These parameters are sample tested at full temperature range.

Converter Electrical Characteristics (continued)

The following specifications apply for V_{CC} = +5V, DV_{CC} = +3.3V, 52 MSPS. **Boldface limits apply for $T_A = T_{min}$ = −40°C to T_{max} = +85°C,** all other limits T_A = 25°C(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Min conversion rate (ENCODE)			20		MSPS
t_P	Pulse width high (ENCODE)(9)	50% threshold	**9.5**			ns
t_M	Pulse width low (ENCODE)(9)	50% threshold	**9.5**			ns
t_{DNV}	ENCODE rising edge to DATA not valid(9)		**4.5**			ns
t_{DGV}	ENCODE rising edge to DATA ensured valid(9)				**13.0**	ns
t_{DAV}	Falling ENCODE to rising DAV delay(9)	50% threshold	**7.7**		**13.5**	ns
t_S	DATA setup time before rising DAV(9)		**t_P−0.8**			ns
t_H	DATA hold time after rising DAV(9)		**t_M−4.7**			ns
	Pipeline latency			3.0		clk cycle
t_A	Effective aperture delay			−0.2		ns
SUPPLY CHARACTERISTICS						
	+5V Supply Current (V_{CC})(11)(12)			260	**300**	mA
	+3.3V Supply Current (DV_{CC})(11)(12)			32	**40**	mA
	Power Dissipation			1.4		W
	V_{CC} Power Supply Rejection Ratio			0.75		mV/V

Typical Performance Characteristics

(V_{CC} = +5V), 52 MSPS; unless specified

Single-Tone Output Spectrum

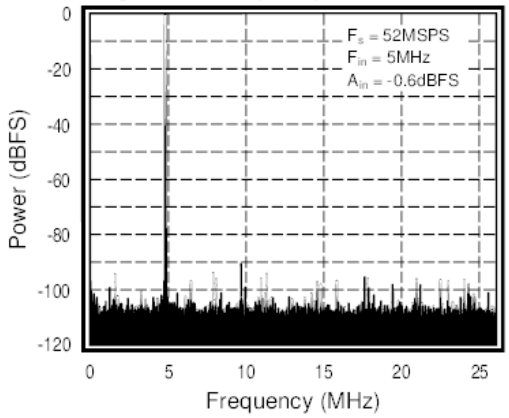


Figure 2.

Single-Tone Output Spectrum

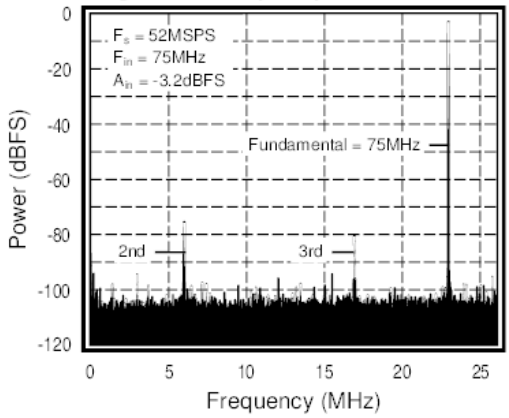


Figure .

Figure 3.

Single-Tone Output Spectrum (w/Dither)

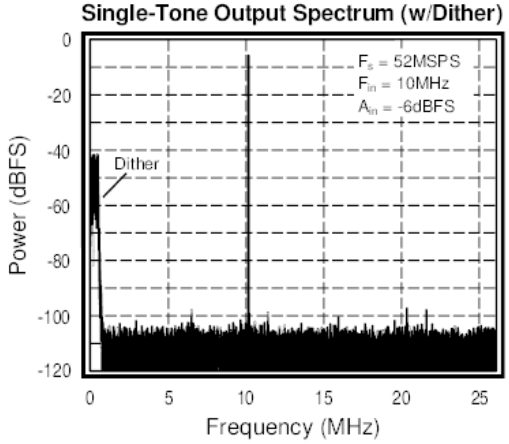


Figure 4.

Single-Tone Output Spectrum w/200KHz Res. BW

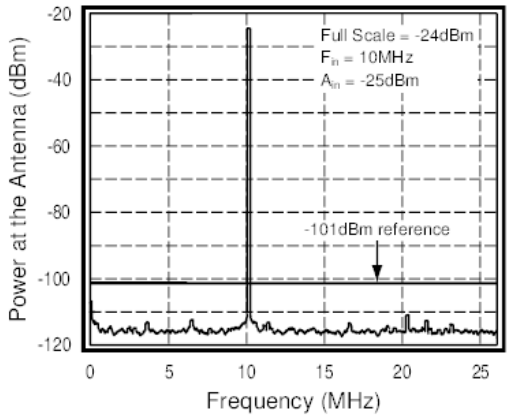


Figure 5.

Two-Tone Output Spectrum

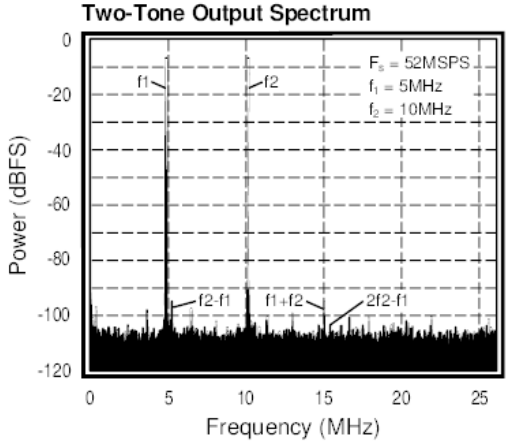


Figure 6.

Two-Tone Output Spec. w/200KHz Res. BW

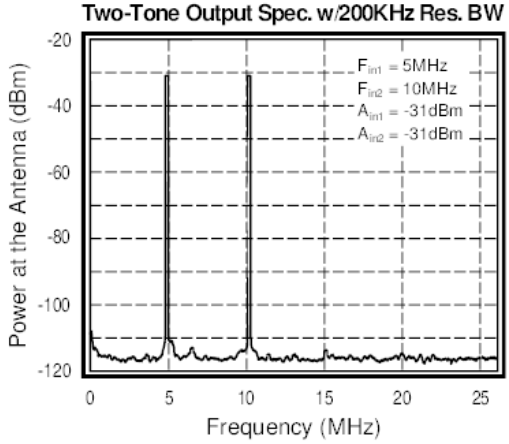


Figure 7.

Typical Performance Characteristics (continued)

(V_{CC} = +5V), 52 MSPS; unless specified

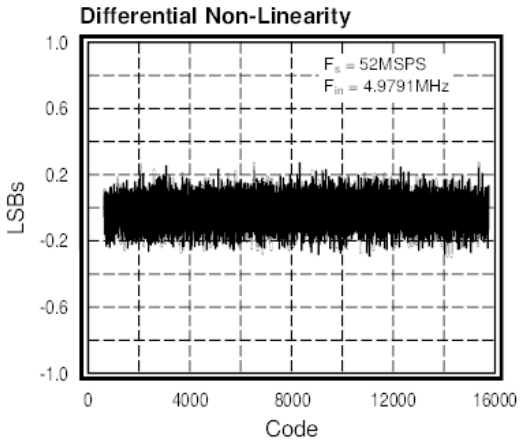
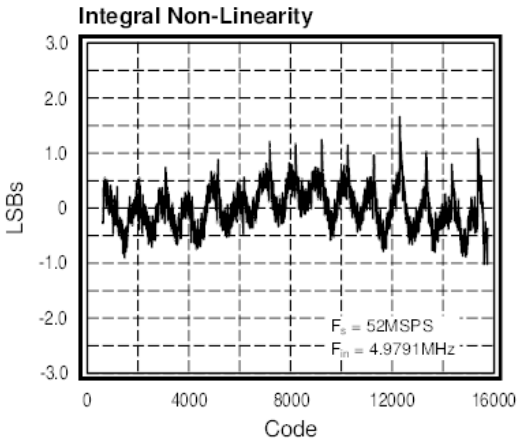


Figure 8.



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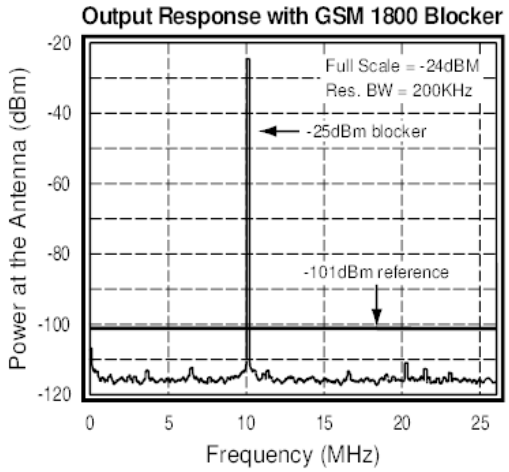

Figure 10.

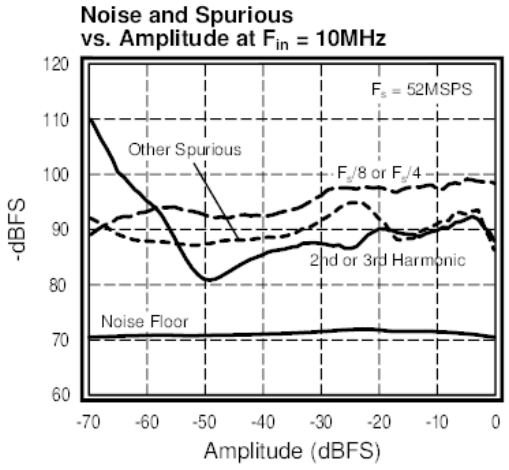

Figure 11.

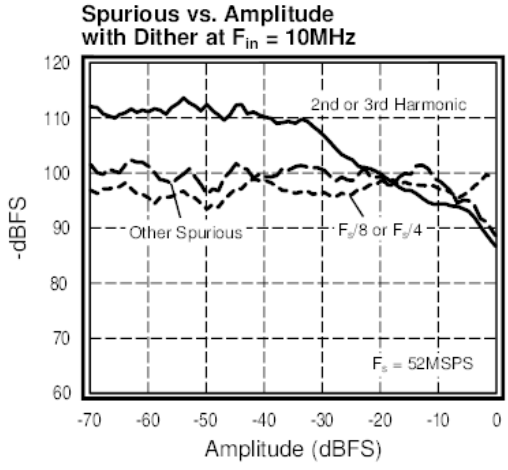

Figure 12.

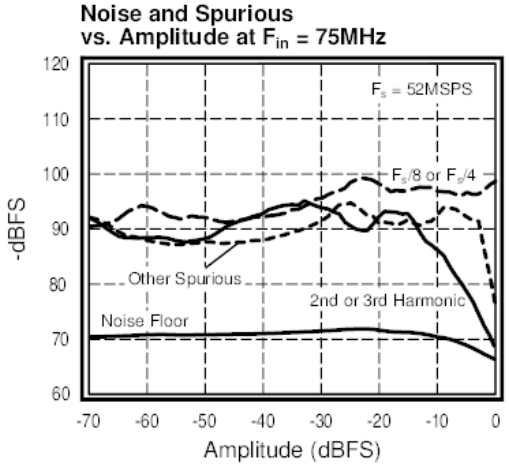

Figure 13.

Typical Performance Characteristics (continued)

(V_{CC} = +5V), 52 MSPS; unless specified

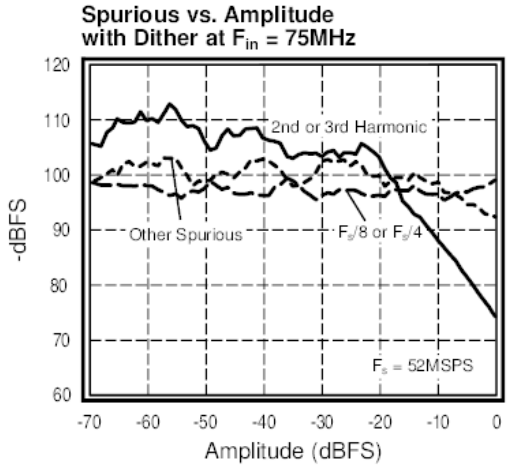

Figure 14.

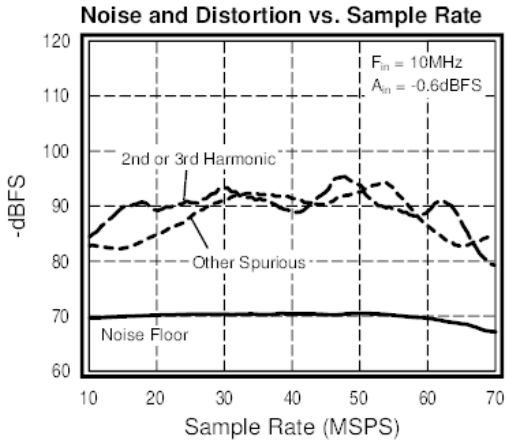

Figure 15.

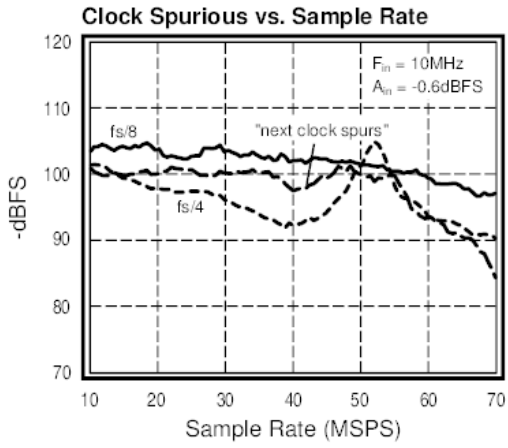

Figure 16.

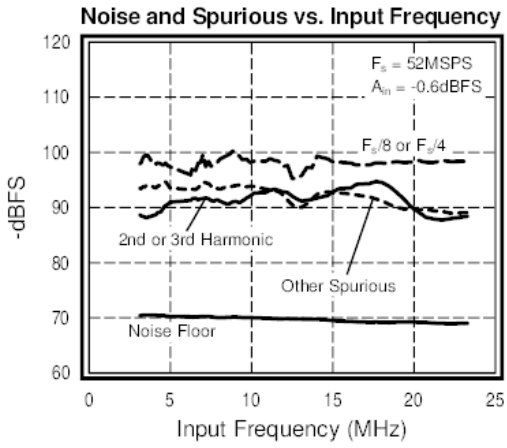

Figure 17.

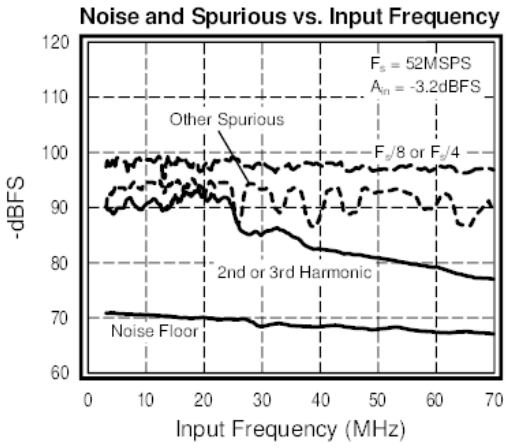

Figure 18.

TIMING DIAGRAM

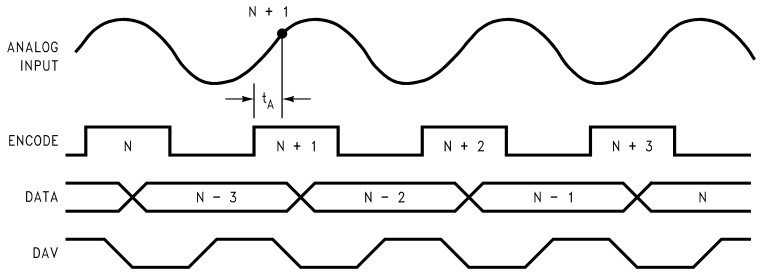

Figure 19. CLC5958 Aperture Delay Diagram
t_A: Effective Aperture Delay Nominally - 0.2ns

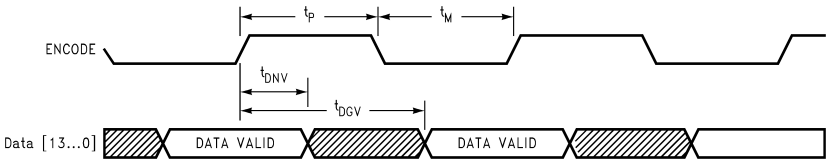

Figure 20. CLC5958 ENCODE to Data Timing Diagram

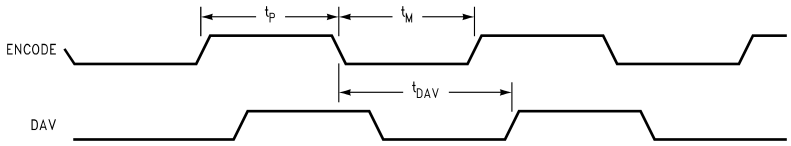

Figure 21. CLC5958 ENCODE to DAV Timing Diagram

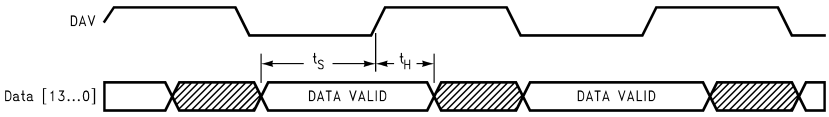

Figure 22. CLC5958 DAV to Data Timing Diagram

CLC5958 Application Information

Driving the Analog Inputs

The differential analog inputs, A_{IN} and $\overline{A_{IN}}$, are biased from an internal 3.25V reference (a 2.4V bandgap reference plus a diode) through an on-chip resistance of 500Ω. This bias voltage is set for optimum performance, and varies with temperature. Since DC coupling the inputs overrides the internal common mode voltage, it is recommended that the inputs to the CLC5958 be AC coupled whenever possible. The time constant of the input coupling network must be greater than 1 µs to minimize distortion due to nonlinear input bias currents. Additionally, the common mode source impedance should be less than 100Ω at the sample rate.

If DC coupling is required, then the V_{CM} output may be used to establish the input common mode voltage. The CLC5958 samples the common mode voltage at the internal track-and-hold output and servos the V_{CM} output to establish the optimum common mode potential at the track-and-hold. It is possible to use the V_{CM} output to construct an external servo loop.

Figure 23 illustrates one input coupling method. The transformer provides noiseless single-ended to differential conversion. The two 50Ω resistors in the secondary define the input impedance and provide a low common mode source impedance through the bypass capacitors.

Alternatively, the inputs can be driven using a differential amplifier as shown in Figure 24.

The network of Figure 24 uses a simple RC low-pass filter to roll off the noise of the differential amplifier. The network has a cutoff frequency of 40 MHz. Different noise filter designs are required for different applications. For example, an IF application would require a band-pass noise filter.

The analog input lines should be routed close together so that any coupling from other sources is common mode.

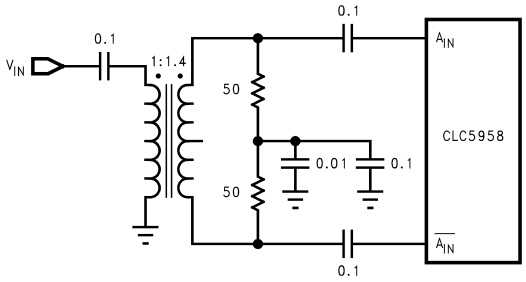

Figure 23. Input Coupling

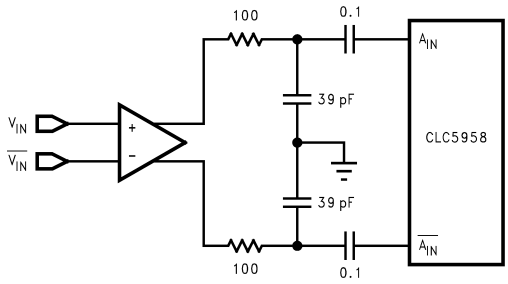

Figure 24. Differential Amplifier

Driving the ENCODE Inputs

The ENCODE and $\overline{\text{ENCODE}}$ inputs are differential clock inputs that are referenced to V_{CC}. They may be driven with PECL input levels. Alternatively they may be driven with a differential input (e.g. a sine input) that is centered at 1.2V below V_{CC} and which meets the min and max ratings for V_{IL} and V_{IH}. Low noise differential clock signals provide the best SNR performance for the converter.

The ENCODE inputs are not self-biasing, so a DC bias current path must be provided to each of the inputs.

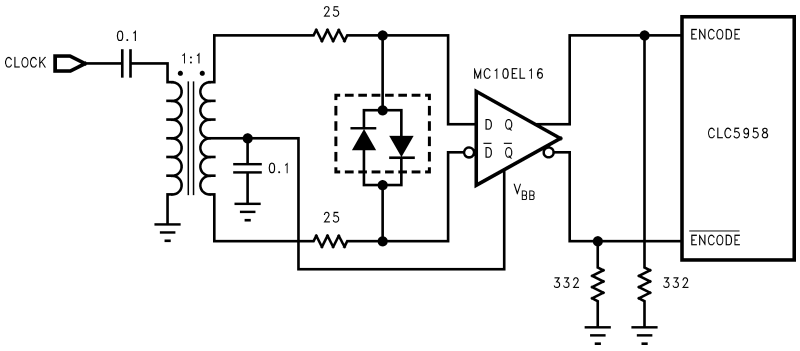

Figure 25. Encode Inputs

Figure 25 shows one method of driving the encode inputs.

The transformer converts the single-ended clock signal to a differential signal. The center-tap of the secondary is biased by the V_{BB} potential of the ECL buffer. The diodes in the secondary limit the input swing to the buffer.

Since the encode inputs are close to the analog inputs, it is recommended that the analog inputs be routed on the top of the board directly over a ground plane and that the encode lines be routed on the back of the board and then connected through via to the encode inputs.

Latching the Output Data

The rising edge of DAV is approximately centered in the data transition window, and may be used to latch the output data. The DAV output has twice the load driving capability of the data outputs so that two latch clock inputs may be driven by this output.

Routing Output Data Lines

It is recommended that the ground plane be removed under the data output lines to minimize the capacitive loading of these lines. In some systems this may not be permissible because of EMI considerations.

Harmonics and Clock Spurious

Harmonics are created by non-linearity in the track-and-hold and the quantizer. Harmonics that arise from repetitive non-linearities in the quantizer may be reduced by the application of a dither signal.

Transformers and baluns can contribute harmonic distortion, particularly at low frequencies where transformer operation relies on magnetic flux in the core. If a transformer is used to perform single ended to differential conversion at the input, care should be taken in the selection of the transformer.

The clock is internally divided by the CLC5958 in order to generate internal control signals. These divided clocks can contribute spurious energy, principally at fs/4 and fs/8. The clock spurious is typically less than −90 dBFS.

Calibration Sidebands

The CLC5958 incorporates on-board calibration. The calibration process creates low level sideband spurious close to the carrier and near DC for some input frequencies. In most applications these sidebands will not be an issue. The sidebands add negligible power to the carrier and therefore do not reduce sensitivity in receiver applications. Also, the sidebands never fall in adjacent channels with any appreciable power. They may be visible in some very narrow-band applications, and so are documented here for completeness.

The offset of the sidebands relative to the carrier and relative to DC is derived using the equations:

$$n = \text{round}\left(\frac{32\, f_{IN}}{f_S}\right) \qquad f_\Delta = \left| f_{IN} - \frac{n\, f_S}{32} \right|$$

where

- f_Δ is the sideband offset
- f_{IN} is the input frequency
- f_S is the sample rate
- and *round*(•) denotes integer rounding

(1)

The magnitude of the sideband relative to the carrier for a full scale input tone is approximated by the equations

$$x = 1024\pi f_\Delta / f_S \qquad a_\Delta = \alpha \left| \frac{\sin(x)}{x} \right|$$

where

- a_Δ is the sideband magnitude relative to the input
- α is the calibration sideband coefficient

(2)

The value of α rolls off 2 dB per dB as the input amplitude is reduced.

For example, assume the input frequency is 4.8671 MHz and the sample rate is 52 MSPS. Then the sideband offset is derived as follows:

$$n = \text{round}\left(\frac{32 * 4.8671e^6}{52e^6}\right) = 3$$

$$f_\Delta = \left| 4.8671e^6 - \frac{3 * 52e^6}{32} \right| = 7.9\ \text{kHz}$$

(3)

If the input is a full scale input, then the magnitude of the sidebands is derived as:

$$x = 1024\,\pi 7.9e^{3}/52e^{6} = 0.489$$

$$a_{\Delta} = 100e^{-6} * \left| \frac{\sin(0.489)}{0.489} \right| = 96e^{-6} = -80\,\text{dBc} \quad (4)$$

The sidebands roll off rapidly with increasing sideband offset. For example, if the sideband is offset 200 kHz from the carrier (in an adjacent GSM channel) as opposed to the 7.9 kHz offset from the previous example, the sideband magnitude is reduced to −116 dBc.

Figure 26 shows how the sideband offset frequency varies with input frequency at a sample rate of 52 MSPS.

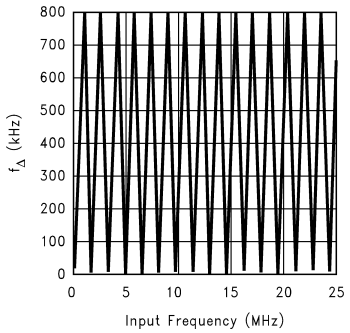

Figure 26. Sideband Offset vs. Input Frequency

The sideband magnitude is a function of the sideband offset, as illustrated in Figure 27.

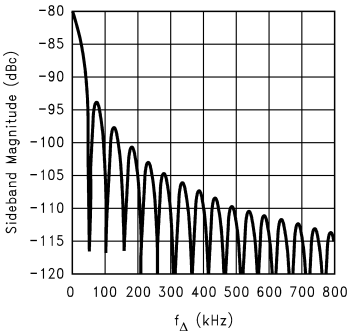

Figure 27. Sideband Magnitude vs. Sideband Offset

Power Supplies

The V_{CC} pins supply power to all of the CLC5958 circuitry with the exception of the digital output buffers. The DV_{CC} pins provide power to the digital output buffers. Each supply pin should be connected to a supply (i.e., do not leave any supply pins floating).

Local groups of supply pins should be bypassed with 0.01 µF capacitors. These capacitors should be placed as close to the part as possible. Avoid using via to the ground plane. If vias to the ground plane cannot be avoided, then use multiple vias in close proximity to the bypass capacitor.

The supplies should be bypassed in a manner to prevent supply return currents from flowing near the analog inputs. The evaluation board layout is an example of how to accomplish this.

The digital output buffer supplies (DV_{CC}) provide a means for programming the output buffer high level. Supply values ranging from 3.3V to 5.0V may be applied to these pins. In general, best performance is achieved with DV_{CC} set to 3.3V.

Layout Recommendations for the PLGA

The 48-lead chip scale package not only provides a small footprint, but also provides an excellent connection to ground. The thermal vias on the bottom of the package also serve as additional ground pads. The solder pad dimensions on the pc board should match the package pads 1:1.

Soldering Recommendations for the PLGA

A 4 mil thick stencil for the solder screen printing is recommended. The suggested IR reflow profile is:

Ramp Up:	2°C/sec
Dwell Time > 183°C:	75 sec
Solder Temperature:	215°C
(max solder temperature):	235°C
Dwell Time @ Max. Temp:	5 sec
Ramp Down:	2°C/sec

Minimum Conversion Rate

This ADC is optimized for high-speed operation. The internal bipolar track and hold circuits will cause droop errors at low sample rates. The point at which these errors cause a degradation of performance is listed on the specifications page as the minimum conversion rate. If a lower sample rate is desired, the ADC should be clocked at a higher rate, and the output data should be decimated. For example, to obtain a 10MSPS output, the ADC should be clocked at 20MHz, and every other output sample should be used. No significant power savings occurs at lower sample rates, since most of the power is used in analog circuits rather than digital circuits.

Evaluation Board

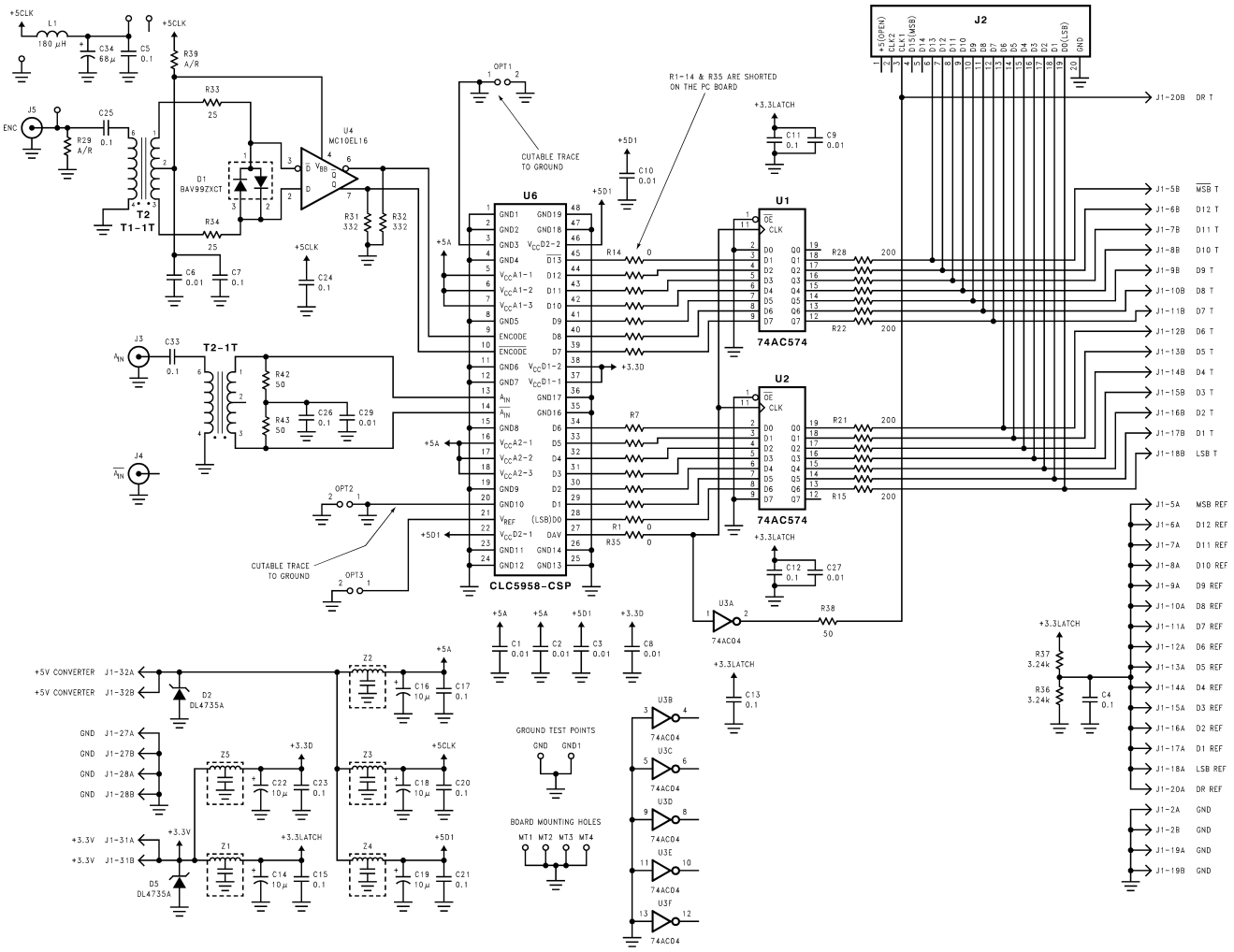

Figure 28. Evaluation Board Schematic

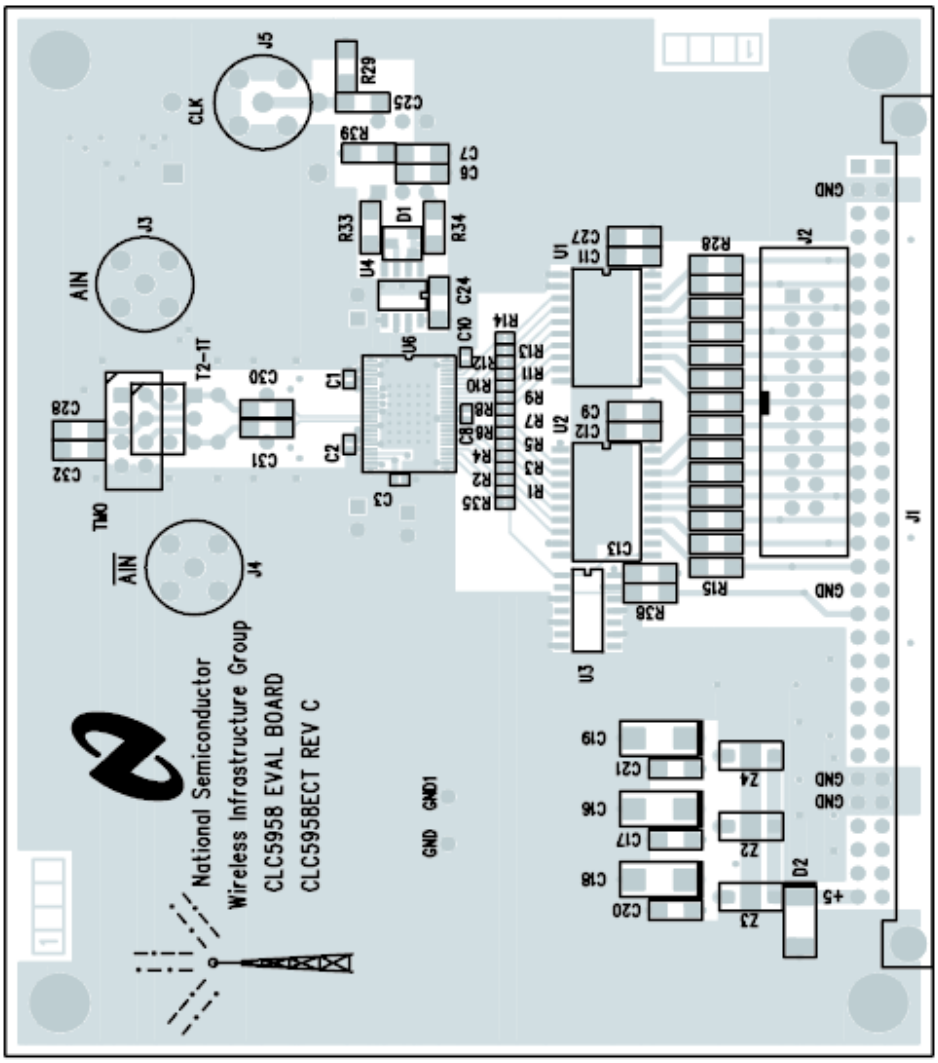

Figure 29. CLC5958PCASM Layer 1

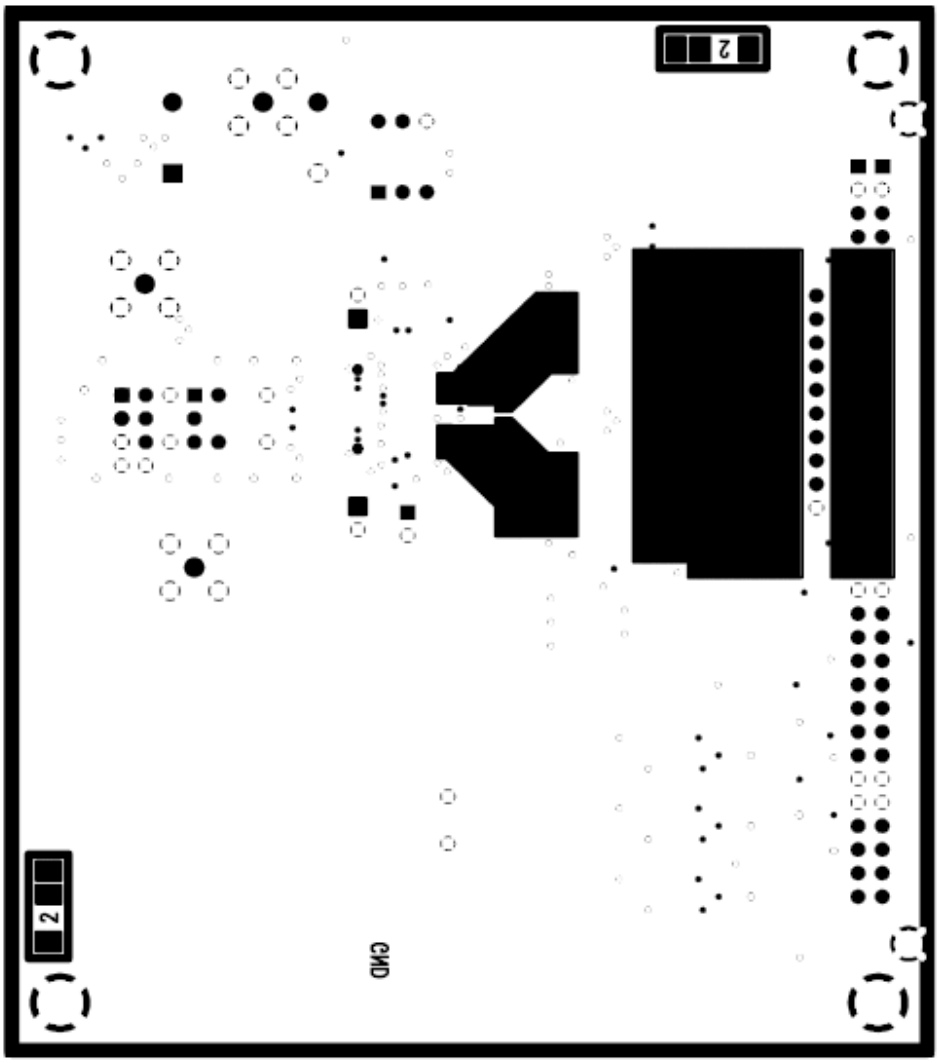

Figure 30. CLC5958PCASM Layer 2

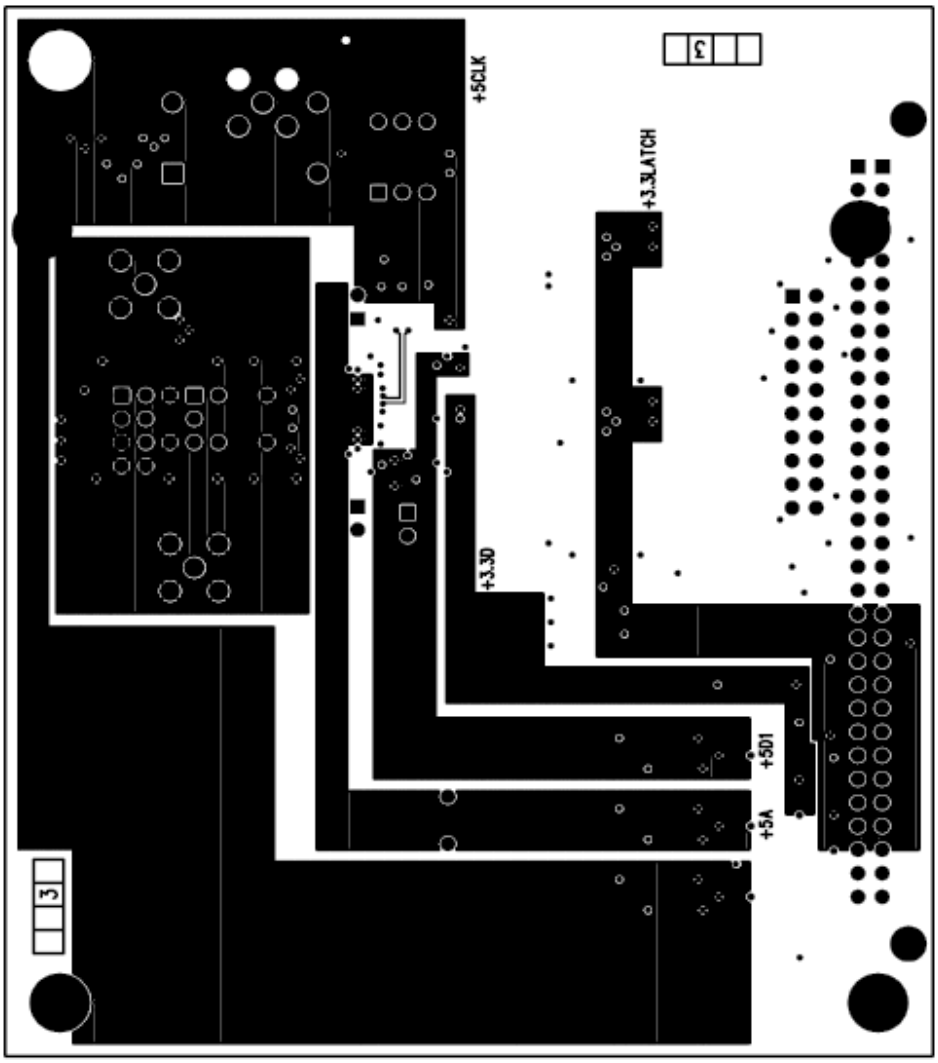

Figure 31. CLC5958PCASM Layer 3

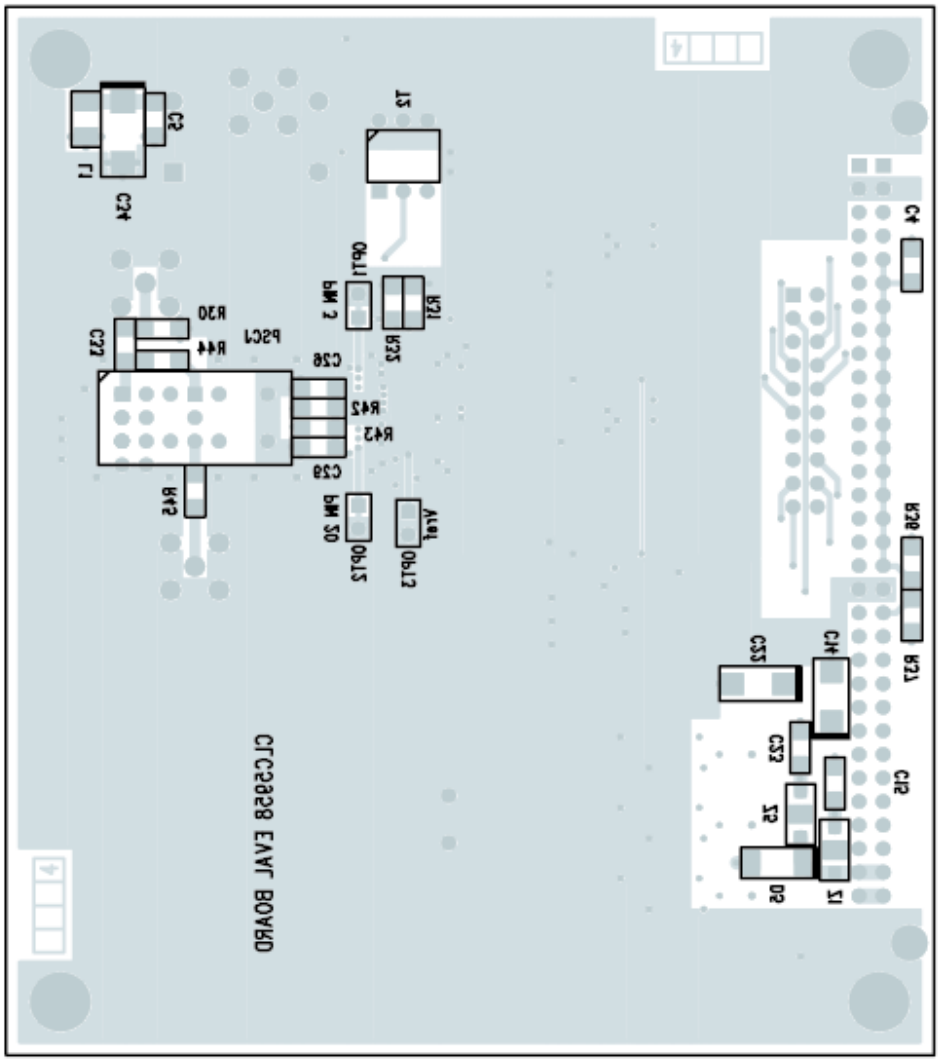

Figure 32. CLC5958PCASM Layer 4

Evaluation Printed Circuit Board

The CLC5958 evaluation printed circuit board provides a convenient test bed for rapid evaluation of the CLC5958. It illustrates the proper approach to layout in order to achieve best performance, and provides a performance benchmark.

Analog Input

The CLC5958 evaluation board is configured to be driven by a single-ended signal at the AIN SMA connector (the AIN connector is disconnected). The AIN SMA connector should be driven from a 50Ω source impedance. A full scale input is approximately 1.4 V_{PP} (7 dBm). The single-ended input is converted to a differential input by an on-board transformer.

When performing sine wave testing, it is critical that the input sine wave be filtered to remove harmonics and source noise.

Encode Input

The CLK SMA connector is the encode input and should also be driven from a 50Ω source. A low jitter 16 dBm sine wave should be applied at this input. In some cases it may be necessary to band-pass filter the sine wave in order to achieve low jitter.

The single-ended clock input is converted to a differential signal by an on-board transformer and buffered by an ECL buffer.

Digital Outputs

The digital outputs are available at the Eurocard connector (J1). Data bits D0 through $\overline{D13}$ are available at J1 pins 18B through 5B. The data ready signal (labeled DR in the schematic) is available at J1 pin 20B. These outputs are also available at the HP 01650-63203 termination adapter for direct connection to an HP logic analyzer (see Figure 28). The outputs are buffered by 3.3V digital latches. The falling edge of the data ready signal may be used to latch the output data.

Supply Voltages

Power is sourced to the board through the Eurocard connector. A 5V supply should be connected at J1 pins 32A and 32B. A 3.3V supply should be connected at J1 pins 31A and 31B. The ground return for these supplies is at J1 pins 27A, 27B, 28A, and 28B. It is recommended that low noise linear supplies be used.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	19

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