



## **Excellent Integrated System Limited**

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Texas Instruments](#)  
[DS90CR583MTD](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

## DS90CR583/DS90CR584 LVDS 24-Bit Color Flat Panel Display (FPD) Link— 65 MHz

Check for Samples: [DS90CR583](#), [DS90CR584](#)

### FEATURES

- 20 to 65 MHz Shift clk Support
- Up to 227 Mbytes/s Bandwidth
- Cable Size is Reduced to Save Cost
- 290 mV Swing LVDS Devices for Low EMI
- Low Power CMOS Design (< 550 mW typ)
- Power-Down Mode Saves Power (< 0.25 mW)
- PLL Requires No External Components
- Low Profile 56-lead TSSOP Package
- Rising Edge Data Strobe
- Compatible with TIA/EIA-644 LVDS Standard
- Single Pixel Per Clock XGA (1024 x 768)
- Supports VGA, SVGA, XGA and Higher
- 1.8 Gbps Throughput

### DESCRIPTION

The DS90CR583 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR584 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CONTROL) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 227 Mbytes per second. These devices are offered with rising edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

### BLOCK DIAGRAM

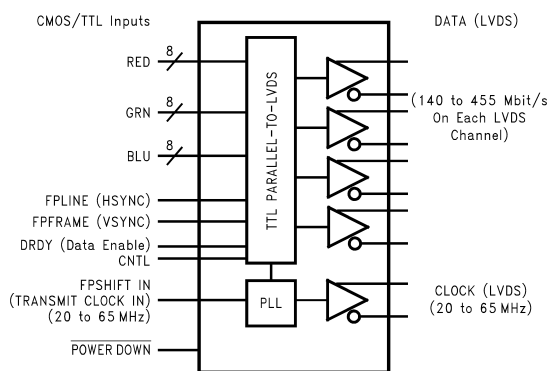


Figure 1. DS90CR583  
See Package Number DGG

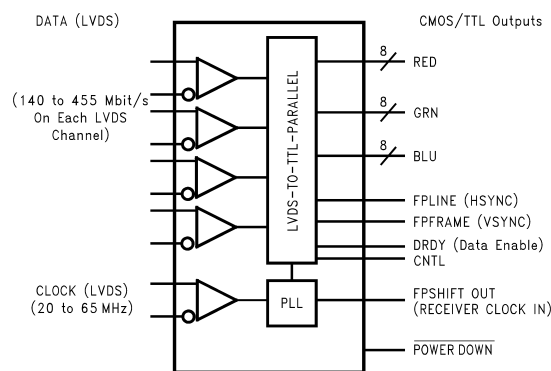


Figure 2. DS90CR584  
See Package Number DGG



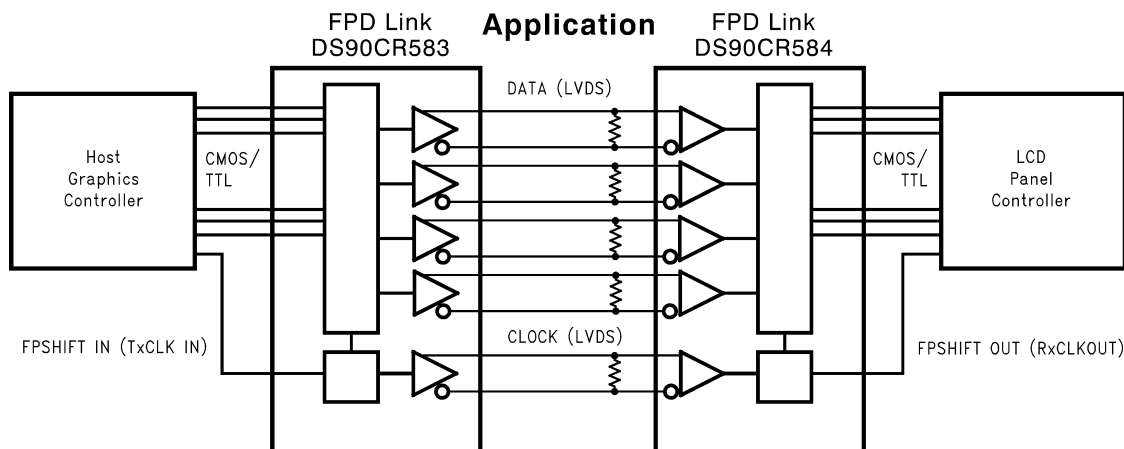
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

## DS90CR583, DS90CR584

SNLS110B – JULY 1997 – REVISED APRIL 2013

www.ti.com



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

Supply Voltage ( $V_{CC}$ )	-0.3V to +6V		
CMOS/TTL Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )		
CMOS/TTL Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )		
LVDS Receiver Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )		
LVDS Driver Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )		
LVDS Output Short Circuit Duration	Continuous		
Junction Temperature	+150°C		
Storage Temperature	-65°C to +150°C		
Lead Temperature (Soldering, 4 sec)	+260°C		
Maximum Power Dissipation @ 25°C	DGG (TSSOP) Package:	DS90CR583	1.63W
		DS90CR584	1.61W
	Package Derating:	DS90CR583	12.5 mW/°C above +25°C
		DS90CR584	12.4 mW/°C above +25°C
This device does not meet 2000V ESD rating <sup>(3)</sup> .			

- "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.
- If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- ESD Rating: HBM (1.5 kΩ, 100 pF) PLL  $V_{CC} \geq 1000V$  All other pins  $\geq 2000V$  EIAJ (0Ω, 200 pF)  $\geq 150V$

### Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage ( $V_{CC}$ )	4.75	5.0	5.25	V
Operating Free Air Temperature ( $T_A$ )	-10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage ( $V_{CC}$ )			100	mV <sub>P-P</sub>

### ELECTRICAL CHARACTERISTICS

over recommended operating supply and temperature ranges unless otherwise specified rating free-air temperature range (unless otherwise noted)

Symb	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS/TTL DC SPECIFICATIONS</b>						
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V

**ELECTRICAL CHARACTERISTICS (continued)**

over recommended operating supply and temperature ranges unless otherwise specified rating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
$V_{IL}$	Low Level Input Voltage		GND		0.8	V	
$V_{OH}$	High Level Output Voltage	$I_{OH} = -0.4$ mA	3.8	4.9		V	
$V_{OL}$	Low Level Output Voltage	$I_{OL} = 2$ mA		0.1	0.3	V	
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA		-0.79	-1.5	V	
$I_{IN}$	Input Current	$V_{IN} = V_{CC}, GND, 2.5V$ or $0.4V$		$\pm 5.1$	$\pm 10$	$\mu A$	
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V$			-120	mA	
<b>LVDS DRIVER DC SPECIFICATIONS</b>							
$V_{OD}$	Differential Output Voltage	$R_L = 100\Omega$	250	290	450	mV	
$\Delta V_{OD}$	Change in $V_{OD}$ between Complementary Output States				35	mV	
$\Delta V_{CM}$	Change in $V_{CM}$ between Complementary Output States				35	mV	
$V_{OL}$	Low Level Output Voltage		0.9	1.01		V	
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V, R_L = 100\Omega$		-2.9	-5	mA	
$I_{OZ}$	Output TRI-STATE Current	Power Down = $0V, V_{OUT} = 0V$ or $V_{CC}$		$\pm 1$	$\pm 10$	$\mu A$	
<b>LVDS RECEIVER DC SPECIFICATIONS</b>							
$V_{TH}$	Differential Input High Threshold	$V_{CM} = +1.2V$			+100	mV	
$V_{TL}$	Differential Input Low Threshold		-100			mV	
$I_{IN}$	Input Current	$V_{IN} = +2.4V$	$V_{CC} = 5.5V$		$\pm 10$	$\mu A$	
		$V_{IN} = 0V$			$\pm 10$	$\mu A$	
<b>TRANSMITTER SUPPLY CURRENT</b>							
$I_{CCTW}$	Transmitter Supply Current, Worst Case	$R_L = 100\Omega, C_L = 5$ pF, Worst Case Pattern (Figure 3, Figure 5)	$f = 32.5$ MHz		49	63	mA
			$f = 37.5$ MHz		51	64	mA
			$f = 65$ MHz		70	84	mA
$I_{CCTG}$	Transmitter Supply Current, 16 Grayscale	$R_L = 100\Omega, C_L = 5$ pF, 16 Grayscale Pattern (Figure 4, Figure 5)	$f = 32.5$ MHz		40	55	mA
			$f = 37.5$ MHz		41	55	mA
			$f = 65$ MHz		55	67	mA
$I_{CCTZ}$	Transmitter Supply Current, Power Down	Power Down = Low			1	10	$\mu A$
$I_{CCRW}$	Receiver Supply Current, Worst Case	$C_L = 8$ pF, Worst Case Pattern (Figure 3, Figure 6)	$f = 32.5$ MHz		64	77	mA
			$f = 37.5$ MHz		70	85	mA
			$f = 65$ MHz		110	140	mA
$I_{CCRG}$	Receiver Supply Current, 16 Grayscale	$C_L = 8$ pF, 16 Grayscale Pattern (Figure 4, Figure 6)	$f = 32.5$ MHz		35	55	mA
			$f = 37.5$ MHz		37	55	mA
			$f = 65$ MHz		55	67	mA
$I_{CCRZ}$	Receiver Supply Current, Power Down	Power Down = Low			1	10	$\mu A$

**Transmitter Switching Characteristics**

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (Figure 5)		0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 5)		0.75	1.5	ns
TCIT	TxCLK IN Transition Time (Figure 7)			8	ns
TCCS	TxOUT Channel-to-Channel Skew <sup>(1)</sup> (Figure 8)			350	ps
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, $V_{CC} = 5.0V$ (Figure 11)	3.5		8.5	ns

(1) This limit based on bench characterization.

## DS90CR583, DS90CR584

SNLS110B – JULY 1997 – REVISED APRIL 2013

[www.ti.com](http://www.ti.com)

### Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
TCIP	TxCLK IN Period (Figure 9)	15	T	50	ns	
TCIH	TxCLK IN High Time (Figure 9)	0.35T	0.5T	0.65T	ns	
TCIL	TxCLK IN Low Time (Figure 9)	0.35T	0.5T	0.65T	ns	
TSTC	TxIN Setup to TxCLK IN (Figure 9)	f = 65 MHz	5	3.5		ns
THTC	TxIN Hold to TxCLK IN (Figure 9)		2.5	1.5		ns
TPDD	Transmitter Powerdown Delay (Figure 20)				100	ns
TPLLS	Transmitter Phase Lock Loop Set (Figure 13)				10	ms
TPPos0	Transmitter Output Pulse Position 0 (Figure 15)		-0.30	0	0.30	ns
TPPos1	Transmitter Output Pulse Position 1		1.70	1/7 T <sub>clk</sub>	2.50	ns
TPPos2	Transmitter Output Pulse Position 2		3.60	2/7 T <sub>clk</sub>	4.50	ns
TPPos3	Transmitter Output Pulse Position 3		5.90	3/7 T <sub>clk</sub>	6.75	ns
TPPos4	Transmitter Output Pulse Position 4		8.30	4/7 T <sub>clk</sub>	9.00	ns
TPPos5	Transmitter Output Pulse Position 5		10.40	5/7 T <sub>clk</sub>	11.10	ns
TPPos6	Transmitter Output Pulse Position 6		12.70	6/7 T <sub>clk</sub>	13.40	ns

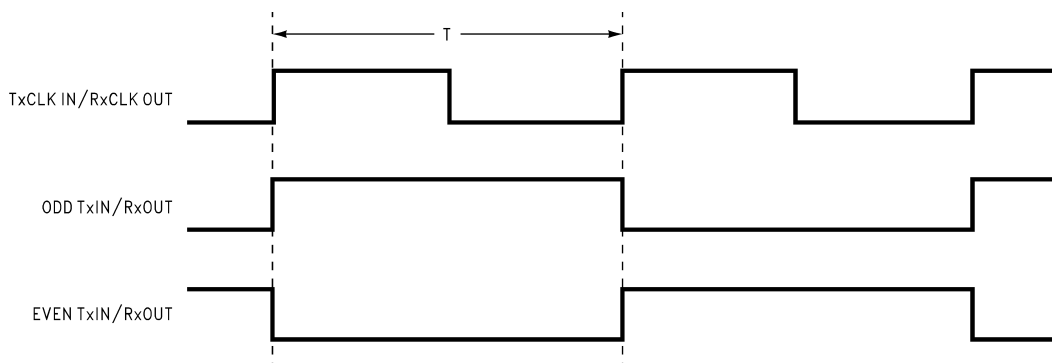
### Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 6)		2.5	4.0	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 6)		2.0	3.5	ns
RCOP	RxCLK OUT Period	15	T	50	ns
RCOH	RxCLK OUT High Time	f = 65 MHz	3.8	5	ns
RCOL	RxCLK OUT Low Time	f = 65 MHz	7.8	9	ns
RSRC	RxOUT Setup to RxCLK OUT	f = 65 MHz	2.5	4.2	ns
RHRC	RxOUT Hold to RxCLK OUT	f = 65 MHz	4.0	5.2	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V <sub>CC</sub> = 5.0V (Figure 12)	6.4		10.7	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 14)			10	ms
RSKM	RxIN Skew Margin <sup>(1)</sup> (Figure 16)	V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C	600		ps
RPDD	Receiver Powerdown (Figure 19)			1	μs

- (1) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output skew (TCCS) and the setup and hold time (internal data sampling window), allowing for LVDS cable skew dependent on type/length and source clock (TxCLK IN) jitter RSKM ≥ cable skew (type, length) + source clock jitter (cycle to cycle)

**AC Timing Diagrams**



**Figure 3. "Worst Case" Test Pattern**

Device Pin Name	Signal	Signal Pattern	Signal Frequency
TxCLK IN/RxCLK OUT	Dot Clk	[Square Wave]	f
TxIN0/RxOUT0	R0	[Square Wave]	f/16
TxIN1/RxOUT1	R1	[Square Wave]	f/8
TxIN2/RxOUT2	R2	[Square Wave]	f/4
TxIN3/RxOUT3	R3	[Square Wave]	f/2
TxIN4/RxOUT4	R4	[Steady State, Low]	Steady State, Low
TxIN5/RxOUT5	R7	[Steady State, Low]	Steady State, Low
TxIN6/RxOUT6	R5	[Steady State, Low]	Steady State, Low
TxIN7/RxOUT7	G0	[Steady State, Low]	Steady State, Low
TxIN8/RxOUT8	G1	[Square Wave]	f/16
TxIN9/RxOUT9	G2	[Square Wave]	f/8
TxIN10/RxOUT10	G6	[Square Wave]	f/4
TxIN11/RxOUT11	G7	[Square Wave]	f/2
TxIN12/RxOUT12	G3	[Steady State, Low]	Steady State, Low
TxIN13/RxOUT13	G4	[Steady State, Low]	Steady State, Low
TxIN14/RxOUT14	G5	[Steady State, Low]	Steady State, Low
TxIN15/RxOUT15	B0	[Steady State, Low]	Steady State, Low
TxIN16/RxOUT16	B6	[Square Wave]	f/16
TxIN17/RxOUT17	B7	[Square Wave]	f/8
TxIN18/RxOUT18	B1	[Square Wave]	f/4
TxIN19/RxOUT19	B2	[Square Wave]	f/2
TxIN20/RxOUT20	B3	[Steady State, Low]	Steady State, Low
TxIN21/RxOUT21	B4	[Steady State, Low]	Steady State, Low
TxIN22/RxOUT22	B5	[Steady State, Low]	Steady State, Low
TxIN23/RxOUT23	RES	[Steady State, Low]	Steady State, Low
TxIN24/RxOUT24	HSYNC	[Steady State, High]	Steady State, High
TxIN25/RxOUT25	VSYNC	[Steady State, High]	Steady State, High
TxIN26/RxOUT26	DEN	[Steady State, High]	Steady State, High
TxIN27/RxOUT27	R6	[Steady State, High]	Steady State, High

- (1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.
- (2) The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.
- (3) Figure 3 and Figure 4 show a falling edge data strobe (TxCLK IN/RxCLK OUT).
- (4) Recommended pin to signal mapping. Customer may choose to define differently.

**Figure 4. "16 Grayscale" Test Pattern**

**DS90CR583, DS90CR584**

SNLS110B - JULY 1997 - REVISED APRIL 2013

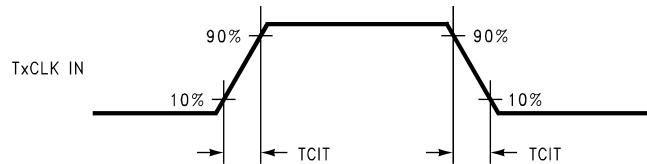
www.ti.com



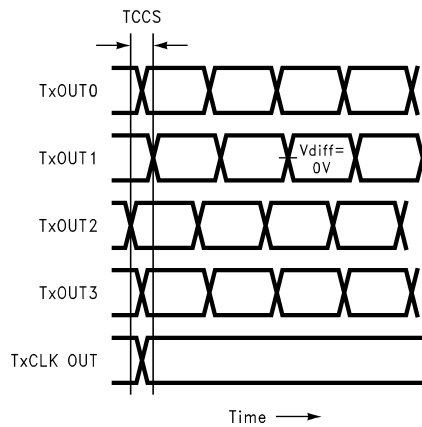
**Figure 5. DS90CR583 (Transmitter) LVDS Output Load and Transition Times**



**Figure 6. DS90CR584 (Receiver) CMOS/TTL Output Load and Transition Times**

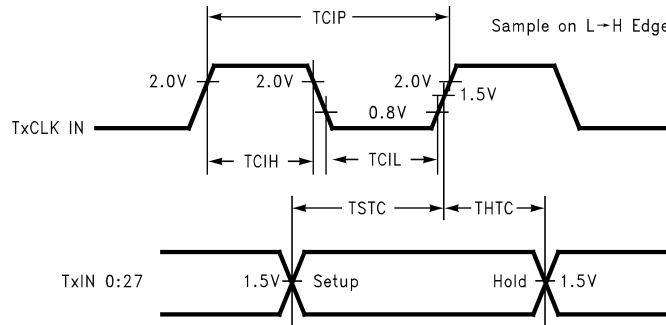


**Figure 7. DS90CR583 (Transmitter) Input Clock Transition Time**

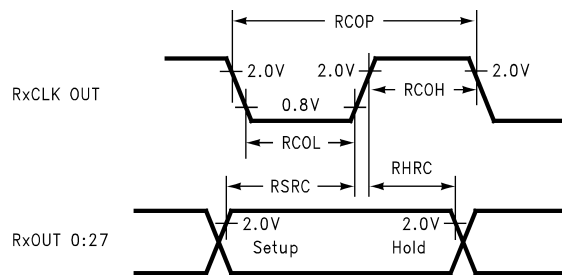


- Note:** Measurements at  $V_{diff} = 0V$
- Note:** TCCS measured between earliest and latest LVDS edges.
- Note:** TxCLK Differential High→Low Edge

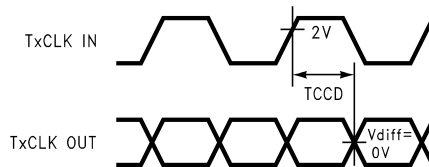
**Figure 8. DS90CR583 (Transmitter) Channel-to-Channel Skew and Pulse Width**



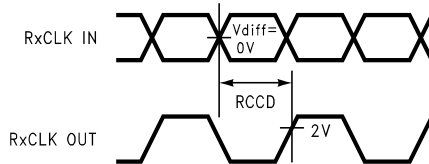
**Figure 9. DS90CR583 (Transmitter) Setup/Hold and High/Low Times**



**Figure 10. DS90CR584 (Receiver) Clock In to Clock Out Delay**



**Figure 11. DS90CR583 (Transmitter) Clock In to Clock Out Delay**



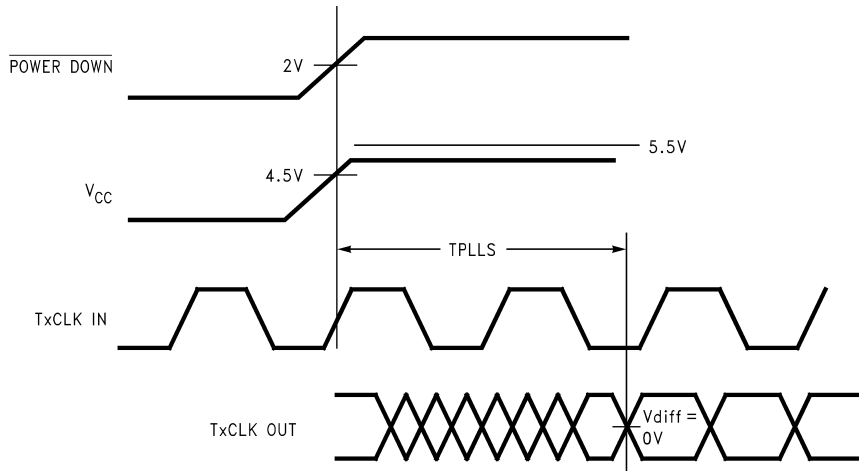
**Figure 12. DS90CR584 (Receiver) Clock In to Clock Out Delay**



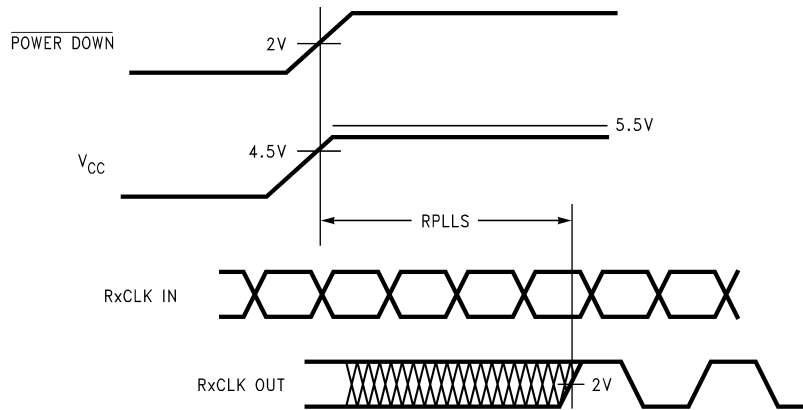
**DS90CR583, DS90CR584**

SNLS110B - JULY 1997 - REVISED APRIL 2013

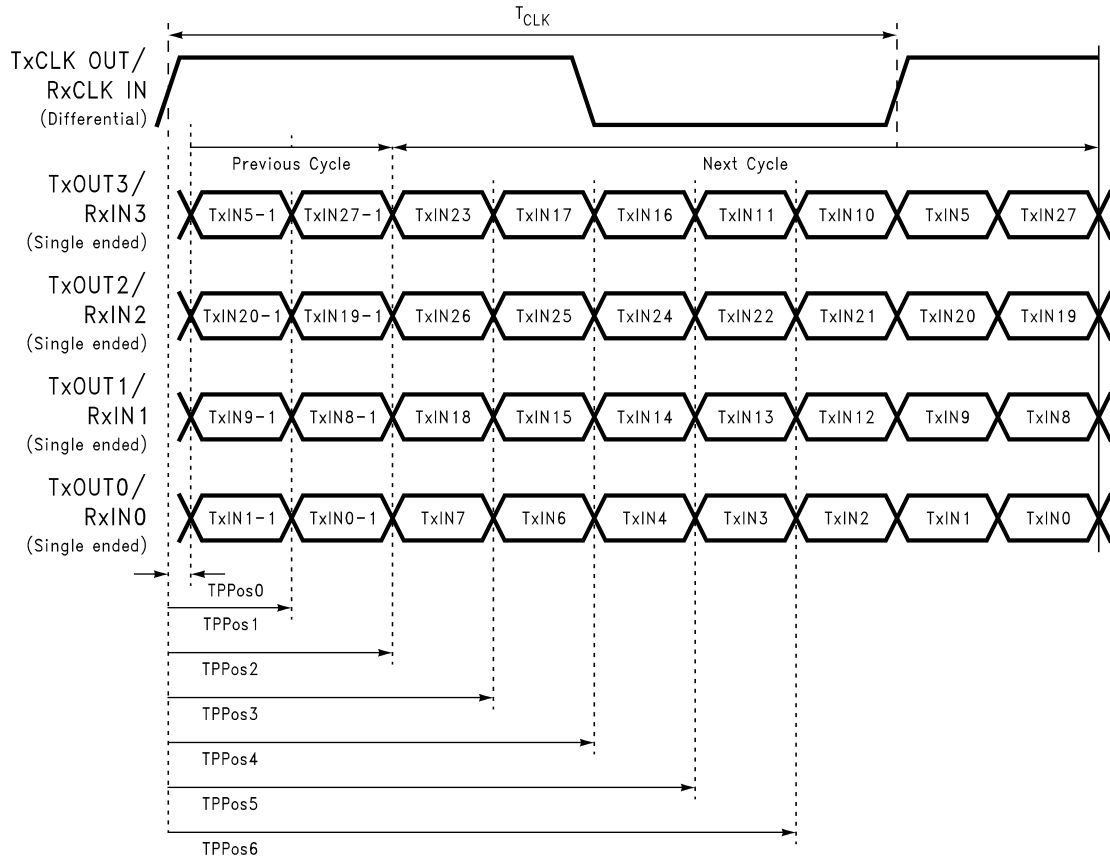
www.ti.com



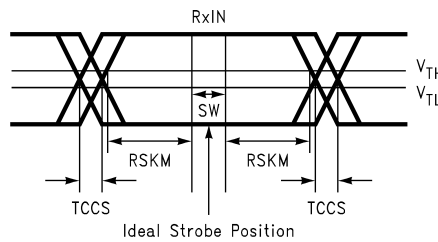
**Figure 13. DS90CR583 (Transmitter) Phase Lock Loop Set Time**



**Figure 14. DS90CR584 (Receiver) Phase Lock Loop Set Time**



**Figure 15. Transmitter LVDS Output Pulse Position Measurement**



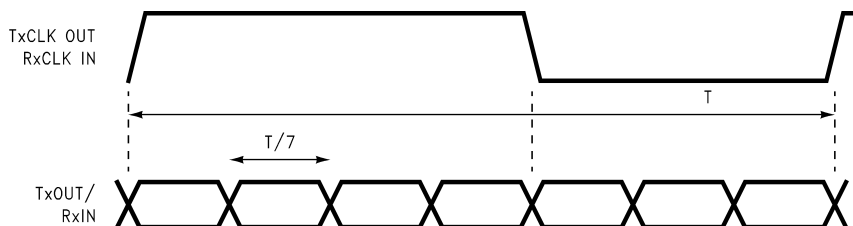
SW—Setup and Hold Time (Internal Data Sampling Window)

TCCS—Transmitter Output Skew

RSKM  $\geq$  Cable Skew (type, length) + Source Clock Jitter (cycle to cycle)

Cable Skew—typically 10 ps–40 ps per foot

**Figure 16. Receiver LVDS Input Skew Margin**



**Figure 17. Seven Bits of LVDS in One Clock Cycle**

DS90CR583, DS90CR584

SNLS110B –JULY 1997–REVISED APRIL 2013

www.ti.com

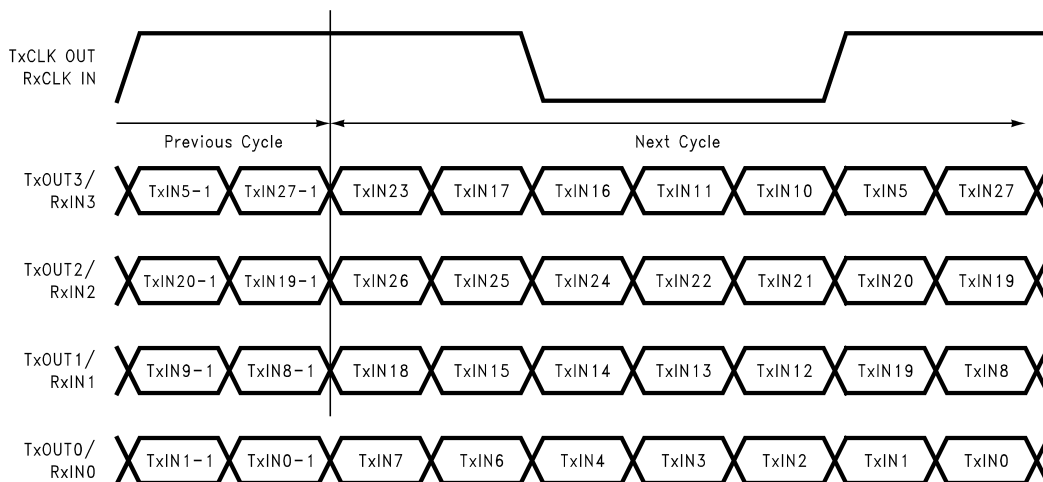


Figure 18. Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR583)

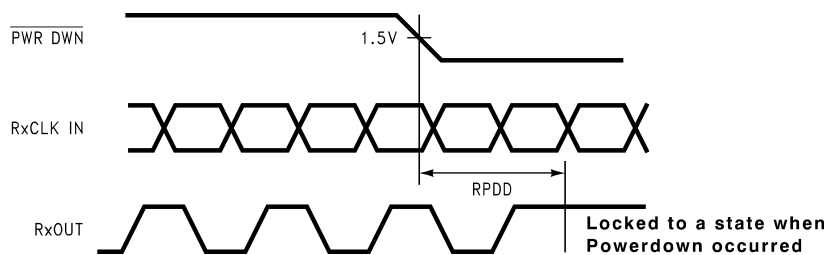


Figure 19. Receiver Powerdown Delay

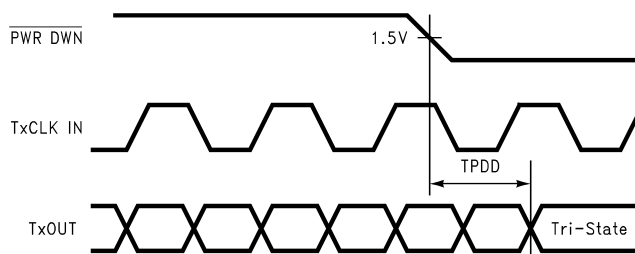


Figure 20. Transmitter Powerdown Delay

DS90CR583 Pin Descriptions—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY and CNTL (also referred to as HSYNC, VSYNC, Data Enable, CNTL)
TxOUT+	O	4	Positive LVDS differential data output
TxOUT-	O	4	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT-	O	1	Negative LVDS differential clock output
PWR DOWN	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V <sub>CC</sub>	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs

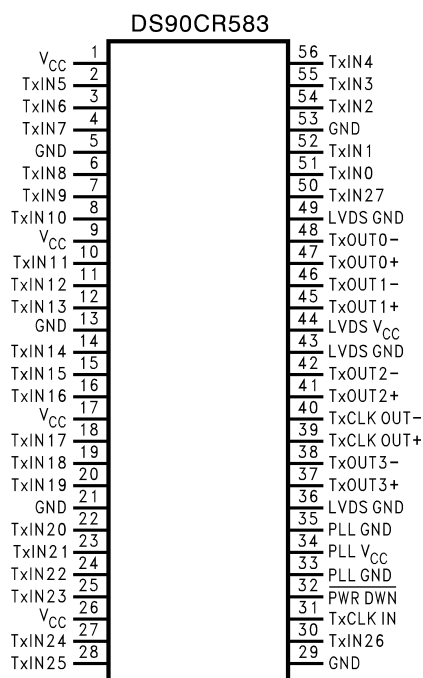
**DS90CR583 Pin Descriptions—FPD Link Transmitter (continued)**

Pin Name	I/O	No.	Description
PLL V <sub>CC</sub>	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

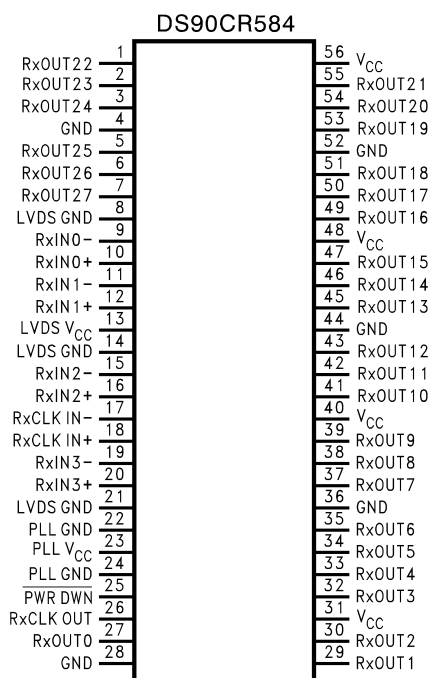
**DS90CR584 Pin Descriptions—FPD Link Receiver**

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs
RxIN-	I	4	Negative LVDS differential data inputs
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY and CNTL (also referred to as HSYNC, VSYNC, Data Enable, CNTL)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN-	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe
PWR DOWN	I	1	TTL level input. Assertion (low input) maintains the receiver outputs in the previous state
V <sub>CC</sub>	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V <sub>CC</sub>	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

**Connection Diagram**



**Figure 21. 56 Pin TSSOP**  
See Package Number DGG



**Figure 22. 56 Pin TSSOP**  
See Package Number DGG

---

## DS90CR583, DS90CR584



SNLS110B – JULY 1997 – REVISED APRIL 2013

[www.ti.com](http://www.ti.com)

---

### REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
--	------

---

- Changed layout of National Data Sheet to TI format ..... 11
-

### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

#### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

#### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

#### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)