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Texas Instruments
LM3488MM/NOPB

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# LM3488/-Q1 High-Efficiency, Low-Side, N-Channel Controller for Switching Regulators

## 1 Features

- LM3488-Q1 is AEC-Q100 Qualified and Manufactured on an Automotive-Grade Flow
- 8-Lead VSSOP Package
- Internal Push-Pull Driver With 1-A Peak Current Capability
- Current Limit and Thermal Shutdown
- Frequency Compensation Optimized With a Capacitor and a Resistor
- Internal Soft-Start
- Current Mode Operation
- Undervoltage Lockout With Hysteresis
- Key Specifications:
  - Wide Supply Voltage Range of 2.97 V to 40 V
  - 100-kHz to 1-MHz Adjustable and Synchronizable Clock Frequency
  - ±1.5% (Overtemperature) Internal Reference
  - 5-µA Shutdown Current (Overtemperature)

## 2 Applications

- Distributed Power Systems
- Notebook, PDA, Digital Camera, and other Portable Applications
- Offline Power Supplies
- Set-Top Boxes

## 3 Description

The LM3488 is a versatile low-side N-FET high-performance controller for switching regulators. This device is suitable for use in topologies requiring low-side FET, such as boost, flyback, or SEPIC. Moreover, the LM3488 can be operated at extremely high switching frequency to reduce the overall solution size. The switching frequency of LM3488 can be adjusted to any value from 100 kHz to 1 MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response, besides cycle-by-cycle current limiting. Output current can be programmed with a single external resistor.
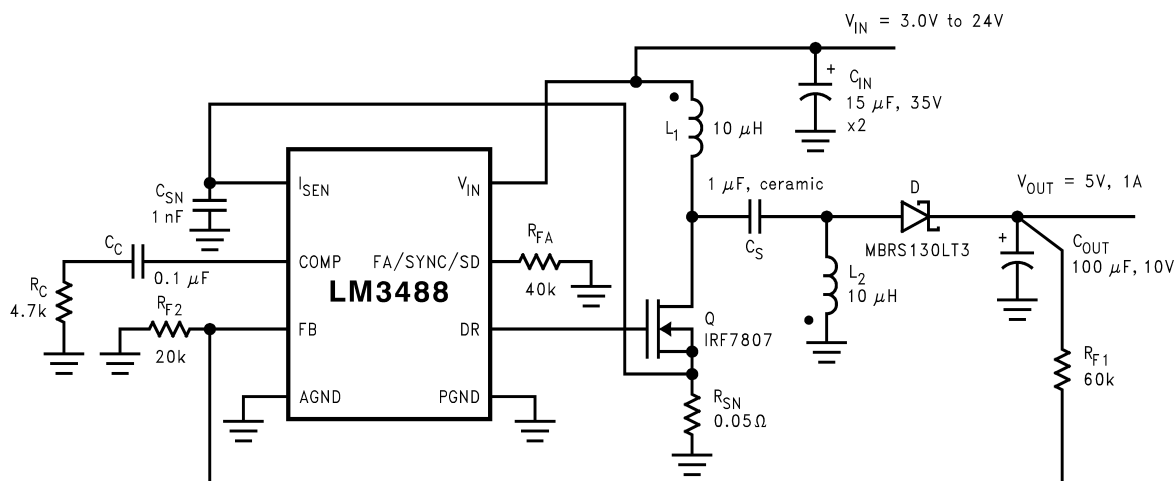
The LM3488 has built-in features such as thermal shutdown, short-circuit protection, and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 5 µA and allows power supply sequencing. Internal soft-start limits the inrush current at start-up.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LM3488 | VSSOP (8) | 3.00 mm × 3.00 mm |
| LM3488-Q1 | | |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Typical SEPIC Converter**

# Table of Contents

# 4 Revision History

**Changes from Revision M (March 2013) to Revision N**           **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ........................................................................................................................................ 1

**Changes from Revision L (March 2013) to Revision M**           **Page**

- Changed layout of National Data Sheet to TI format ....................................................................................... 29

# 5   Pin Configuration and Functions

**8-Pin DGK**
**VSSOP Package**
**Top View**

```
        ┌──────────────┐
I_SEN ──┤ 1 ●       8  ├── V_IN
COMP  ──┤ 2  LM3488  7 ├── FA/SYNC/SD
FB    ──┤ 3         6  ├── DR
AGND  ──┤ 4         5  ├── PGND
        └──────────────┘
```
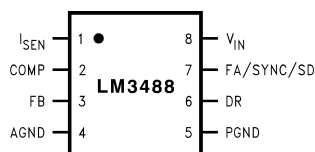
**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $I_{SEN}$ | 1 | I | Current sense input pin. Voltage generated across an external sense resistor is fed into this pin. |
| COMP | 2 | A | Compensation pin. A resistor, capacitor combination connected to this pin provides compensation for the control loop. |
| FB | 3 | I | Feedback pin. The output voltage should be adjusted using a resistor divider to provide 1.26 V at this pin. |
| AGND | 4 | P | Analog ground pin. |
| PGND | 5 | P | Power ground pin. |
| DR | 6 | O | Drive pin of the IC. The gate of the external MOSFET should be connected to this pin. |
| FA/SYNC/SD | 7 | A | Frequency adjust, synchronization, and Shutdown pin. A resistor connected to this pin sets the oscillator frequency. An external clock signal at this pin will synchronize the controller to the frequency of the clock. A high level on this pin for ≥ 30 µs will turn the device off. The device will then draw less than 10µA from the supply. |
| $V_{IN}$ | 8 | P | Power supply input pin. |

# 6   Specifications

## 6.1   Absolute Maximum Ratings [(1)]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | | | 45 | V |
| FB pin voltage | | $-0.4 < V_{FB}$ | $V_{FB} < 7$ | V |
| FA/SYNC/SD pin voltage | | $-0.4 < V_{FA/SYNC/SD}$ | $V_{FA/SYNC/SD} < 7$ | V |
| Peak driver output current (< 10 µs) | | | 1 | A |
| Power dissipation | | | Internally Limited | |
| Junction temperature | | | 150 | °C |
| Lead temperature | Vapor Phase (60 s) | | 215 | °C |
| | Infared (15 s) | | 260 | °C |
| DR pin voltage | | $-0.4 ≤ VDR$ | $VDR ≤ 8$ | V |
| $I_{LIM}$ pin voltage | | | 600 | mV |

(1)   Absolute Maximum Ratings are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics*.

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Datasheet of LM3488MM/NOPB - IC REG CTRL BST FLYBK PWM 8VSSOP
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## 6.2 Handling Ratings : LM3488

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| T_stg | Storage temperature range | | −65 | 150 | °C |
| V_(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | −2000 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | −750 | 750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Handling Ratings: LM3488-Q1

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| T_stg | Storage temperature range | | | −65 | 150 | °C |
| V_(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002[1] | | −2000 | 2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | Corner pins (1, 4, 5, and 8) | −750 | 750 | |
| | | | Other pins | −750 | 750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.4 Recommended Operating Conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Voltage | $2.97 \leq V_{IN}$ | $V_{IN} \leq 40$ | V |
| Junction Temperature Range | $-40 \leq T_J$ | $T_J \leq 125$ | °C |
| Switching Frequency | $100 \leq F_{SW}$ | $F_{SW} \leq 1$ | kHz/MHz |

## 6.5 Thermal Information

| | THERMAL METRIC[1] | LM3488, LM3488-Q1 DGK 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 160 | |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 50 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 77 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 4.7 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 76 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.6 Electrical Characteristics

Unless otherwise specified, $V_{IN}$ = 12 V, $R_{FA}$ = 40 kΩ, $T_J$ = 25°C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{FB}$ | Feedback Voltage | $V_{COMP}$ = 1.4 V, $2.97 \leq V_{IN} \leq 40$ V | 1.2507 | 1.26 | 1.2753 | V |
| | | $V_{COMP}$ = 1.4 V, $2.97 \leq V_{IN} \leq 40$ V, $-40°C \leq T_J \leq 125°C$ | 1.24 | | 1.28 | |
| $\Delta V_{LINE}$ | Feedback Voltage Line Regulation | $2.97 \leq V_{IN} \leq 40$ V | | 0.001 | | %/V |
| $\Delta V_{LOAD}$ | Output Voltage Load Regulation | $I_{EAO}$ Source/Sink | | ±0.5 | | %/V (max) |
| $V_{UVLO}$ | Input Undervoltage Lock-out | | | 2.85 | | V |
| | | $-40°C \leq T_J \leq 125°C$ | | | 2.97 | |
| $V_{UV(HYS)}$ | Input Undervoltage Lock-out Hysteresis | | | 170 | | mV |
| | | $-40°C \leq T_J \leq 125°C$ | 130 | | 210 | |

**TEXAS INSTRUMENTS**

**LM3488, LM3488-Q1**

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## Electrical Characteristics (continued)

Unless otherwise specified, $V_{IN}$ = 12 V, $R_{FA}$ = 40 kΩ, $T_J$ = 25°C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $F_{nom}$ | Nominal Switching Frequency | $R_{FA}$ = 40 KΩ | | 400 | | kHz |
| | | $R_{FA}$ = 40 KΩ, −40°C ≤ $T_J$ ≤ 125°C | 360 | | 430 | |
| $R_{DS1\ (ON)}$ | Driver Switch On Resistance (top) | $I_{DR}$ = 0.2A, $V_{IN}$= 5 V | | 16 | | Ω |
| $R_{DS2\ (ON)}$ | Driver Switch On Resistance (bottom) | $I_{DR}$ = 0.2A | | 4.5 | | Ω |
| $V_{DR\ (max)}$ | Maximum Drive Voltage Swing[1] | $V_{IN}$ < 7.2 V | | $V_{IN}$ | | V |
| | | $V_{IN}$ ≥ 7.2 V | | 7.2 | | |
| $D_{max}$ | Maximum Duty Cycle[2] | | | 100% | | |
| $T_{min}$ (on) | Minimum On Time | | | 325 | | nsec |
| | | −40°C ≤ $T_J$ ≤ 125°C | 230 | | 550 | |
| $I_{SUPPLY}$ | Supply Current (switching) | See [3] | | 2.7 | | mA |
| | | See [3], −40°C ≤ $T_J$ ≤ 125°C | | | 3.0 | |
| $I_Q$ | Quiescent Current in Shutdown Mode | $V_{FA/SYNC/SD}$ = 5 V[4], $V_{IN}$ = 5 V | | 5 | | µA |
| | | $V_{FA/SYNC/SD}$ = 5 V[4], $V_{IN}$ = 5 V, −40°C ≤ $T_J$ ≤ 125°C | | | 7 | |
| $V_{SENSE}$ | Current Sense Threshold Voltage | $V_{IN}$ = 5 V | 135 | 156 | 180 | mV |
| | | $V_{IN}$ = 5 V, −40°C ≤ $T_J$ ≤ 125°C | 125 | | 190 | |
| $V_{SC}$ | Short-Circuit Current Limit Sense Voltage | $V_{IN}$ = 5 V | | 343 | | mV |
| | | $V_{IN}$ = 5 V, −40°C ≤ $T_J$ ≤ 125°C | 250 | | 415 | |
| $V_{SL}$ | Internal Compensation Ramp Voltage | $V_{IN}$ = 5 V | | 92 | | mV |
| | | $V_{IN}$ = 5 V, −40°C ≤ $T_J$ ≤ 125°C | 52 | | 132 | |
| $V_{SL}$ ratio | $V_{SL}/V_{SENSE}$ | | 0.30 | 0.49 | 0.70 | |
| $V_{OVP}$ | Output Overvoltage Protection (with respect to feedback voltage) [5] | $V_{COMP}$ = 1.4 V | 32 | 50 | 78 | mV |
| | | $V_{COMP}$ = 1.4 V, −40°C ≤ $T_J$ ≤ 125°C | 25 | | 85 | |
| $V_{OVP(HYS)}$ | Output Over-Voltage Protection Hysteresis[5] | $V_{COMP}$ = 1.4 V | | 60 | | mV |
| | | $V_{COMP}$ = 1.4 V, −40°C ≤ $T_J$ ≤ 125°C | 20 | | 110 | |
| Gm | Error Ampifier Transconductance | $V_{COMP}$ = 1.4 V, $I_{EAO}$ = 100 µA (Source/Sink) | 600 | 800 | 1000 | µmho |
| | | $V_{COMP}$ = 1.4 V, $I_{EAO}$ = 100 µA (Source/Sink), −40°C ≤ $T_J$ ≤ 125°C | 365 | | 1265 | |
| $A_{VOL}$ | Error Amplifier Voltage Gain | $V_{COMP}$ = 1.4 V, $I_{EAO}$ = 100 µA (Source/Sink) | | 38 | | V/V |
| | | $V_{COMP}$ = 1.4 V, $I_{EAO}$ = 100 µA (Source/Sink), −40°C ≤ $T_J$ ≤ 125°C | 26 | | 44 | |
| $I_{EAO}$ | Error Amplifier Output Current (Source/Sink) | Source, $V_{COMP}$ = 1.4 V, $V_{FB}$ = 0 V | 80 | 110 | 140 | µA |
| | | Source, $V_{COMP}$ = 1.4 V, $V_{FB}$ = 0 V, −40°C ≤ $T_J$ ≤ 125°C | 50 | | 180 | |
| | | Sink, $V_{COMP}$ = 1.4 V, $V_{FB}$ = 1.4 V | −100 | −140 | −180 | µA |
| | | Sink, $V_{COMP}$ = 1.4 V, $V_{FB}$ = 1.4 V, −40°C ≤ $T_J$ ≤ 125°C | −85 | | −185 | |

(1) The voltage on the drive pin, $V_{DR}$ is equal to the input voltage when input voltage is less than 7.2 V. $V_{DR}$ is equal to 7.2 V when the input voltage is greater than or equal to 7.2 V.
(2) The limits for the maximum duty cycle can not be specified since the part does not permit less than 100% maximum duty cycle operation.
(3) For this test, the FA/SYNC/SD Pin is pulled to ground using a 40K resistor .
(4) For this test, the FA/SYNC/SD Pin is pulled to 5 V using a 40K resistor.
(5) The over-voltage protection is specified with respect to the feedback voltage. This is because the over-voltage protection tracks the feedback voltage. The over-voltage thresold can be calculated by adding the feedback voltage, $V_{FB}$ to the over-voltage protection specification.

Product Folder Links: *LM3488  LM3488-Q1*

## Electrical Characteristics (continued)

Unless otherwise specified, $V_{IN}$ = 12 V, $R_{FA}$ = 40 kΩ, $T_J$ = 25°C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{EAO}$ | Error Amplifier Output Voltage Swing | Upper Limit: $V_{FB}$ = 0 V, COMP Pin = Floating | | 2.2 | | V |
| | | Upper Limit: $V_{FB}$ = 0 V, COMP Pin = Floating, −40°C ≤ $T_J$ ≤ 125°C | 1.8 | | 2.4 | |
| | | Lower Limit: $V_{FB}$ = 1.4 V | | 0.56 | | V |
| | | Lower Limit: $V_{FB}$ = 1.4 V, −40°C ≤ $T_J$ ≤ 125°C | 0.2 | | 1.0 | |
| $T_{SS}$ | Internal Soft-Start Delay | $V_{FB}$ = 1.2 V, $V_{COMP}$ = Floating | | 4 | | ms |
| $T_r$ | Drive Pin Rise Time | Cgs = 3000 pf, $V_{DR}$ = 0 to 3 V | | 25 | | ns |
| $T_f$ | Drive Pin Fall Time | Cgs = 3000 pf, $V_{DR}$ = 0 to 3 V | | 25 | | ns |
| VSD | Shutdown and Synchronization signal threshold [6] | Output = High | | 1.27 | | V |
| | | Output = High, −40°C ≤ $T_J$ ≤ 125°C | | | 1.4 | |
| | | Output = Low | | 0.65 | | V |
| | | Output = Low, −40°C ≤ $T_J$ ≤ 125°C | 0.3 | | | |
| $I_{SD}$ | Shutdown Pin Current | $V_{SD}$ = 5 V | | −1 | | µA |
| | | $V_{SD}$ = 0 V | | +1 | | |
| $I_{FB}$ | Feedback Pin Current | | | 15 | | nA |
| TSD | Thermal Shutdown | | | 165 | | °C |
| $T_{sh}$ | Thermal Shutdown Hysteresis | | | 10 | | °C |

(6)    The FA/SYNC/SD pin should be pulled to $V_{IN}$ through a resistor to turn the regulator off.

**TEXAS INSTRUMENTS**

**LM3488, LM3488-Q1**

## 6.7 Typical Characteristics

Unless otherwise specified, $V_{IN}$ = 12V, $T_J$ = 25°C.
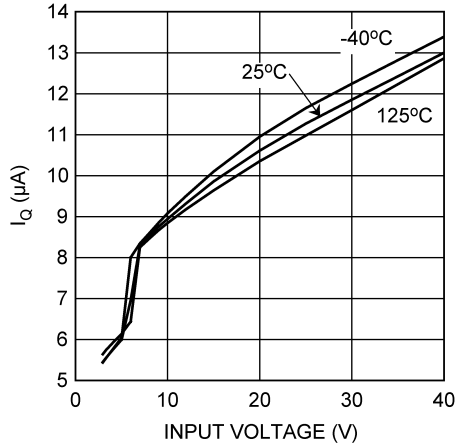


**Figure 1. $I_Q$ vs Temperature & Input Voltage**
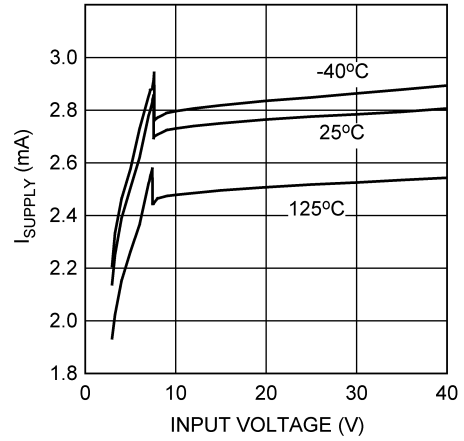


**Figure 2. $I_{Supply}$ vs Input Voltage (Non-Switching)**
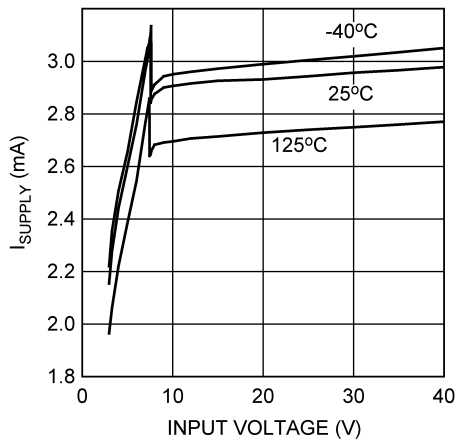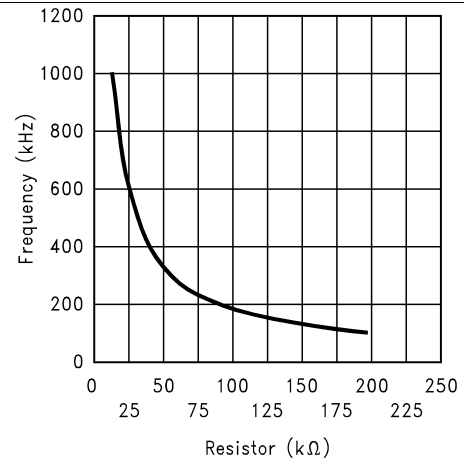


**Figure 3. $I_{Supply}$ vs $V_{IN}$**



**Figure 4. Switching Frequency vs RFA**
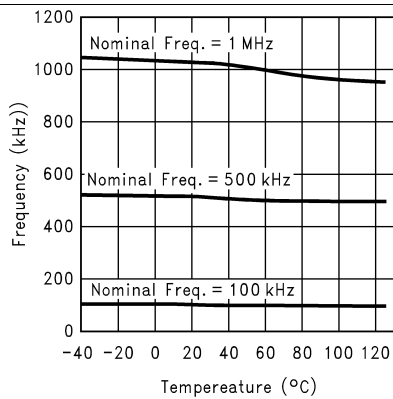


**Figure 5. Frequency vs Temperature**
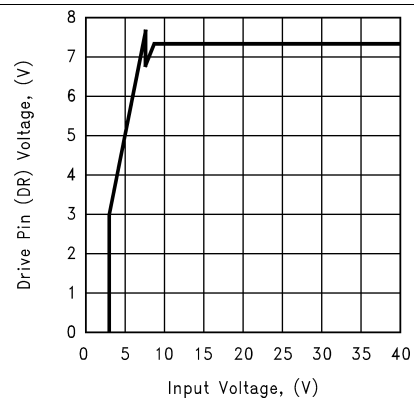


**Figure 6. Drive Voltage vs Input Voltage**

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## Typical Characteristics (continued)

Unless otherwise specified, $V_{IN}$ = 12V, $T_J$ = 25°C.
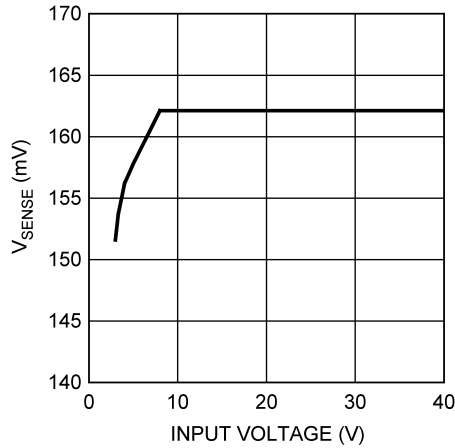

**Figure 7. Current Sense Threshold vs Input Voltage**
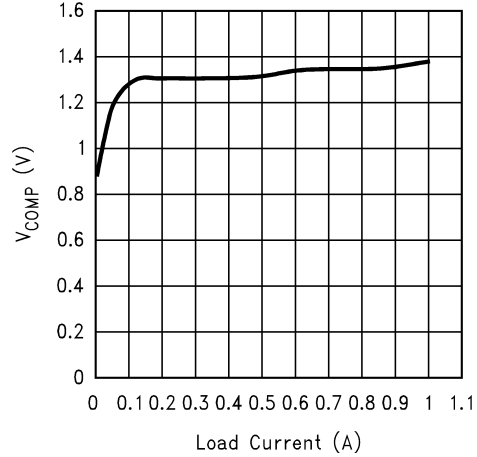

**Figure 8. COMP Pin Voltage vs Load Current**
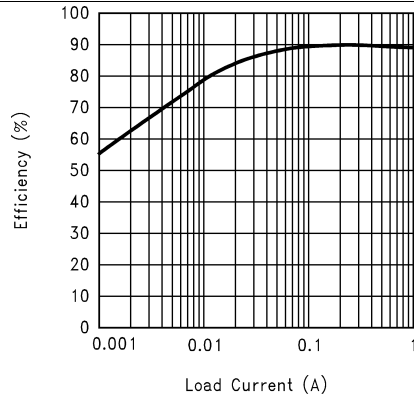

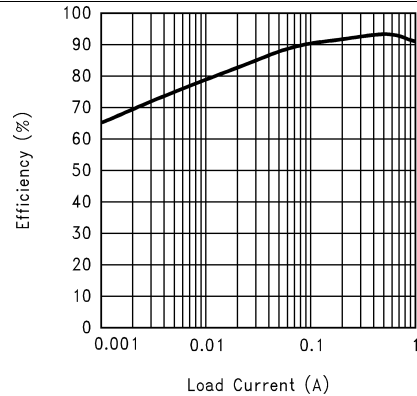**Figure 9. Efficiency vs Load Current (3.3 V In and 12 V Out)**


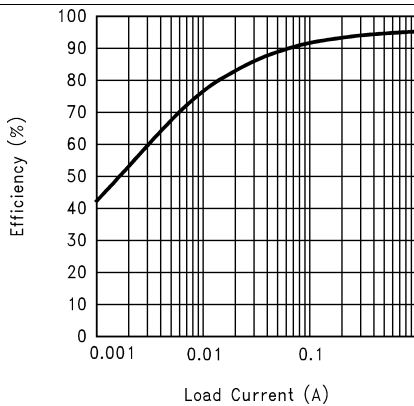**Figure 10. Efficiency vs Load Current (5 V In and 12 V Out)**


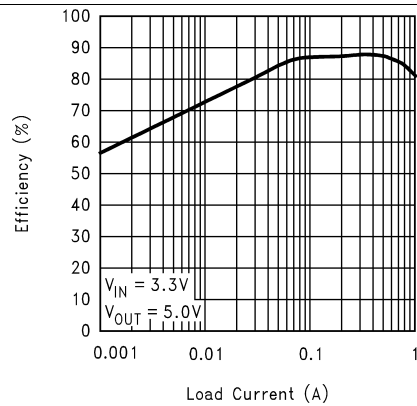**Figure 11. Efficiency vs Load Current (9 V In and 12 V Out)**


**Figure 12. Efficiency vs Load Current (3.3 V In and 5 V Out)**

Product Folder Links: *LM3488  LM3488-Q1*

## Typical Characteristics (continued)

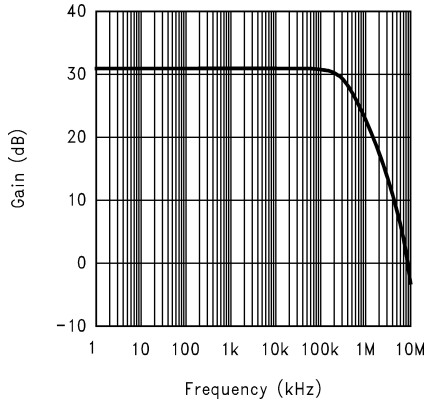Unless otherwise specified, $V_{IN}$ = 12V, $T_J$ = 25°C.


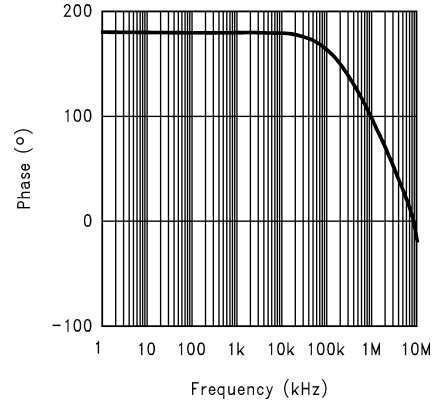**Figure 13. Error Amplifier Gain**


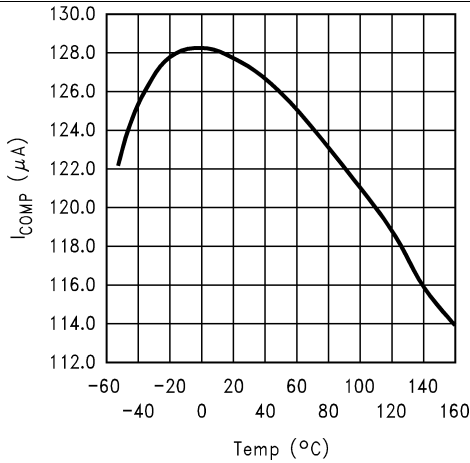**Figure 14. Error Amplifier Phase**


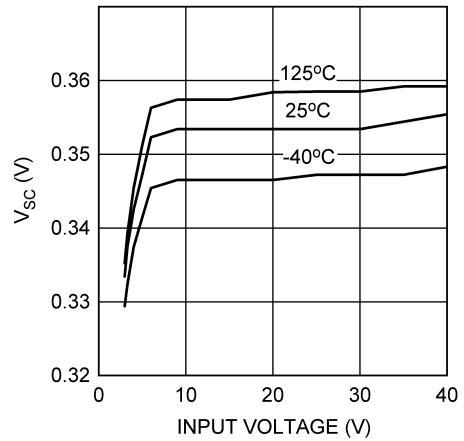**Figure 15. COMP Pin Source Current vs Temperature**


**Figure 16. Short Circuit Protection vs Input Voltage**
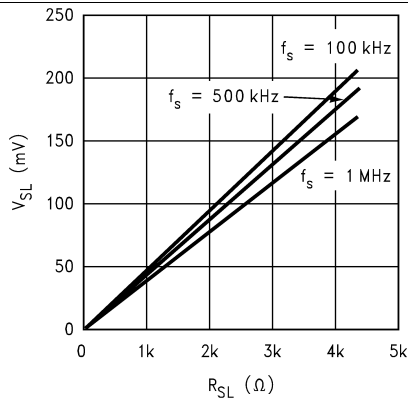

**Figure 17. Compensation Ramp vs Compensation Resistor**


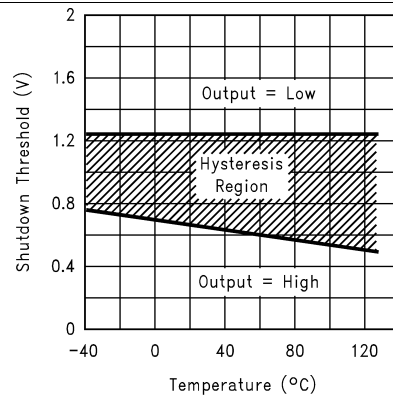**Figure 18. Shutdown Threshold Hysteresis vs Temperature**

## Typical Characteristics (continued)

Unless otherwise specified, $V_{IN}$ = 12V, $T_J$ = 25°C.



**Figure 19. Current Sense Voltage vs Duty Cycle**

Product Folder Links: *LM3488  LM3488-Q1*

# 7 Detailed Description

## 7.1 Overview

The LM3488 uses a fixed frequency, Pulse Width Modulated (PWM), current mode control architecture. In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the $I_{SEN}$ pin. This voltage is then level shifted and fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator.

At the start of any switching cycle, the oscillator sets the RS latch using the SET/Blank-out and switch logic blocks. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off.

The voltage sensed across the sense resistor generally contains spurious noise spikes, as shown in Figure 20. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is about 150ns and is called the blank-out time.

Under extremely light load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET is on during the blank-out time is more than what is delivered to the load. An over-voltage comparator inside the LM3488 prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch under these conditions. The latch remains in reset state till the output decays to the nominal value.
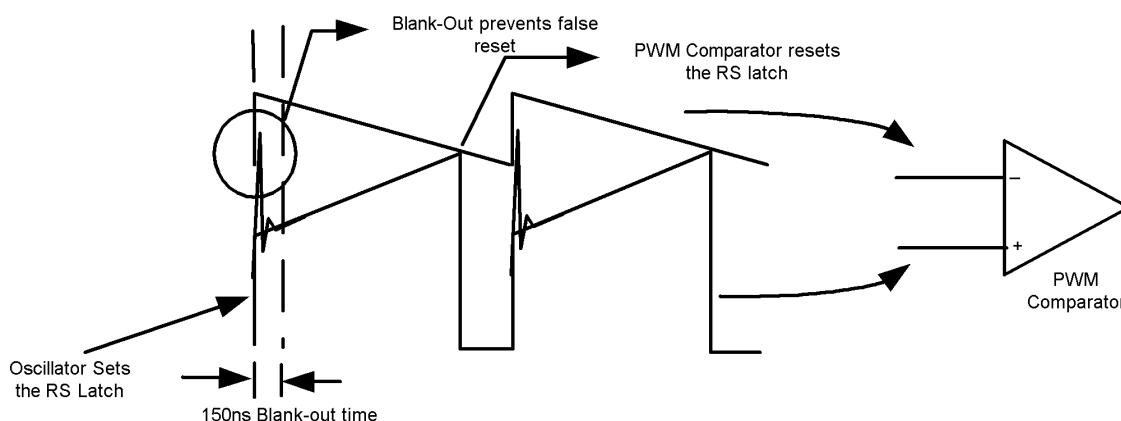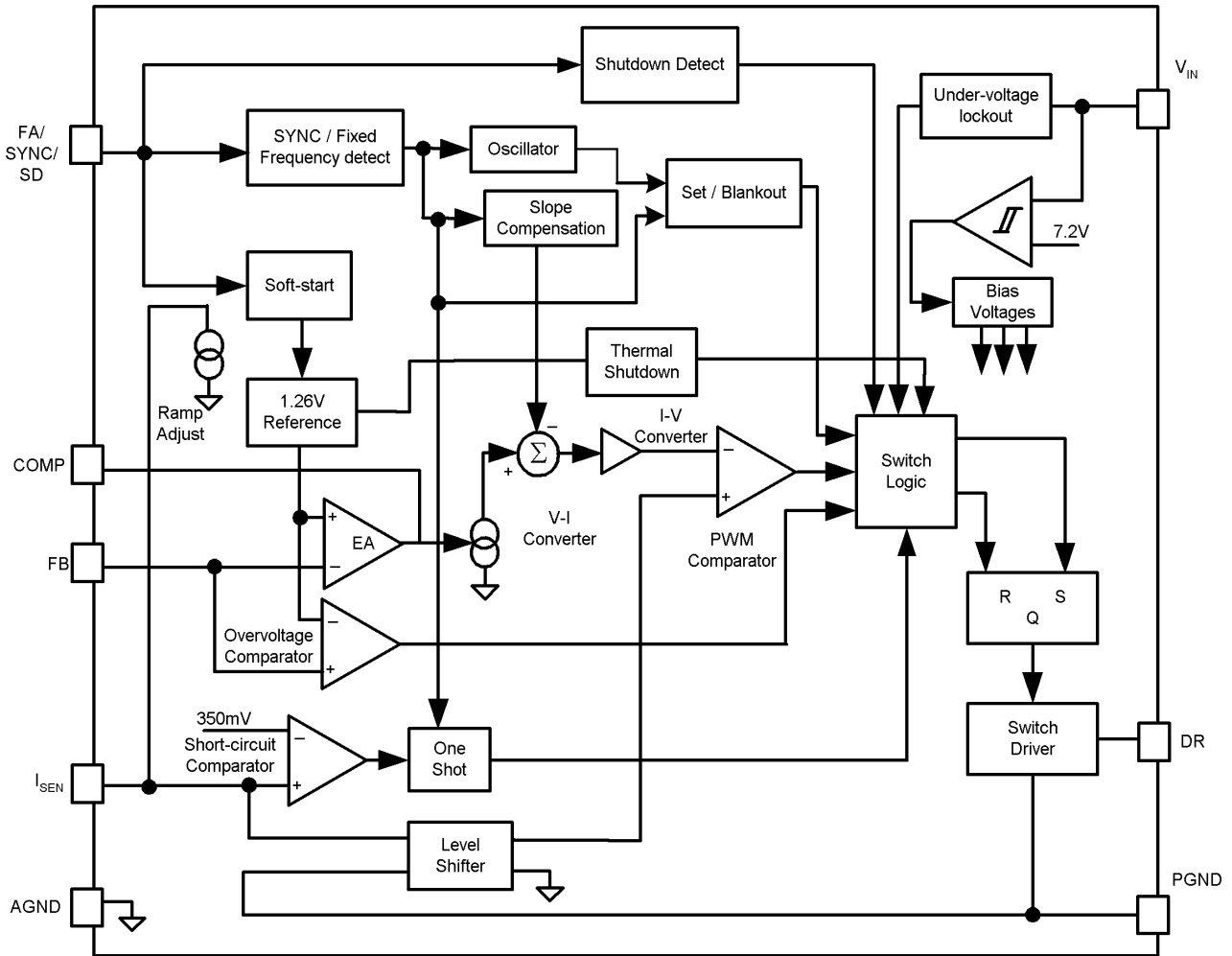


**Figure 20. Basic Operation of the PWM Comparator**

Product Folder Links: *LM3488  LM3488-Q1*

**LM3488, LM3488-Q1**

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## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Slope Compensation Ramp

The LM3488 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch, and simpler control loop characteristics. It is also easy to parallel power stages using current mode control since as current sharing is automatic.

Current mode control has an inherent instability for duty cycles greater than 50%, as shown in Figure 21. In Figure 21, a small increase in the load current causes the switch current to increase by $\Delta I_O$. The effect of this load change, $\Delta I_1$, is :

$$\Delta I_1 = -\left(\frac{M_2}{M_1}\right) \Delta I_O = -\left(\frac{D}{1-D}\right) \Delta I_O$$

(1)

From the above equation, when D > 0.5, $\Delta I_1$ will be greater than $\Delta I_O$. In other words, the disturbance is divergent. So a very small perturbation in the load will cause the disturbance to increase.

To prevent the sub-harmonic oscillations, a compensation ramp is added to the control signal, as shown in Figure 22.

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## Feature Description (continued)

With the compensation ramp,

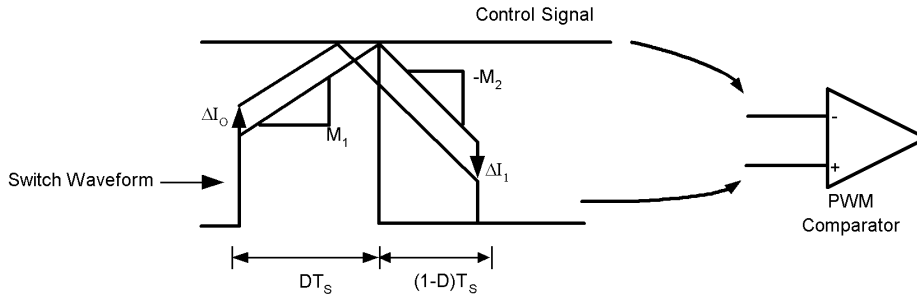$$\Delta I_1 = -\left(\frac{M_2 - M_C}{M_1 + M_C}\right) \Delta I_O$$

(2)



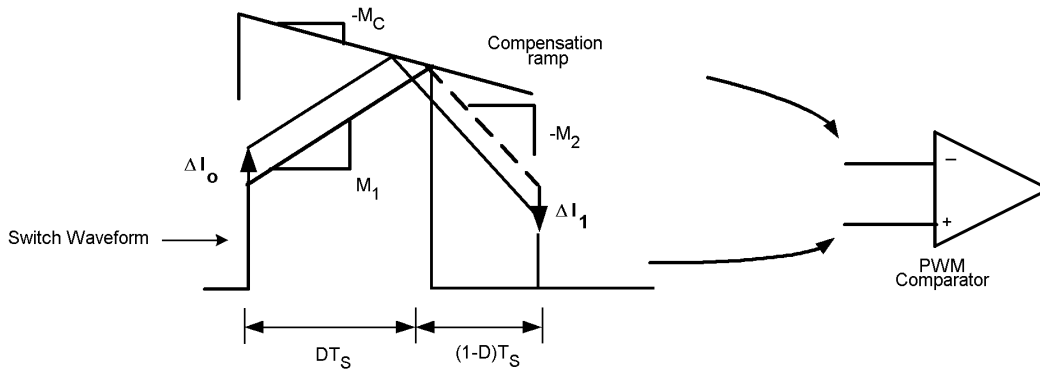**Figure 21. Sub-Harmonic Oscillation for D>0.5**



**Figure 22. Compensation Ramp Avoids Sub-Harmonic Oscillation**

The compensation ramp has been added internally in LM3488. The slope of this compensation ramp has been selected to satisfy most of the applications. The slope of the internal compensation ramp depends on the frequency. This slope can be calculated using the formula:

$$M_C = V_{SL} . F_S \text{ Volts/second}$$

(3)

In the above equation, $V_{SL}$ is the amplitude of the internal compensation ramp. Limits for $V_{SL}$ have been specified in the electrical characteristics.

In order to provide the user additional flexibility, a patented scheme has been implemented inside the IC to increase the slope of the compensation ramp externally, if the need arises. Adding a single external resistor, $R_{SL}$(as shown in Figure 23) increases the slope of the compensation ramp, $M_C$ by :

$$\Delta M_C = \frac{40 \times 10^{-6} . R_{SL} . F_S}{R_{SEN}} \frac{\text{Amps}}{\text{second}}$$

(4)

In this equation, $\Delta V_{SL}$ is equal to $40.10^{-6} R_{SL}$. Hence,

$$\Delta M_C = \frac{\Delta V_{SL} . F_S}{R_{SEN}} \frac{\text{Amps}}{\text{second}}$$

(5)

$\Delta V_{SL}$ versus $R_{SL}$ has been plotted in Figure 24 for different frequencies.

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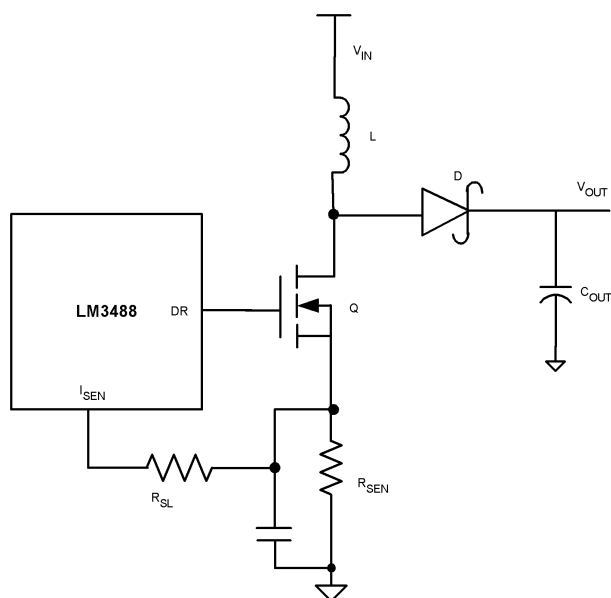## Feature Description (continued)



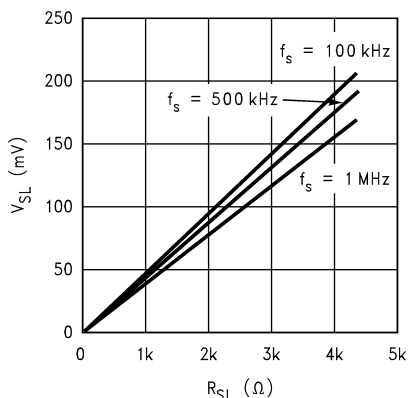**Figure 23. Increasing the Slope of the Compensation Ramp**



**Figure 24. ΔV$_{SL}$ vs R$_{SL}$**

### 7.3.2 Frequency Adjust/Synchronization/Shutdown

The switching frequency of LM3488 can be adjusted between 100kHz and 1MHz using a single external resistor. This resistor must be connected between FA/SYNC/SD pin and ground, as shown in Figure 25. See *Typical Characteristics* to determine the value of the resistor required for a desired switching frequency.

The LM3488 can be synchronized to an external clock. The external clock must be connected to the FA/SYNC/SD pin through a resistor, R$_{SYNC}$ as shown in Figure 26. The value of this resistor is dependent on the off time of the synchronization pulse, T$_{OFF(SYNC)}$. Table 1 shows the range of resistors to be used for a given T$_{OFF(SYNC)}$.

**Table 1. Recommended Series Resistance for Synchronization**

| T$_{OFF(SYNC)}$ (µs) | R$_{SYNC}$ range (kΩ) |
|---|---|
| 1 | 5 to 13 |
| 2 | 20 to 40 |

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**Table 1. Recommended Series Resistance for Synchronization (continued)**

| $T_{OFF(SYNC)}$ (µs) | $R_{SYNC}$ range (kΩ) |
|:---:|:---:|
| 3 | 40 to 65 |
| 4 | 55 to 90 |
| 5 | 70 to 110 |
| 6 | 85 to 140 |
| 7 | 100 to 160 |
| 8 | 120 to 190 |
| 9 | 135 to 215 |
| 10 | 150 to 240 |

It is also necessary to have the width of the synchronization pulse wider than the duty cycle of the converter (when DR pin is high and the switching point is low). It is also necessary to have the synchronization pulse width ≥ 300nsecs.

The FA/SYNC/SD pin also functions as a shutdown pin. If a high signal (see *Electrical Characteristics* for definition of high signal) appears on the FA/SYNC/SD pin, the LM3488 stops switching and goes into a low current mode. The total supply current of the IC reduces to less than 10µA under these conditions.

Figure 27 and Figure 28 show implementation of shutdown function when operating in Frequency adjust mode and synchronization mode respectively. In frequency adjust mode, connecting the FA/SYNC/SD pin to ground forces the clock to run at a certain frequency. Pulling this pin high shuts down the IC. In frequency adjust or synchronization mode, a high signal for more than 30µs shuts down the IC.

Figure 29 shows implementation of both frequency adjust with $R_{FA}$ resistor and frequency synchronization with $R_{SYNC}$. The switching frequency is defined by $R_{FA}$ when a synchronization signal is not applied. When sync is applied it overrides the $R_{FA}$ setting.
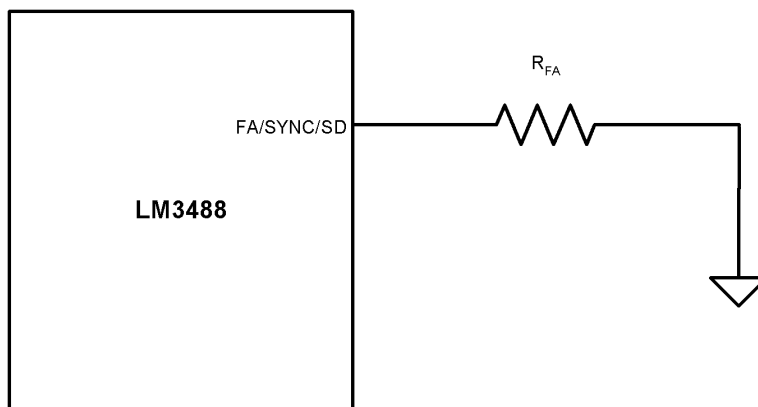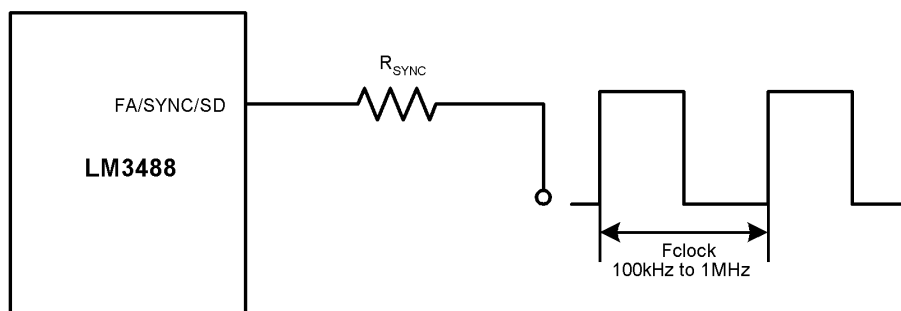


**Figure 25. Frequency Adjust**



**Figure 26. Frequency Synchronization**

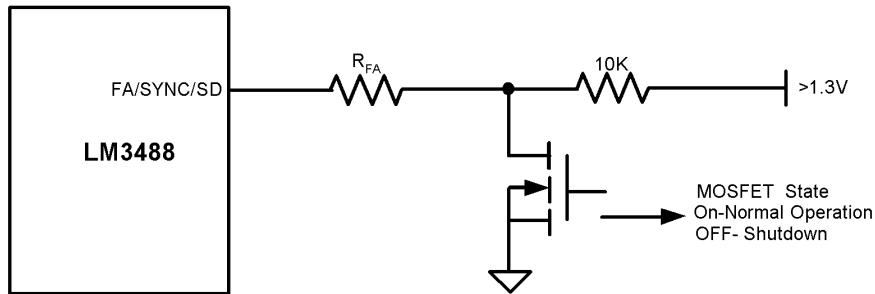Product Folder Links: *LM3488  LM3488-Q1*

**Figure 27. Shutdown Operation in Frequency Adjust Mode**
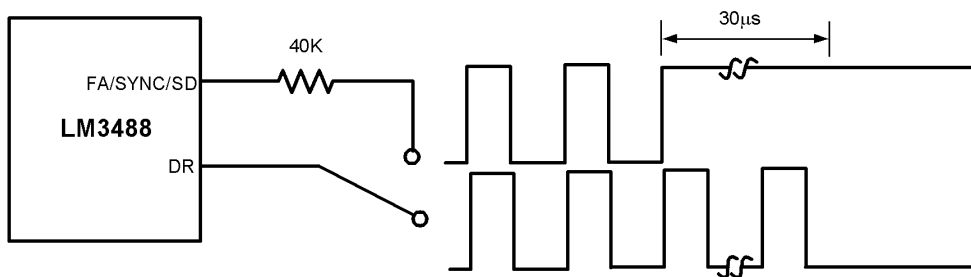


**Figure 28. Shutdown Operation in Synchronization Mode**
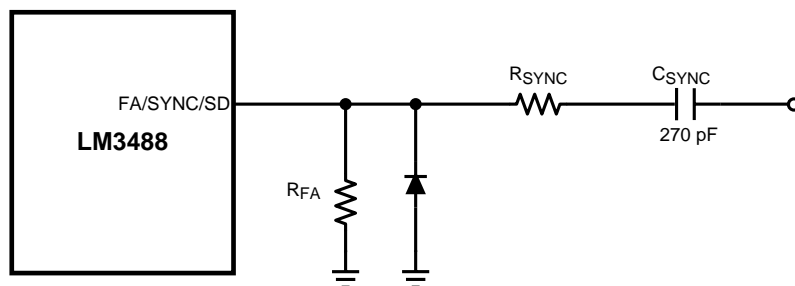


**Figure 29. Frequency Adjust or Frequency Synchronization**

### 7.3.3 Short-Circuit Protection

When the voltage across the sense resistor (measured on $I_{SEN}$ Pin) exceeds 350mV, short-circuit current limit gets activated. A comparator inside LM3488 reduces the switching frequency by a factor of 5 and maintains this condition till the short is removed.

## 7.4 Device Functional Modes

The device is set to run as soon as the input voltage crosses above the UVLO set point and at a frequency set according to the FA/SYNC/SD pin pull-down resistor or to run at a frequency set by the waveform applied to the FA/SYNC/SD pin.

If the FA/SYNC/SD pin is pulled high, the LM3488 enters shut-down mode.

If the voltage at the $I_{SEN}$ pin exceeds $V_{sc}$, the device enters short-circuit protection mode.

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# 8 Application and Implementation

> **NOTE**
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LM3488 may be operated in either continuous or discontinuous conduction mode. The following applications are designed for continuous conduction operation. This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

## 8.2 Typical Applications

### 8.2.1 Boost Converter
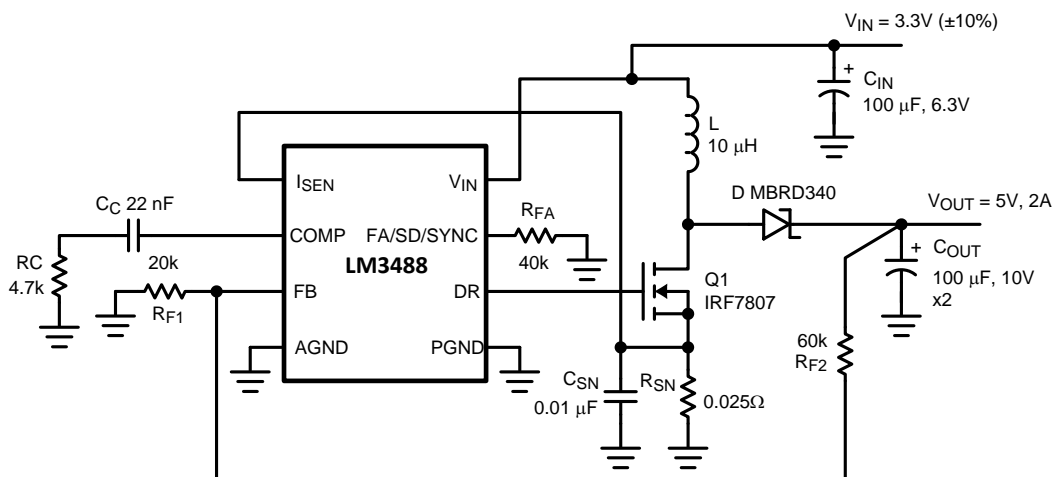


**Figure 30. Typical High Efficiency Step-Up (Boost) Converter**

The most common topology for LM3488 is the boost or step-up topology. The boost converter converts a low input voltage into a higher output voltage. The basic configuration for a boost regulator is shown in Figure 31. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles. In the first cycle of operation, MOSFET Q is turned on and energy is stored in the inductor. During this cycle, diode D is reverse biased and load current is supplied by the output capacitor, $C_{OUT}$.

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## Typical Applications (continued)



**Figure 31. Simplified Boost Converter Diagram**
**(a) First cycle of operation**
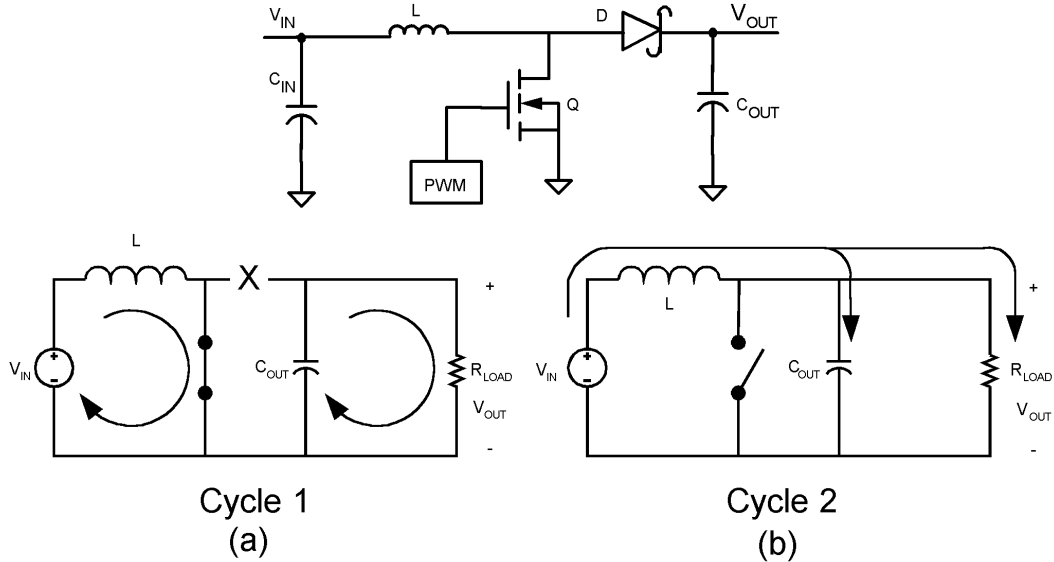**(b) Second cycle of operation**

In the second cycle, MOSFET Q is off and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined as:

$$V_{OUT} = \frac{V_{IN}}{1-D}$$

(6)

(ignoring the drop across the MOSFET and the diode), or

$$V_{OUT} + V_D = \frac{V_{IN} - V_Q}{1-D}$$

where

- D is the duty cycle of the switch
- $V_D$ is the forward voltage drop of the diode
- $V_Q$ is the drop across the MOSFET when it is on

(7)

### 8.2.1.1 Design Requirements

To calculate component values for a Boost converter, the power supply parameters shown in Table 2 should be known. The design shown in Figure 30 is the result of starting with example values shown in Table 2.

**Table 2. Boost Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 3V to 3.6V |
| Output voltage | 5V |
| Maximum current | 2A |
| Operating frequency | 350kHz |

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### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Power Inductor Selection

The inductor is one of the two energy storage elements in a boost converter. Figure 32 shows how the inductor current varies during a switching cycle. The current through an inductor is quantified as:
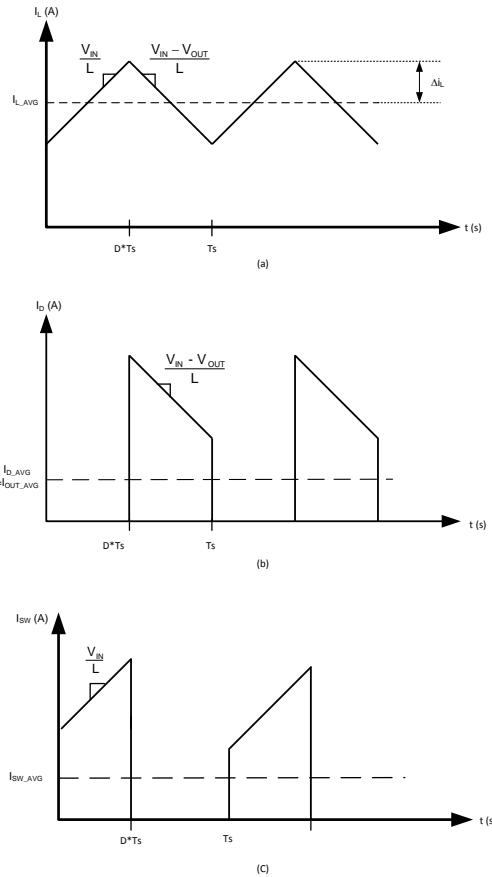
$$V_L(t) = L \frac{di_L(t)}{dt} \tag{8}$$



**Figure 32. A. Inductor Current B. Diode Current C. Switch Current**

If $V_L(t)$ is constant, $di_L(t)/dt$ must be constant. Hence, for a given input voltage and output voltage, the current in the inductor changes at a constant rate.

The important quantities in determining a proper inductance value are $\bar{I}_L$ (the average inductor current) and $\Delta i_L$ (the inductor current ripple). If $\Delta i_L$ is larger than $\bar{I}_L$, the inductor current will drop to zero for a portion of the cycle and the converter will operate in discontinuous conduction mode. If $\Delta i_L$ is smaller than $\bar{I}_L$, the inductor current will stay above zero and the converter will operate in continuous conduction mode. All the analysis in this datasheet assumes operation in continuous conduction mode. To operate in continuous conduction mode, the following conditions must be met:

$$I_L > \Delta i_L \tag{9}$$

$$\frac{I_{OUT}}{1-D} > \frac{DV_{IN}}{2f_S L} \tag{10}$$

$$L > \frac{D(1-D)V_{IN}}{2I_{OUT}f_S} \tag{11}$$

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Choose the minimum $I_{OUT}$ to determine the minimum L. A common choice is to set $\Delta i_L$ to 30% of $\bar{I}_L$. Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. In a boost converter,

$$\bar{I}_L = \frac{I_{OUT}}{1-D}$$

(12)

and $I_{L\_peak} = \bar{I}_L(max) + \Delta i_L(max)$,

where

$$\Delta i_L = \frac{DV_{IN}}{2f_S L}$$

(13)

A core size with ratings higher than these values should be chosen. If the core is not properly rated, saturation will dramatically reduce overall efficiency.

The LM3488 can be set to switch at very high frequencies. When the switching frequency is high, the converter can be operated with very small inductor values. With a small inductor value, the peak inductor current can be extremely higher than the output currents, especially under light load conditions.

The LM3488 senses the peak current through the switch. The peak current through the switch is the same as the peak current calculated above.

#### 8.2.1.2.2 Programming the Output Voltage

The output voltage can be programmed using a resistor divider between the output and the feedback pins, as shown in Figure 33. The resistors are selected such that the voltage at the feedback pin is 1.26V. $R_{F1}$ and $R_{F2}$ can be selected using the equation,

$$V_{OUT} = 1.26\left(1 + \frac{R_{F1}}{R_{F2}}\right)$$

(14)

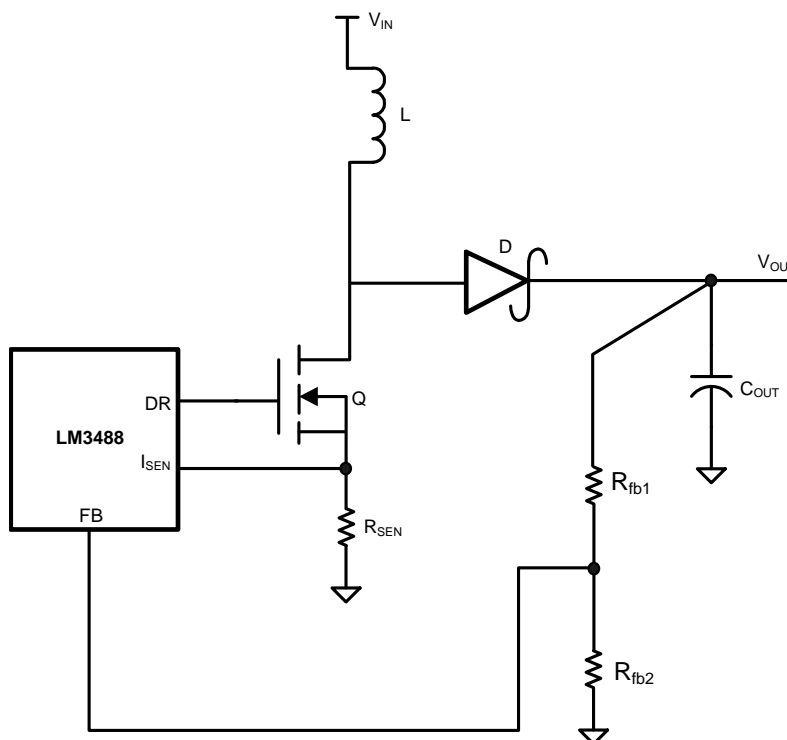A 100-pF capacitor may be connected between the feedback and ground pins to reduce noise.



**Figure 33. Adjusting the Output Voltage**

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### 8.2.1.2.3  Setting the Current Limit

The maximum amount of current that can be delivered to the load is set by the sense resistor, $R_{SEN}$. Current limit occurs when the voltage that is generated across the sense resistor equals the current sense threshold voltage, $V_{SENSE}$. When this threshold is reached, the switch will be turned off until the next cycle. Limits for $V_{SENSE}$ are specified in *Electrical Characteristics*. $V_{SENSE}$ represents the maximum value of the internal control signal $V_{CS}$. This control signal, however, is not a constant value and changes over the course of a period as a result of the internal compensation ramp (see Figure 20). Therefore the current limit threshold will also change. The actual current limit threshold is a function of the sense voltage ($V_{SENSE}$) and the internal compensation ramp:

$$R_{SEN} \times ISW_{LIMIT} = VCS_{MAX} = V_{SENSE} - (D \times V_{SL})$$

where

- $ISW_{LIMIT}$ is the peak switch current limit, defined by the equation below. As duty cycle increases, the control voltage is reduced as $V_{SL}$ ramps up. Since current limit threshold varies with duty cycle, the following equation should be used to select $R_{SEN}$ and set the desired current limit threshold: (15)

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SL})}{ISW_{LIMIT}}$$

(16)

The numerator of the above equation is $V_{CS}$, and $ISW_{LIMIT}$ is calculated as:

$$ISW_{LIMIT} = \left[ \frac{I_{OUT}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)} \right]$$

(17)

To avoid false triggering, the current limit value should have some margin above the maximum operating value, typically 120%. Values for both $V_{SENSE}$ and $V_{SL}$ are specified in *Electrical Characteristics*. However, calculating with the limits of these two specs could result in an unrealistically wide current limit or $R_{SEN}$ range. Therefore, the following equation is recommended, using the $V_{SL}$ ratio value given in *Electrical Characteristics*:

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SENSE} \times V_{SL}\text{ratio})}{ISW_{LIMIT}}$$

(18)

$R_{SEN}$ is part of the current mode control loop and has some influence on control loop stability. Therefore, once the current limit threshold is set, loop stability must be verified. To verify stability, use the following equation:

$$R_{SEN} < \frac{2 \times V_{SL} \times f_S \times L}{V_O - (2 \times V_{IN})}$$

(19)

If the selected $R_{SEN}$ is greater than this value, additional slope compensation must be added to ensure stability, as described in *Current Limit with External Slope Compensation*.

### 8.2.1.2.4  Current Limit with External Slope Compensation

$R_{SL}$ is used to add additional slope compensation when required. It is not necessary in most designs and $R_{SL}$ should be no larger than necessary. Select $R_{SL}$ according to the following equation:

$$R_{SL} > \frac{\dfrac{R_{SEN} \times (V_O - 2V_{IN})}{2 \times f_S \times L} - V_{SL}}{40 \ \mu A}$$

where

- $R_{SEN}$ is the selected value based on current limit. With $R_{SL}$ installed, the control signal includes additional external slope to stabilize the loop, which will also have an effect on the current limit threshold. Therefore, the current limit threshold must be re-verified, as illustrated in the equations below : (20)

$$V_{CS} = V_{SENSE} - (D \times (V_{SL} + \Delta V_{SL}))$$

where

- $\Delta V_{SL}$ is the additional slope compensation generated and calculated as: (21)

$$\Delta V_{SL} = 40 \ \mu A \times R_{SL}$$

(22)

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This changes the equation for current limit (or $R_{SEN}$) to:

$$ISW_{LIMIT} = \frac{V_{SENSE} - (D \times (V_{SL} + \Delta V_{SL}))}{R_{SEN}}$$

(23)

The $R_{SEN}$ and $R_{SL}$ values may have to be calculated iteratively in order to achieve both the desired current limit and stable operation. In some designs $R_{SL}$ can also help to filter noise on the ISEN pin.

If the inductor is selected such that ripple current is the recommended 30% value, and the current limit threshold is 120% of the maximum peak, a simpler method can be used to determine $R_{SEN}$. The equation below will provide optimum stability without RSL, provided that the above 2 conditions are met:

$$R_{SEN} = \frac{V_{SENSE}}{ISW_{LIMIT} + \left(\dfrac{Vo - Vi}{L \times f_S}\right) \times D}$$

(24)

#### 8.2.1.2.5 Power Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using the formula:

$$I_{D(Peak)} = I_{OUT} / (1-D) + \Delta I_L$$

(25)

In the above equation, $I_{OUT}$ is the output current and $\Delta I_L$ has been defined in Figure 32.

The peak reverse voltage for boost converter is equal to the regulator output voltage. The diode must be capable of handling this voltage. To improve efficiency, a low forward drop schottky diode is recommended.

#### 8.2.1.2.6 Power MOSFET Selection

The drive pin of LM3488 must be connected to the gate of an external MOSFET. In a boost topology, the drain of the external N-Channel MOSFET is connected to the inductor and the source is connected to the ground. The drive pin (DR) voltage depends on the input voltage (see the *Typical Characteristics* section). In most applications, a logic level MOSFET can be used. For very low input voltages, a sub-logic level MOSFET should be used.

The selected MOSFET directly controls the efficiency. The critical parameters for selection of a MOSFET are:

1. Minimum threshold voltage, $V_{TH}(MIN)$
2. On-resistance, $R_{DS}(ON)$
3. Total gate charge, $Q_g$
4. Reverse transfer capacitance, $C_{RSS}$
5. Maximum drain to source voltage, $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the output voltage. $V_{DS(MAX)}$ of the MOSFET must be greater than the output voltage. The power losses in the MOSFET can be categorized into conduction losses and ac switching or transition losses. $R_{DS(ON)}$ is needed to estimate the conduction losses. The conduction loss, $P_{COND}$, is the $I^2R$ loss across the MOSFET. The maximum conduction loss is given by:

$$P_{COND(MAX)} = \left[\left(\frac{I_{OUT}}{1-D_{MAX}}\right)^2 + \left(\frac{\Delta I}{3}\right)^2\right] D_{MAX} R_{DS(ON)}$$

where

- $D_{MAX}$ is the maximum duty cycle.

(26)

$$D_{MAX} = \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)$$

(27)

The turn-on and turn-off transitions of a MOSFET require times of tens of nano-seconds. $C_{RSS}$ and $Q_g$ are needed to estimate the large instantaneous power loss that occurs during these transitions.

The amount of gate current required to turn the MOSFET on can be calculated using the formula:

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$$I_G = Q_g.F_S \tag{28}$$

The required gate drive power to turn the MOSFET on is equal to the switching frequency times the energy required to deliver the charge to bring the gate charge voltage to $V_{DR}$ (see the *Electrical Characteristics* table and the *Typical Characteristics* section for the drive voltage specification).

$$P_{Drive} = F_S.Q_g.V_{DR} \tag{29}$$

### 8.2.1.2.7 Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular, as shown in Figure 32. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The rms current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta i_L /\sqrt{3} = \frac{1}{2\sqrt{3}}\left(\frac{V_{OUT} - V_{IN}}{V_{OUT}Lf_S}\right) \tag{30}$$

The input capacitor should be capable of handling the rms current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 10 µF to 20 µF. If a value lower than 10µF is used, then problems with impedance interactions or switching noise can affect the LM3488. To improve performance, especially with $V_{IN}$ below 8 volts, it is recommended to use a 20Ω resistor at the input to provide a RC filter. The resistor is placed in series with the $V_{IN}$ pin with only a bypass capacitor attached to the $V_{IN}$ pin directly (see Figure 34). A 0.1-µF or 1-µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.
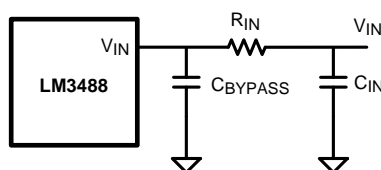


**Figure 34. Reducing IC Input Noise**

### 8.2.1.2.8 Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the inductor is charging. As a result it sees very large ripple currents. The output capacitor should be capable of handling the maximum rms current. The rms current in the output capacitor is:

$$I_{COUT(RMS)} = \sqrt{(1-D)\left[I_{OUT}^2\frac{D}{(1-D)^2} + \frac{\Delta i_L^2}{3}\right]} \tag{31}$$

Where

$$\Delta i_L = \frac{DV_{IN}}{2Lf_S} \tag{32}$$

and D, the duty cycle is equal to $(V_{OUT} - V_{IN})/V_{OUT}$.

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface Mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo- OSCON, or multi-layer ceramic capacitors are recommended at the output.

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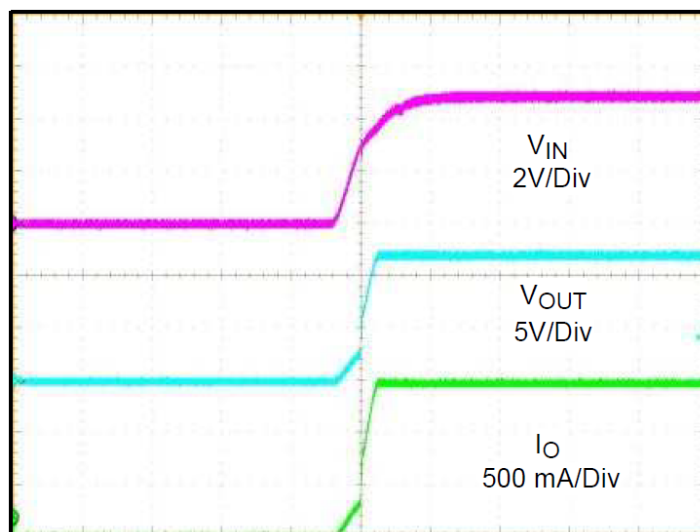SNVS089N – JULY 2000 – REVISED DECEMBER 2014

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### 8.2.1.3 Application Curve



**Figure 35. Typical Startup Waveform (horizontal scale: 10ms/DIV)**

### 8.2.2 Designing SEPIC Using LM3488

Since the LM3488 controls a low-side N-Channel MOSFET, it can also be used in SEPIC (Single Ended Primary Inductance Converter) applications. An example of SEPIC using LM3488 is shown in Figure 36. As shown in Figure 36, the output voltage can be higher or lower than the input voltage. The SEPIC uses two inductors to step-up or step-down the input voltage. The inductors L1 and L2 can be two discrete inductors or two windings of a coupled transformer since equal voltages are applied across the inductor throughout the switching cycle. Using two discrete inductors allows use of catalog magnetics, as opposed to a custom transformer. The input ripple can be reduced along with size by using the coupled windings of transformer for L1 and L2.
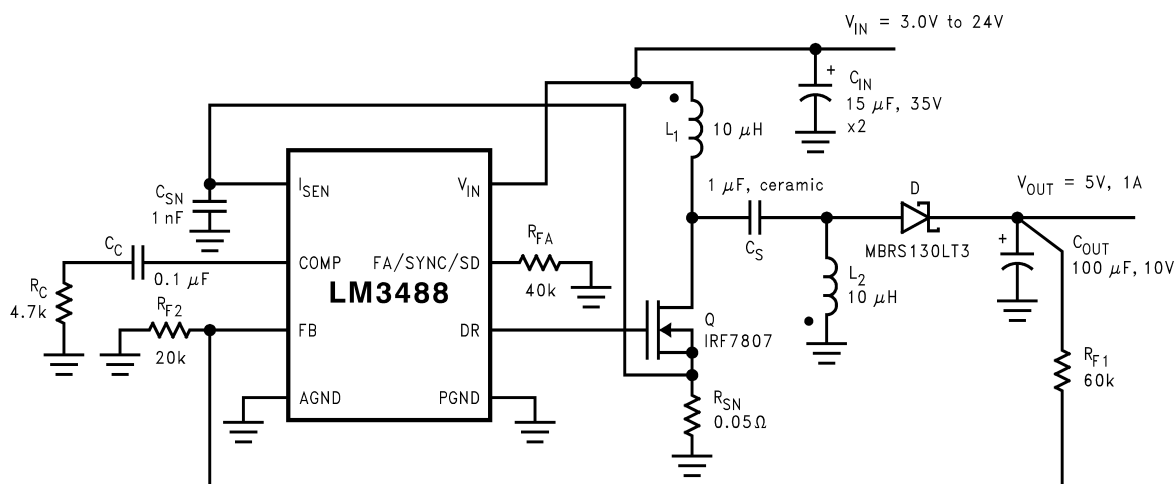


**Figure 36. Typical SEPIC Converter**

Due to the presence of the inductor L1 at the input, the SEPIC inherits all the benefits of a boost converter. One main advantage of SEPIC over boost converter is the inherent input to output isolation. The capacitor CS isolates the input from the output and provides protection against shorted or malfunctioning load. Hence, the A SEPIC is useful for replacing boost circuits when true shutdown is required. This means that the output voltage falls to 0V when the switch is turned off. In a boost converter, the output can only fall to the input voltage minus a diode drop.

The duty cycle of a SEPIC is given by:

$$D = \frac{V_{OUT} + V_{DIODE}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}}$$

(33)

In the above equation, $V_Q$ is the on-state voltage of the MOSFET, Q, and $V_{DIODE}$ is the forward voltage drop of the diode.

### 8.2.2.1 Design Requirements

To calculate component values for a SEPIC converter, the power supply parameters shown in Table 3 should be known. The design shown in Figure 36 is the result of starting with example values shown in Table 3

**Table 3. SEPIC Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 3 V to 24 V |
| Output voltage | 5 V |
| Maximum current | 1 A |
| Operating frequency | 350 kHz |
| Max peak to peak output ripple | 200 mV |

### 8.2.2.2 Detailed Design Procedure

#### 8.2.2.2.1 Power MOSFET Selection

As in boost converter, the parameters governing the selection of the MOSFET are the minimum threshold voltage, $V_{TH(MIN)}$, the on-resistance, $R_{DS(ON)}$, the total gate charge, $Q_g$, the reverse transfer capacitance, $C_{RSS}$, and the maximum drain to source voltage, $V_{DS(MAX)}$. The peak switch voltage in a SEPIC is given by:

$$V_{SW(PEAK)} = V_{IN} + V_{OUT} + V_{DIODE}$$

(34)

The selected MOSFET should satisfy the condition:

$$V_{DS(MAX)} > V_{SW(PEAK)}$$

(35)

The peak switch current is given by:

$$I_{SW(PEAK)} = I_{L1(AVG)} + I_{OUT} + \frac{\Delta I_{L1} + \Delta I_{L2}}{2}$$

(36)

The rms current through the switch is given by:

$$I_{SWRMS} = \sqrt{\left[I_{SWPEAK}^2 - I_{SWPEAK}(\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1} + \Delta I_{L2})^2}{3}\right]D}$$

(37)

#### 8.2.2.2.2 Power Diode Selection

The Power diode must be selected to handle the peak current and the peak reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current. The off-state voltage or peak reverse voltage of the diode is $V_{IN} + V_{OUT}$. Similar to the boost converter, the average diode current is equal to the output current. Schottky diodes are recommended.

#### 8.2.2.2.3 Selection Of Inductors L1 and L2

Proper selection of the inductors L1 and L2 to maintain constant current mode requires calculations of the following parameters.

Average current in the inductors:

$$I_{L1AVE} = \frac{DI_{OUT}}{1-D}$$

(38)

$$I_{L2AVE} = I_{OUT}$$

(39)

Product Folder Links: *LM3488  LM3488-Q1*

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Datasheet of LM3488MM/NOPB - IC REG CTRL BST FLYBK PWM 8VSSOP
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Peak to peak ripple current, to calculate core loss if necessary:

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q)\,D}{(L1)f_S}$$

(40)

$$\Delta I_{L2} = \frac{(V_{IN} - V_Q)\,D}{(L2)f_S}$$

(41)

maintains the condition $I_L > \Delta i_L/2$ to ensure constant current mode.

$$L1 > \frac{(V_{IN} - V_Q)(1-D)}{2I_{OUT}f_S}$$

(42)

$$L2 > \frac{(V_{IN} - V_Q)D}{2I_{OUT}f_S}$$

(43)

Peak current in the inductor, to ensure the inductor does not saturate:

$$I_{L1PK} = \frac{DI_{OUT}}{1-D} + \frac{\Delta I_{L1}}{2}$$

(44)

$$I_{L2PK} = I_{OUT} + \frac{\Delta I_{L2}}{2}$$

(45)

$I_{L1PK}$ must be lower than the maximum current rating set by the current sense resistor.

The value of L1 can be increased above the minimum recommended to reduce input ripple and output ripple. However, once $D_{IL1}$ is less than 20% of $I_{L1AVE}$, the benefit to output ripple is minimal.

By increasing the value of L2 above the minimum recommended, $\Delta_{IL2}$ can be reduced, which in turn will reduce the output ripple voltage:

$$\Delta V_{OUT} = \left(\frac{I_{OUT}}{1-D} + \frac{\Delta I_{L2}}{2}\right) ESR$$

where

  • ESR is the effective series resistance of the output capacitor.

(46)

If L1 and L2 are wound on the same core, then L1 = L2 = L. All the equations above will hold true if the inductance is replaced by 2L. A good choice for transformer with equal turns is Coiltronics CTX series Octopack.

### 8.2.2.2.4 Sense Resistor Selection

The peak current through the switch, $I_{SW(PEAK)}$ can be adjusted using the current sense resistor, $R_{SEN}$, to provide a certain output current. Resistor $R_{SEN}$ can be selected using the formula:

$$R_{SEN} = \frac{V_{SENSE} - D(V_{SL} + \Delta V_{SL})}{I_{SWPEAK}}$$

(47)

### 8.2.2.2.5 SEPIC Capacitor Selection

The selection of SEPIC capacitor, CS, depends on the rms current. The rms current of the SEPIC capacitor is given by:

$$I_{CSRMS} = \sqrt{I_{SWRMS}^2 + \left(I_{L1PK}^2 - I_{L1PK}\Delta I_{L1} + \Delta I_{L1}^2\right)\left(1-D\right)}$$

(48)

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The SEPIC capacitor must be rated for a large ACrms current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the rms current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum capacitors are the best choice for SMT, having high rms current ratings relative to size. Ceramic capacitors could be used, but the low C values will tend to cause larger changes in voltage across the capacitor due to the large currents. High C value ceramics are expensive. Electrolytics work well for through hole applications where the size required to meet the rms current rating can be accommodated. There is an energy balance between CS and L1, which can be used to determine the value of the capacitor. The basic energy balance equation is:

$$\frac{1}{2} C_S \Delta V_S^2 = \frac{1}{2} L_1 \Delta I_{L1}^2 \tag{49}$$

Where

$$\Delta V_S = \left( \frac{V_{OUT}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}} \right) \frac{I_{OUT}}{f_S C_S} \tag{50}$$

is the ripple voltage across the SEPIC capacitor, and

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q) D}{L_1 f_S} \tag{51}$$

is the ripple current through the inductor L1. The energy balance equation can be solved to provide a minimum value for C$_S$:

$$C_S \geq L_1 \frac{I_{OUT}^2}{(V_{IN} - V_Q)^2} \tag{52}$$

#### 8.2.2.2.6  Input Capacitor Selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The rms current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta I_{L1} / \sqrt{12} = \frac{D}{2\sqrt{3}} \left( \frac{V_{IN} - V_Q}{L_1 f_S} \right) \tag{53}$$

The input capacitor should be capable of handling the rms current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 10µF to 20µF. If a value lower than 10µF is used, then problems with impedance interactions or switching noise can affect the LM3488. To improve performance, especially with V$_{IN}$ below 8 volts, it is recommended to use a 20Ω resistor at the input to provide a RC filter. The resistor is placed in series with the V$_{IN}$ pin with only a bypass capacitor attached to the V$_{IN}$ pin directly (see Figure 34). A 0.1µF or 1µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.

#### 8.2.2.2.7  Output Capacitor Selection

The ESR and ESL of the output capacitor directly control the output ripple. Use low capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo- OSCON, or multi-layer ceramic capacitors are recommended at the output.

The output capacitor of the SEPIC sees very large ripple currents (similar to the output capacitor of a boost converter. The rms current through the output capacitor is given by:

$$I_{RMS} = \sqrt{\frac{\left[ I_{SWPK}^2 - I_{SWPK}(\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1} + \Delta I_{L2})^2}{3} \right] (1-D) - I_{OUT}^2}{}} \tag{54}$$

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The ESR and ESL of the output capacitor directly control the output ripple. Use low capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo- OSCON, or multi-layer ceramic capacitors are recommended at the output for low ripple.

## 9   Power Supply Recommendations

The LM3488 is designed to operate from various DC power supply including a car battery. If so, VIN input should be protected from reversal voltage and voltage dump over 48 Volts. The impedance of the input supply rail should be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

## 10   Layout

### 10.1   Layout Guidelines

Good board layout is critical for switching controllers such as the LM3488. First the ground plane area must be sufficient for thermal dissipation purposes and second, appropriate guidelines must be followed to reduce the effects of switching noise. Switch mode converters are very fast switching devices. In such devices, the rapid increase of input current combined with the parasitic trace inductance generates unwanted Ldi/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise. The current sensing circuit in current mode devices can be easily effected by switching noise. This noise can cause duty cycle jitter which leads to increased spectral noise. The most important layout rule is to keep the AC current loops as small as possible. Figure 37 shows the current flow of a boost converter. The top schematic shows a dotted line which represents the current flow during onstate and the middle schematic shows the current flow during off-state. The bottom schematic shows the currents we refer to as AC currents. They are the most critical ones since current is changing in very short time periods. The dotted lined traces of the bottom schematic are the once to make as short as possible.
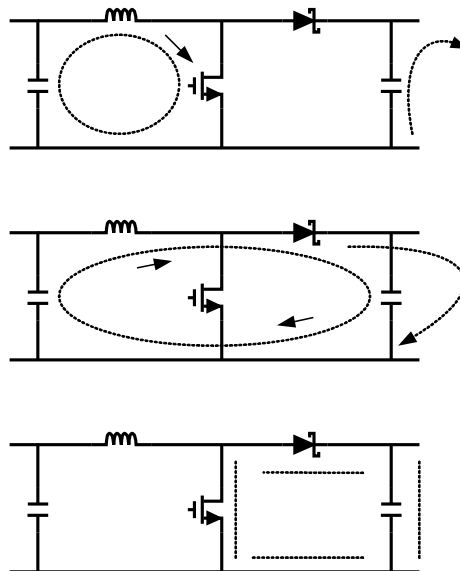


**Figure 37.   Current Flow in a Boost Application**

Product Folder Links: *LM3488  LM3488-Q1*

**TEXAS INSTRUMENTS**

**LM3488, LM3488-Q1**

## Layout Guidelines (continued)

The PGND and AGND pins have to be connected to the same ground very close to the IC. To avoid ground loop currents attach all the grounds of the system only at one point. A ceramic input capacitor should be connected as close as possible to the Vin pin and grounded close to the GND pin. For a layout example please see AN-1204 LM378/LM3488 Evaluation Board (SNVA656A). For more information about layout in switch mode power supplies please refer to AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines (SNVA054c).

### 10.2  Layout Example
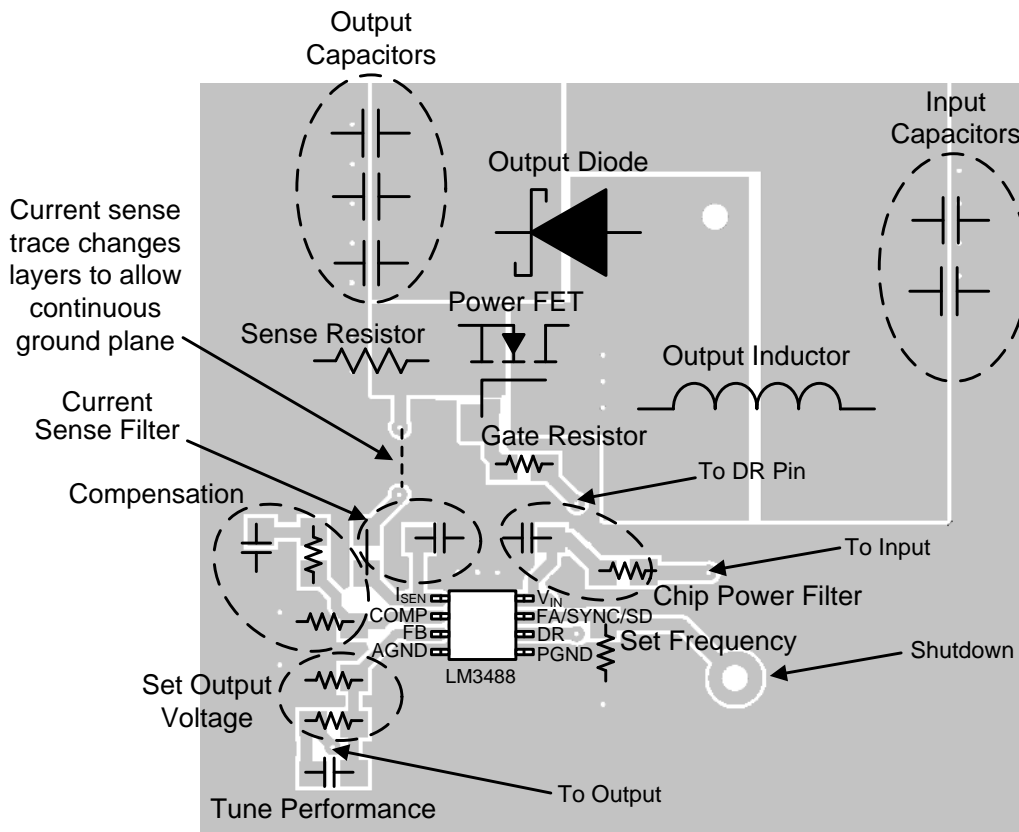


**Figure 38.  Example Layout of a Boost Application using LM3488**

## 11  Device and Documentation Support

### 11.1  Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| LM3488 | Click here | Click here | Click here | Click here | Click here |
| LM3488-Q1 | Click here | Click here | Click here | Click here | Click here |

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## 11.2 Trademarks

All trademarks are the property of their respective owners.

## 11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGE OPTION ADDENDUM**

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3488MM | ACTIVE | VSSOP | DGK | 8 | 1000 | TBD | Call TI | Call TI | | S21B | Samples |
| LM3488MM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAUAG \| CU SN | Level-1-260C-UNLIM | -40 to 125 | S21B | Samples |
| LM3488MMX | NRND | VSSOP | DGK | 8 | | TBD | Call TI | Call TI | -40 to 125 | S21B | |
| LM3488MMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG \| CU SN | Level-1-260C-UNLIM | -40 to 125 | S21B | Samples |
| LM3488QMM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | SSKB | Samples |
| LM3488QMMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | SSKB | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
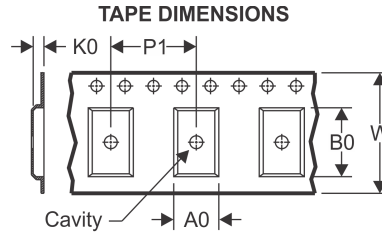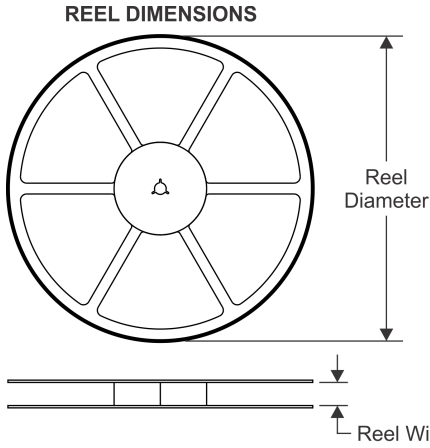
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[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TEXAS INSTRUMENTS**

# PACKAGE MATERIALS INFORMATION

www.ti.com                                                                                                  2-Sep-2015

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

User Direction of Feed

Pocket Quadrants
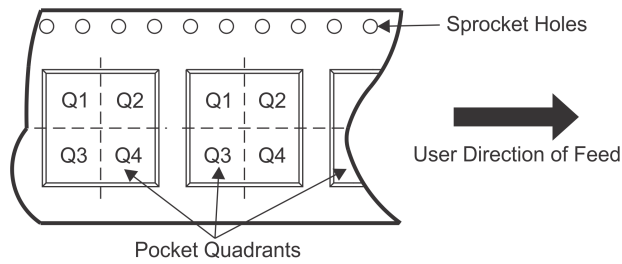
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3488MM | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM3488MM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM3488MMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM3488QMM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM3488QMMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

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# PACKAGE MATERIALS INFORMATION

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2-Sep-2015

**TAPE AND REEL BOX  DIMENSIONS**
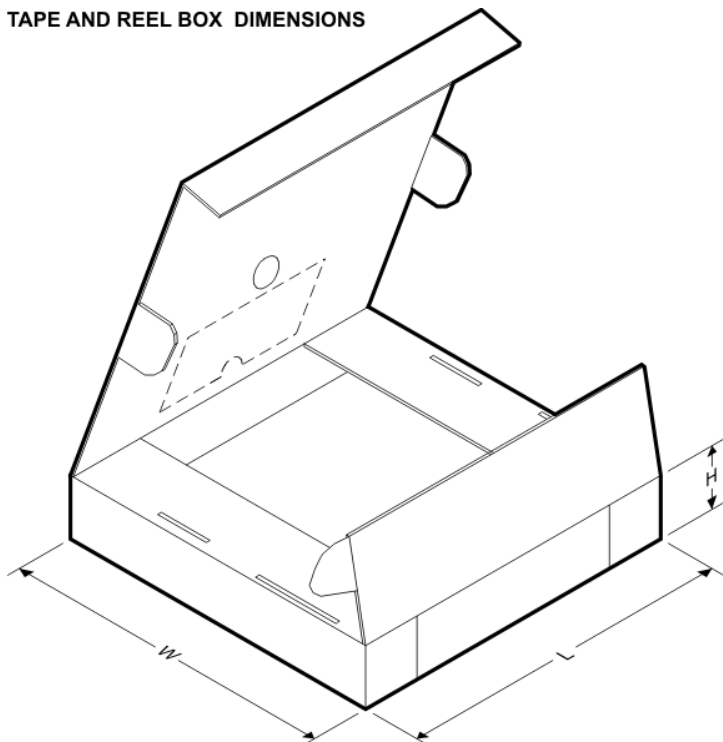


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| LM3488MM | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3488MM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3488MMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LM3488QMM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3488QMMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |

**MECHANICAL DATA**

DGK (S−PDSO−G8)                    PLASTIC SMALL−OUTLINE PACKAGE
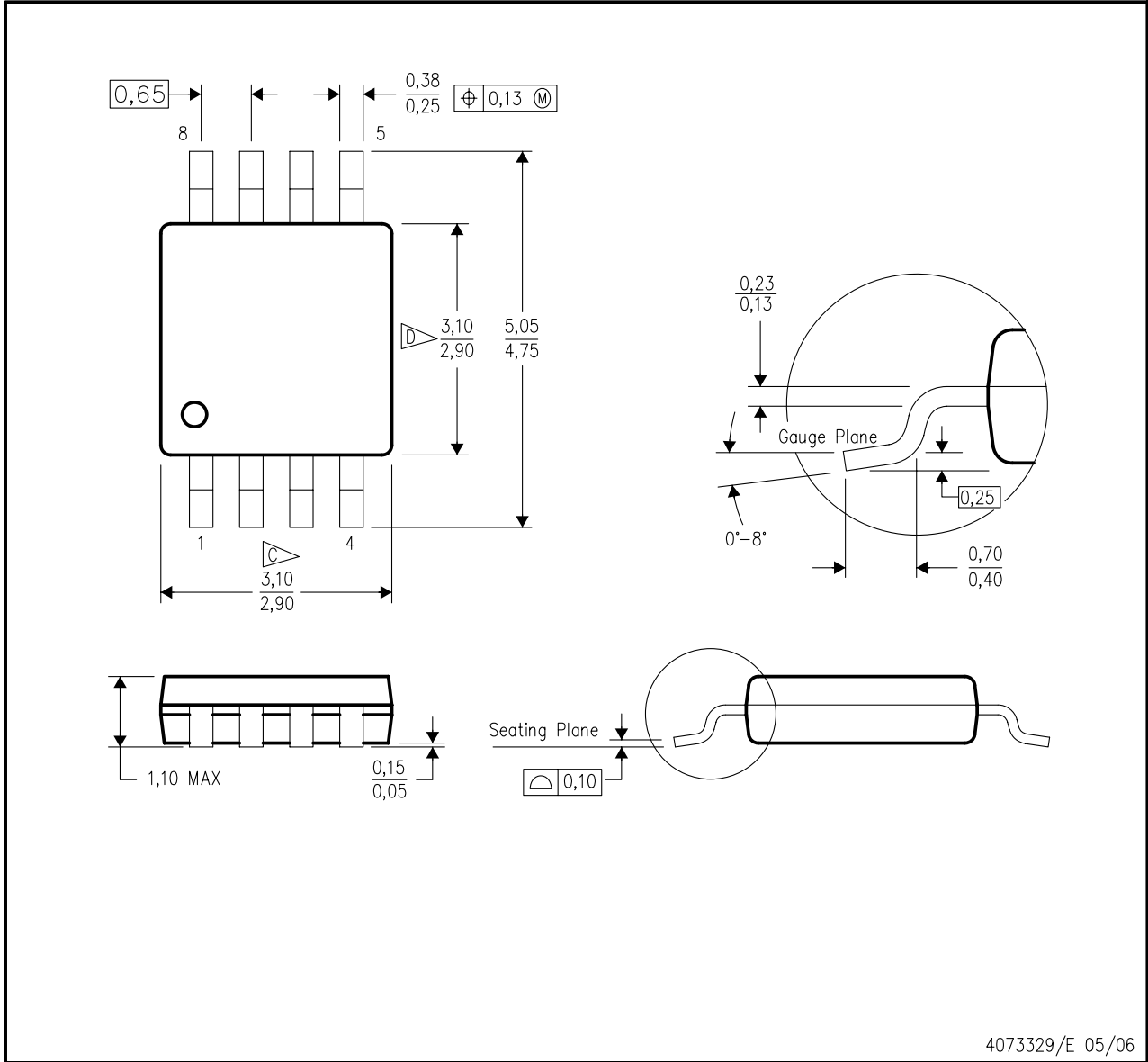


4073329/E 05/06

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
        D.  Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
        E.  Falls within JEDEC MO−187 variation AA, except interlead flash.

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## LAND PATTERN DATA

DGK (S−PDSO−G8)　　　　　PLASTIC SMALL OUTLINE PACKAGE
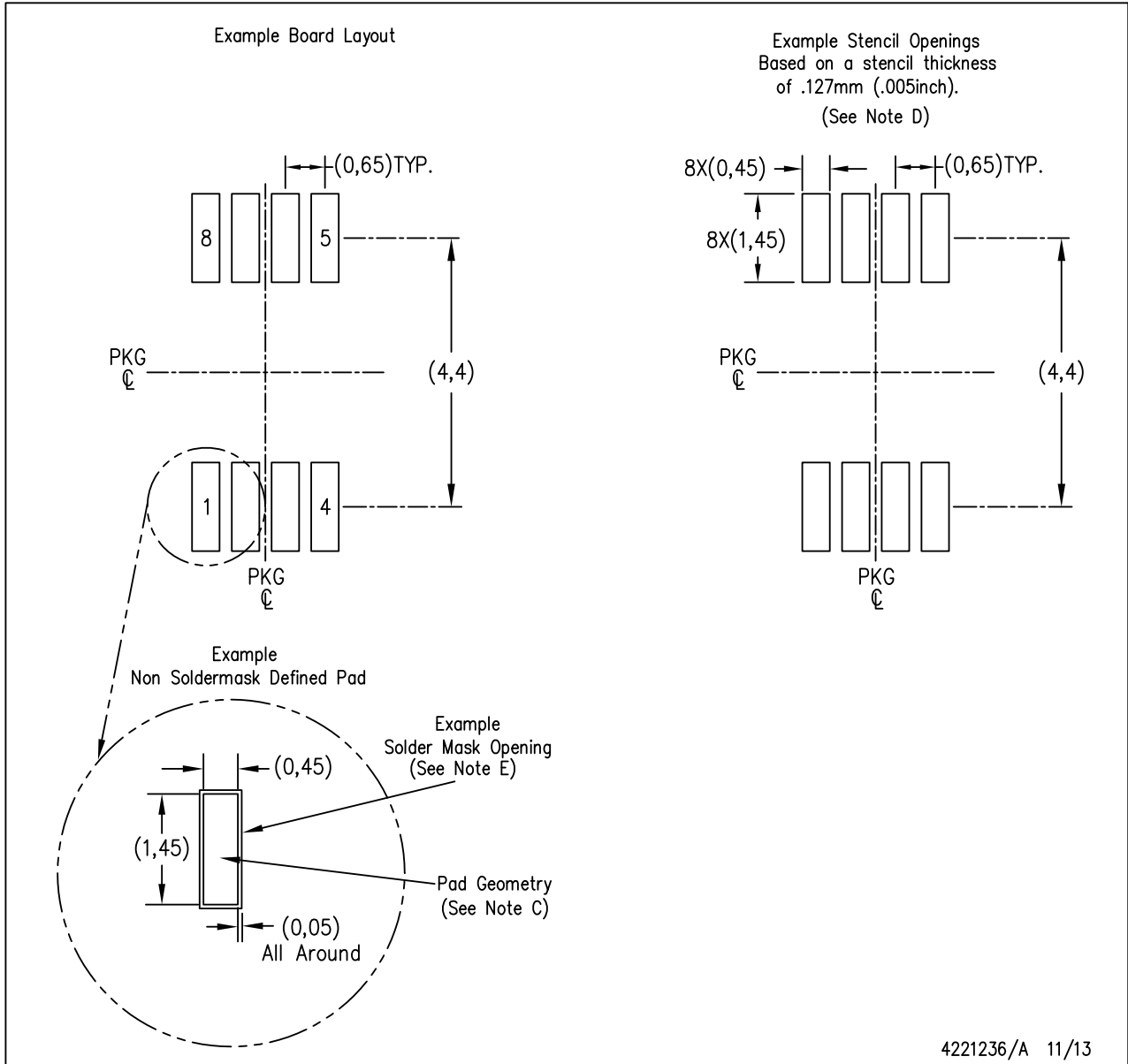


Example Board Layout

(0,65)TYP.

8

5

PKG ℄

(4,4)

1

4

PKG ℄

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

(0,45)

(1,45)

Pad Geometry
(See Note C)

(0,05)
All Around

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

8X(0,45)　　　(0,65)TYP.

8X(1,45)

PKG ℄

(4,4)

PKG ℄

4221236/A  11/13

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Publication IPC−7351 is recommended for alternate designs.
　　　　　D.　Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
　　　　　　　contact their board assembly site for stencil design recommendations.　Refer to IPC−7525 for other stencil recommendations.
　　　　　E.　Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
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| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |