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BUK962R1-40E

N-channel TrenchMOS logic level FET

13 July 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{Gst}(th)$ rating of greater than 0.5V at 175 °C

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 175^\circ\text{C}$		-	-	40	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25^\circ\text{C}$; Fig. 1	[1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25^\circ\text{C}$; Fig. 2		-	-	293	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25^\circ\text{C}$; Fig. 11		-	1.7	2.1	$\text{m}\Omega$
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; Fig. 13 ; Fig. 14		-	29.6	-	nC

[1] Continuous current is limited by package.



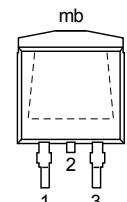
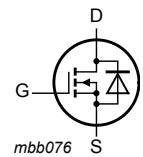
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2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain	 D2PAK (SOT404)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK962R1-40E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
BUK962R1-40E	BUK962R1-40E

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 175^\circ\text{C}$		-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	40	V
V_{GS}	gate-source voltage	$T_j = 25^\circ\text{C}$		-10	10	V
		$T_j = 25^\circ\text{C}$; lifetime =100 hours		-15	15	V
I_D	drain current	$T_{mb} = 25^\circ\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 1	[1]	-	120	A
		$T_{mb} = 100^\circ\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 1	[1]	-	120	A
I_{DM}	peak drain current	$T_{mb} = 25^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4		-	1078	A
P_{tot}	total power dissipation	$T_{mb} = 25^\circ\text{C}$; Fig. 2		-	293	W
T_{stg}	storage temperature			-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 µs; T _{mb} = 25 °C		-	1078	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 120 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 3	[2][3]	-	622	mJ

[1] Continuous current is limited by package.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[3] Refer to application note AN10273 for further information.

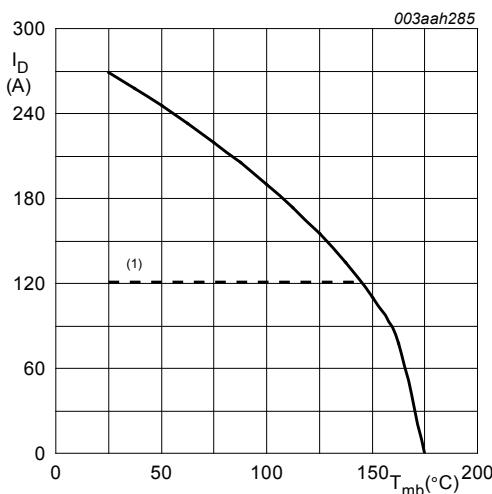


Fig. 1. Continuous drain current as a function of mounting base temperature

V_{GS} ≥ 5V

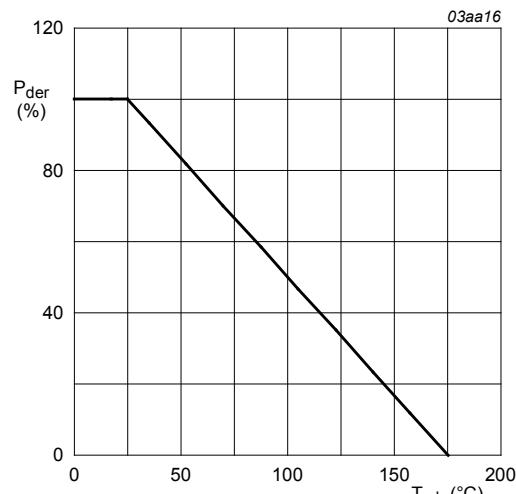


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \%$$

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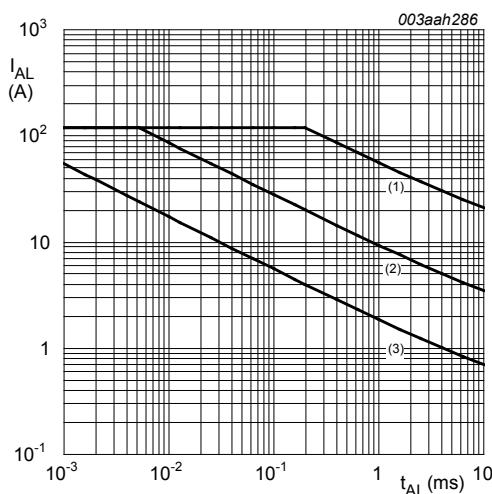


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_j (int) = 25^\circ C$; (2) $T_j (int) = 150^\circ C$; (3) Repetitive Avalanche

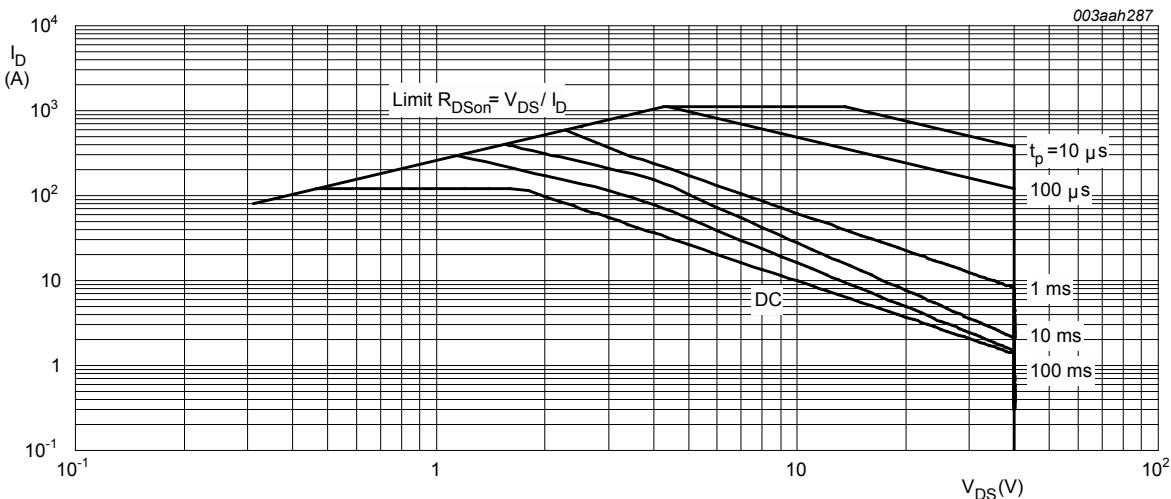


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board		-	50	-	K/W

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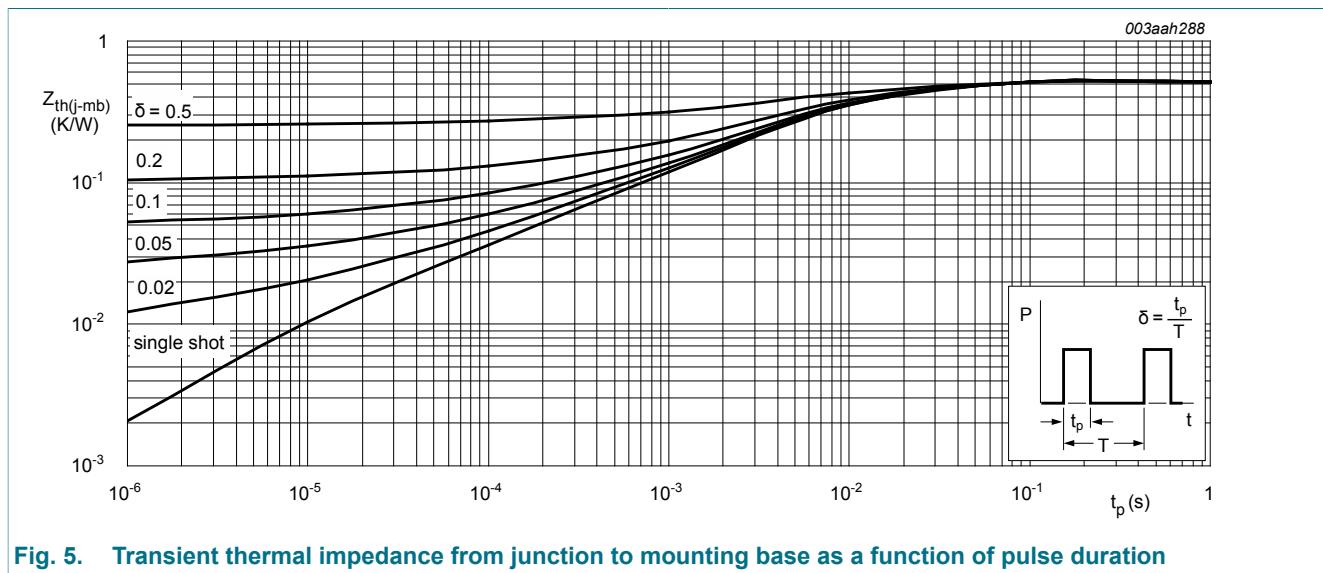


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

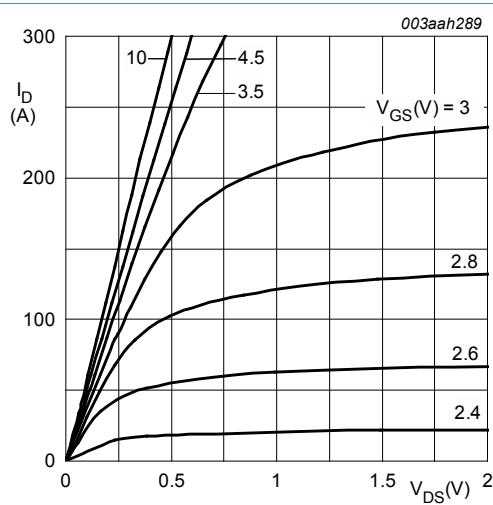
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 µA; V _{GS} = 0 V; T _j = 25 °C	40	-	-	V
		I _D = 250 µA; V _{GS} = 0 V; T _j = -55 °C	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9 ; Fig. 10	1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 9	-	-	2.45	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 9	0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.15	1	µA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	µA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	1.7	2.1	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	1.5	1.8	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; Fig. 12 ; Fig. 11	-	-	4	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 5 V; Fig. 13 ; Fig. 14	-	87.8	-	nC

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}$; $V_{DS} = 32 \text{ V}$; $V_{GS} = 5 \text{ V}$; Fig. 14 ; Fig. 13		-	20.8	-	nC
Q_{GD}	gate-drain charge	$I_D = 25 \text{ A}$; $V_{DS} = 32 \text{ V}$; $V_{GS} = 5 \text{ V}$; Fig. 13 ; Fig. 14		-	29.6	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}$; $V_{DS} = 25 \text{ V}$; $f = 1 \text{ MHz}$;		-	9880	13160	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ\text{C}$; Fig. 15		-	1187	1425	pF
C_{rss}	reverse transfer capacitance			-	600	820	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}$; $R_L = 1.2 \Omega$; $V_{GS} = 5 \text{ V}$;		-	56	-	ns
t_r	rise time	$R_{G(ext)} = 5 \Omega$		-	96	-	ns
$t_{d(off)}$	turn-off delay time			-	151	-	ns
t_f	fall time			-	93	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad		-	7.5	-	nH
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 16		-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$;		-	45	-	ns
Q_r	recovered charge	$V_{DS} = 25 \text{ V}$		-	62	-	nC



$T_j = 25 \text{ }^\circ\text{C}$; $t_p = 300 \mu\text{s}$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

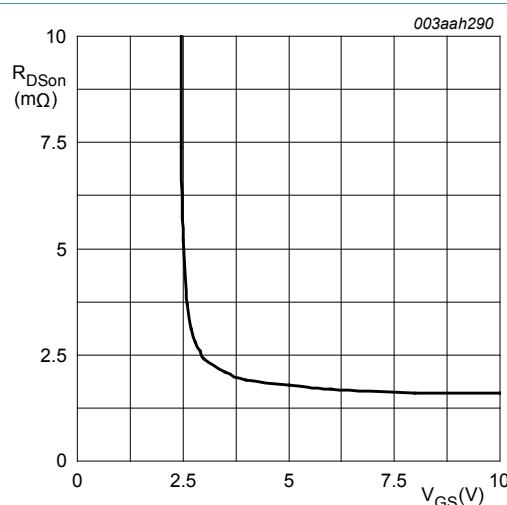


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25 \text{ }^\circ\text{C}$; $I_D = 25 \text{ A}$

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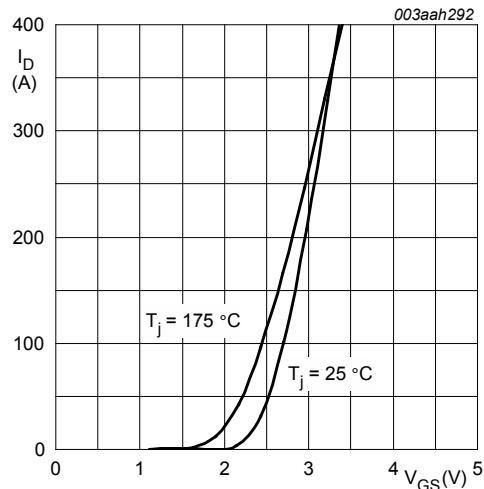


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10V$$

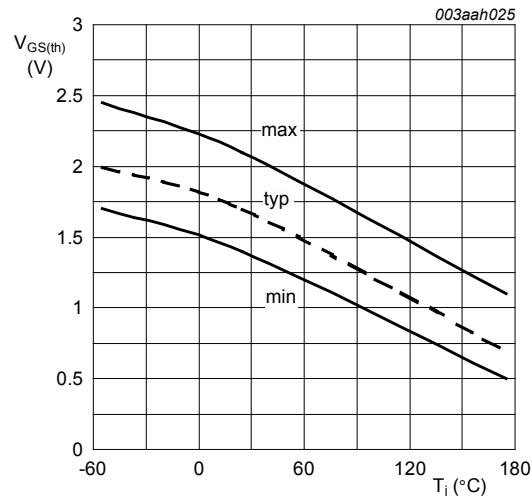


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

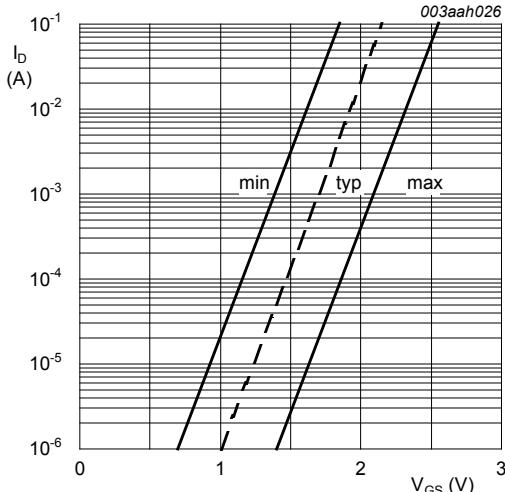
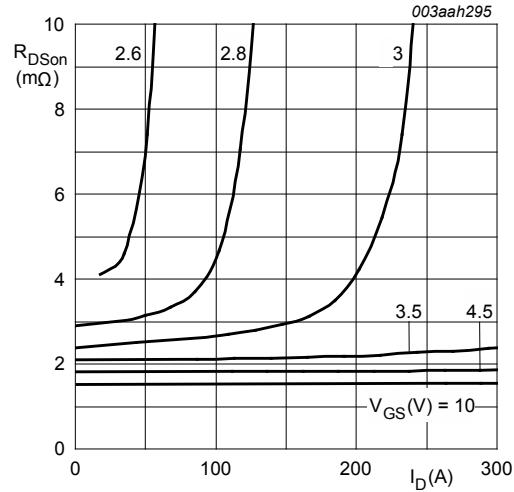


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ C; V_{DS} = 5V$$



$$T_j = 25^\circ C; t_p = 300 \mu s$$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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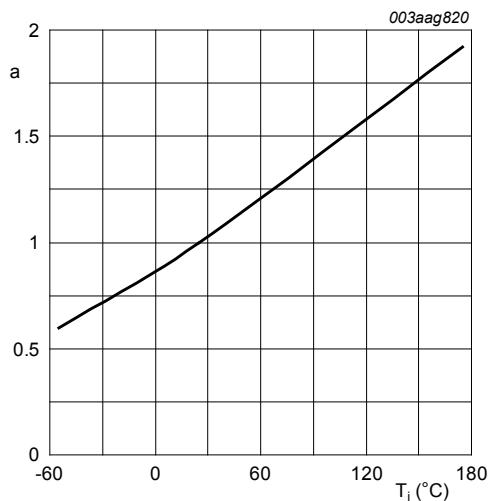


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ }^{\circ}\text{C})}$$

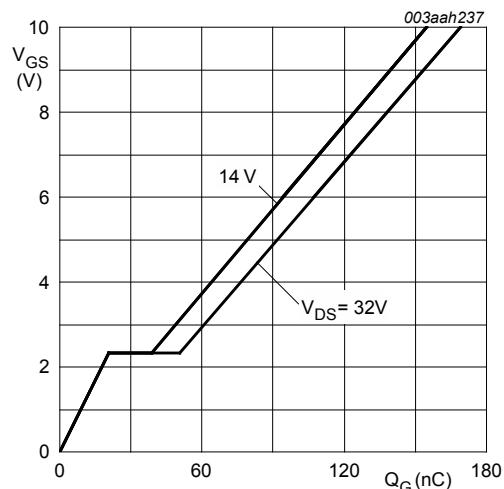


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{A}$$

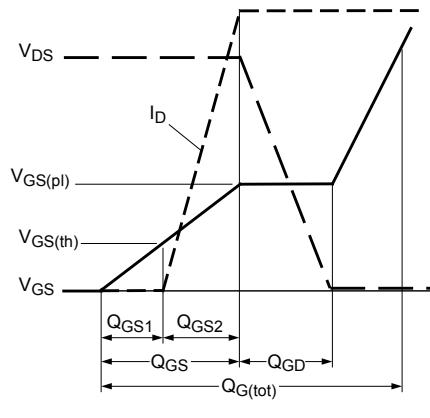


Fig. 13. Gate charge waveform definitions

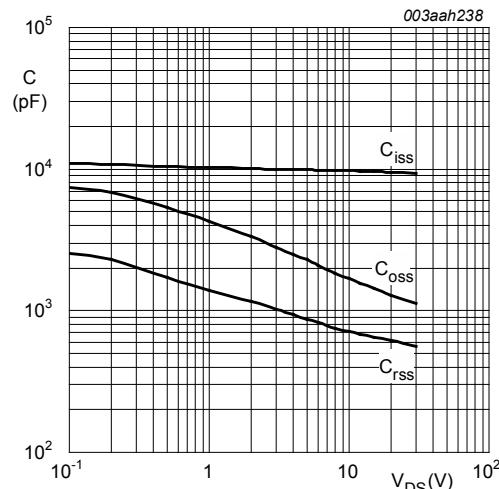
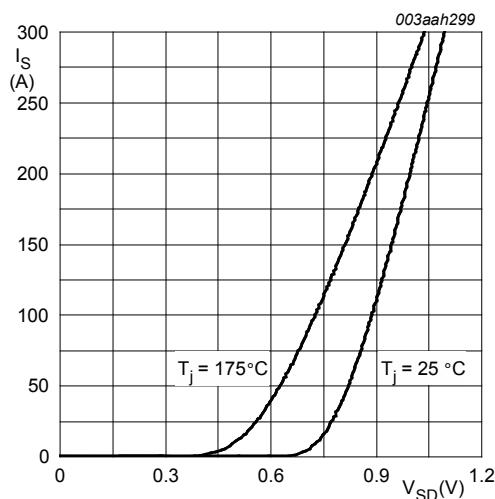


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

NXP Semiconductors**BUK962R1-40E****N-channel TrenchMOS logic level FET****Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values** $V_{GS} = 0V$

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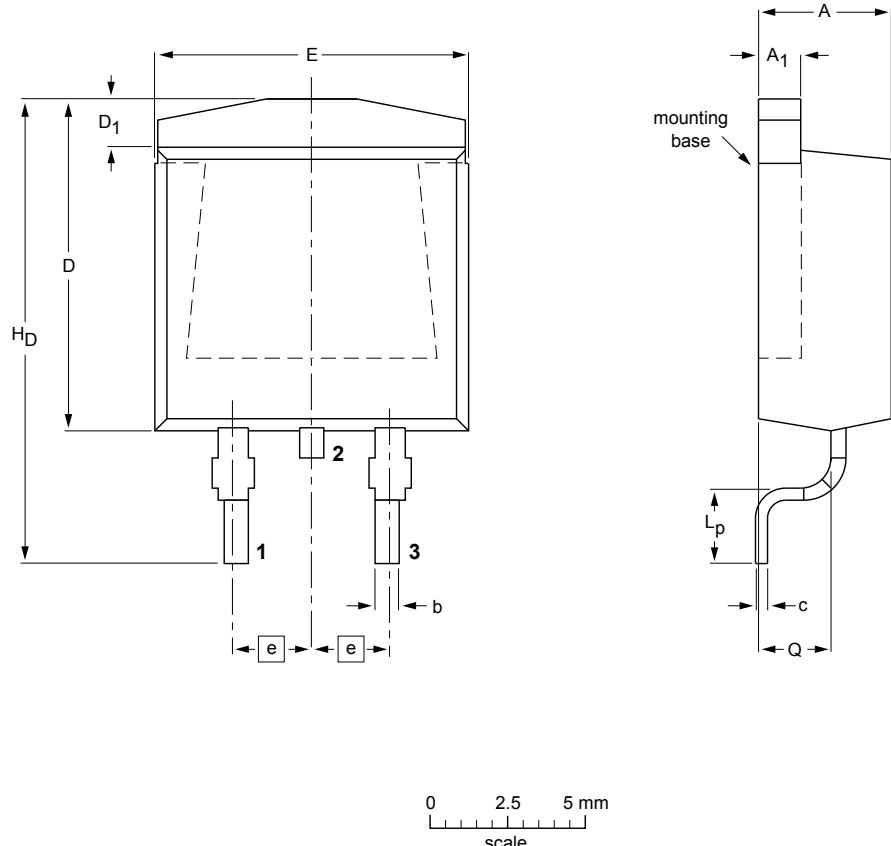
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8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	$D_{max.}$	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig. 17. D2PAK (SOT404)

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9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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