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BUK9Y15-60E

N-channel 60 V, 15 mΩ logic level MOSFET in LPAK56

16 March 2016

Product data sheet

1. General description

Logic level N-channel MOSFET in an LPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	60	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	53	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	95	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	12.1	15	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 15\text{ A}$; $V_{DS} = 48\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	6	-	nC



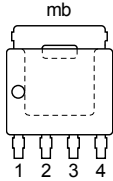
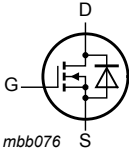
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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y15-60E	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y15-60E	91560E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$	-10	10	V
		Pulsed; $T_j \leq 175\text{ °C}$	[1][2]	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	95	W
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	53	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	37.4	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	212	A

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Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	53	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	212	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 53 A; V _{sup} ≤ 60 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[3][4]	-	42.7 mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

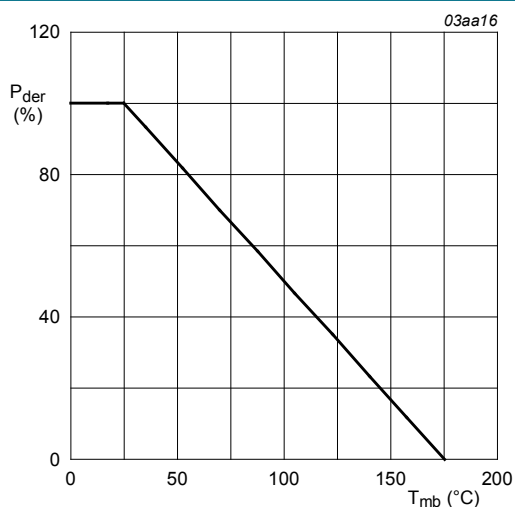


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

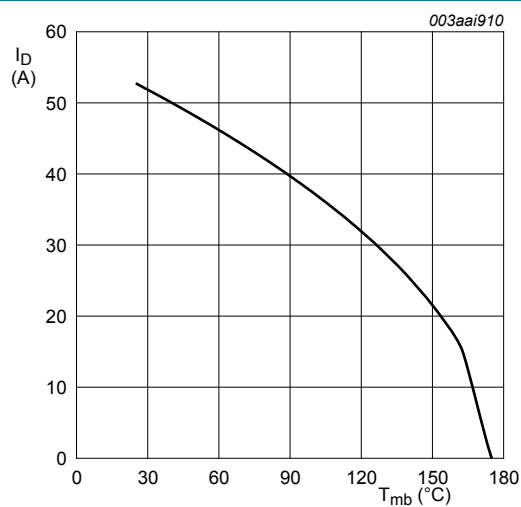


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 5V$$

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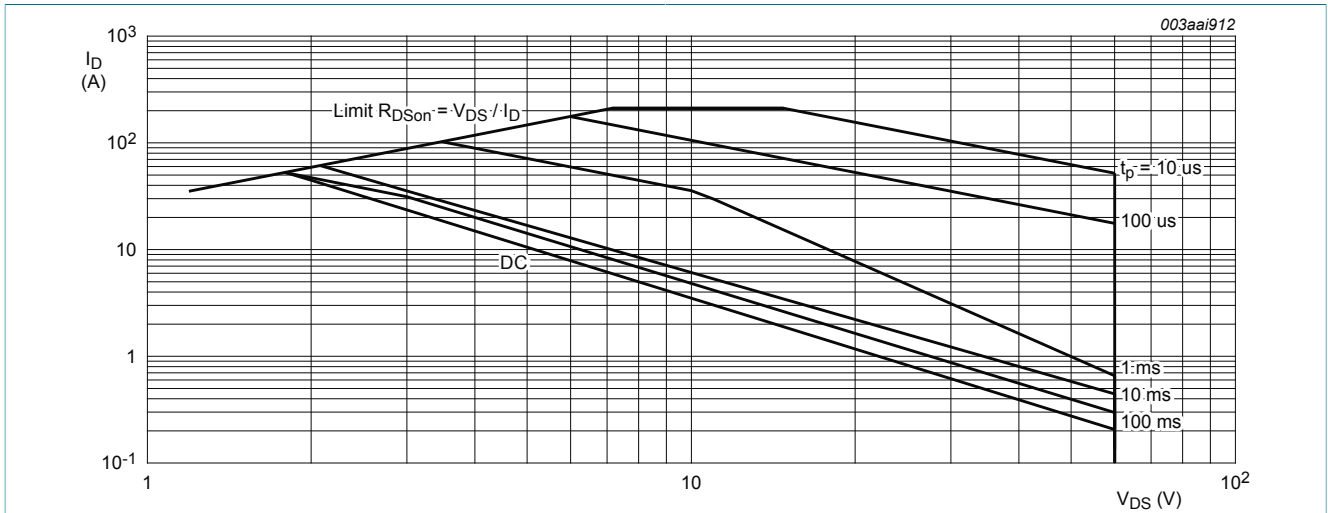


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

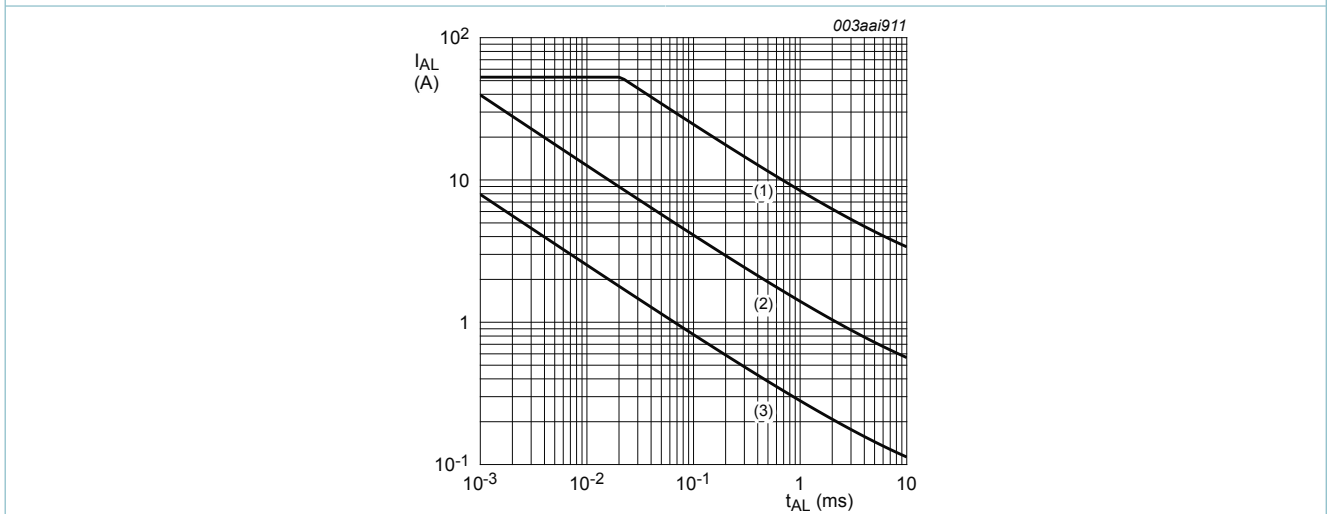


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(init)} = 25^{\circ}\text{C}$; (2) $T_{j(init)} = 150^{\circ}\text{C}$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	1.58	K/W

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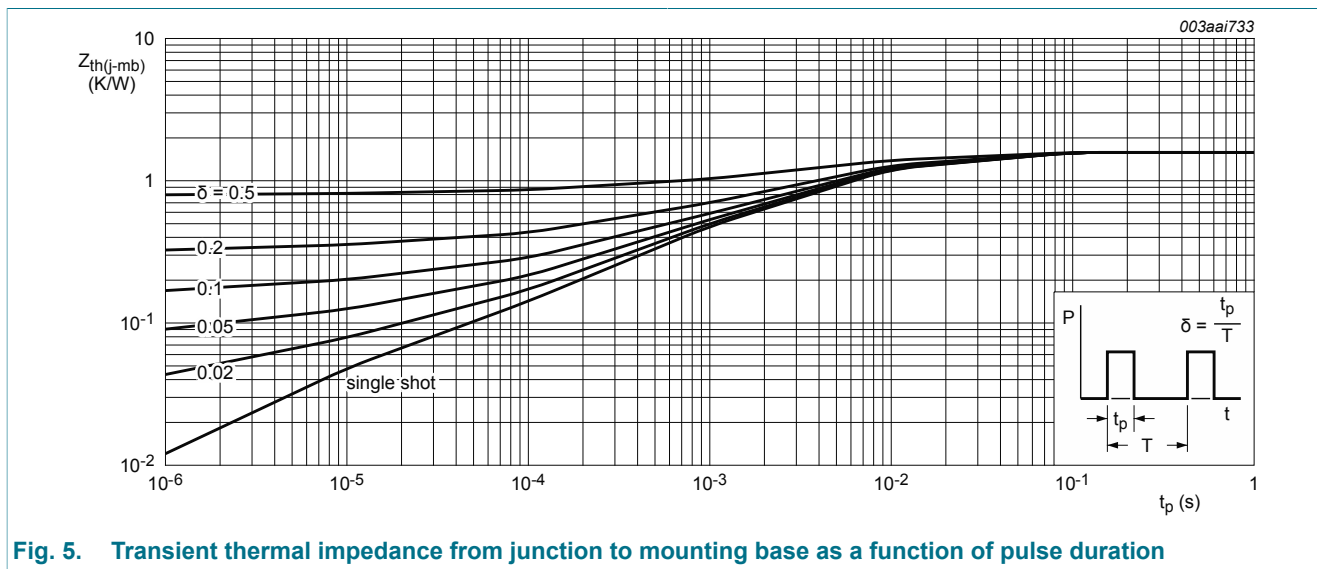


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

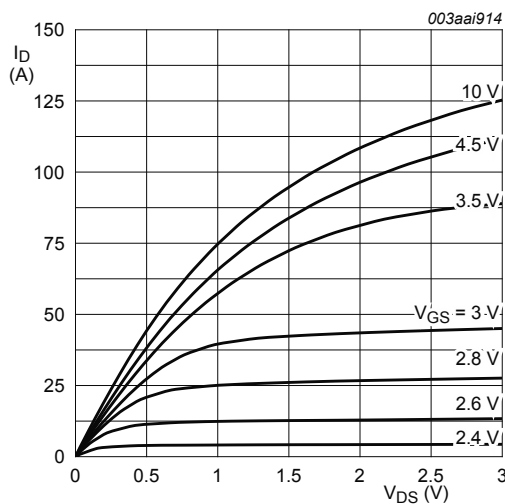
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	60	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	54	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C; Fig. 9 ; Fig. 10	1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C; Fig. 9	-	-	2.45	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 9	0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	1	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 15 A; T _j = 25 °C; Fig. 11	-	12.1	15	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; Fig. 11	-	10.8	13	mΩ
		V _{GS} = 5 V; I _D = 15 A; T _j = 175 °C; Fig. 12 ; Fig. 11	-	-	33.9	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 15 A; V _{DS} = 48 V; V _{GS} = 5 V; T _j = 25 °C; Fig. 13 ; Fig. 14	-	17.2	-	nC
Q _{GS}	gate-source charge		-	4.9	-	nC
Q _{GD}	gate-drain charge		-	6	-	nC

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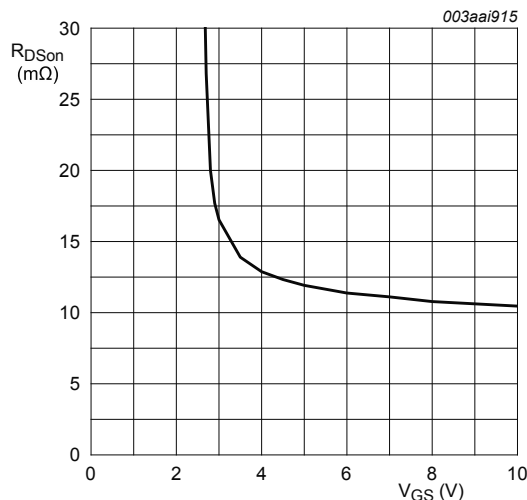
N-channel 60 V, 15 mΩ logic level MOSFET in LFPK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	1952	2603	pF
C_{oss}	output capacitance		-	182	218	pF
C_{rss}	reverse transfer capacitance		-	100	137	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 45\text{ V}; R_L = 3\text{ }^\Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 5\text{ }^\Omega; T_j = 25\text{ }^\circ\text{C}$	-	11.4	-	ns
t_r	rise time		-	17.3	-	ns
$t_{d(off)}$	turn-off delay time		-	25.2	-	ns
t_f	fall time		-	15.3	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	0.83	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	20.7	-	ns
Q_r	recovered charge		-	18.7	-	nC



$T_j = 25\text{ }^\circ\text{C}$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}; I_D = 15\text{ A}$

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

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N-channel 60 V, 15 mΩ logic level MOSFET in LPAK56

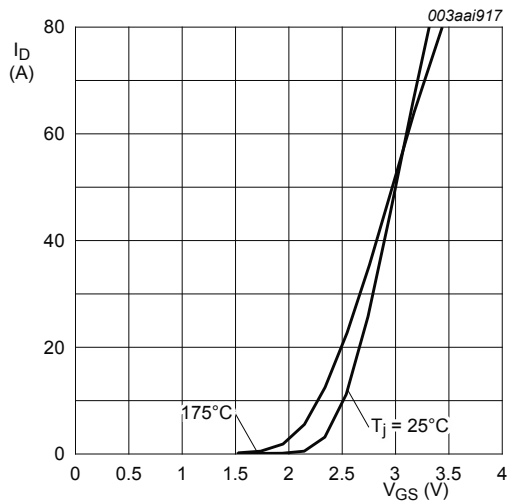


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

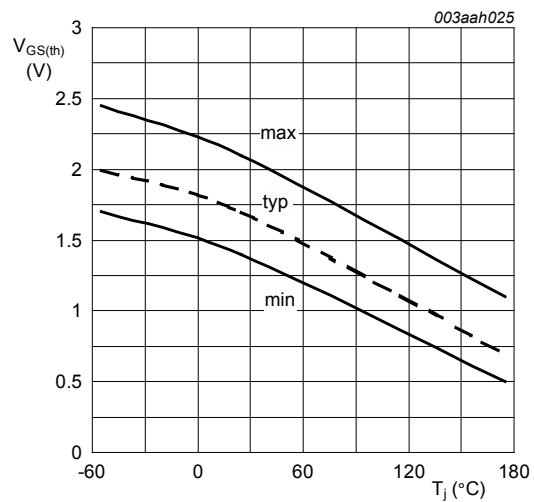


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

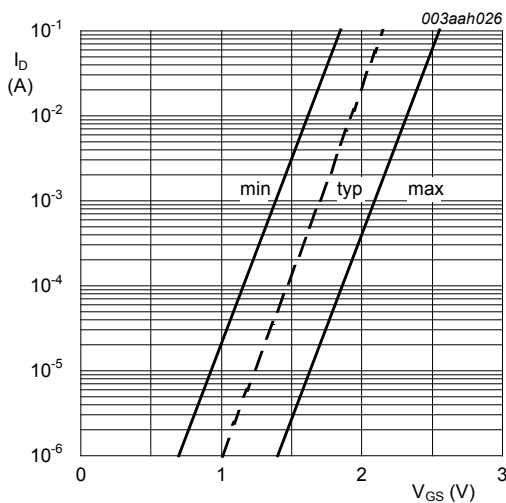
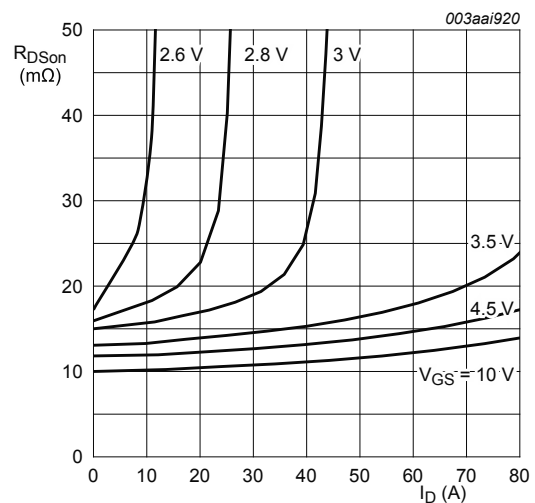


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5V$



$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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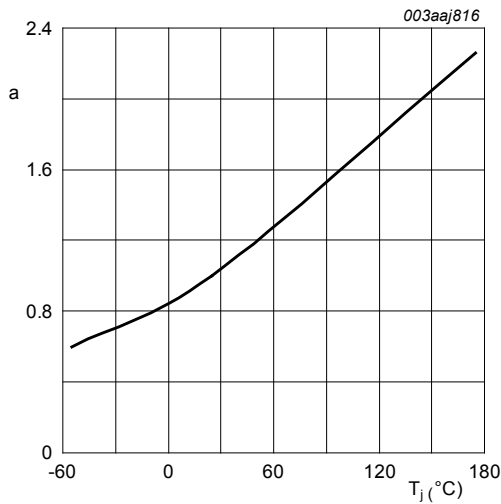


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

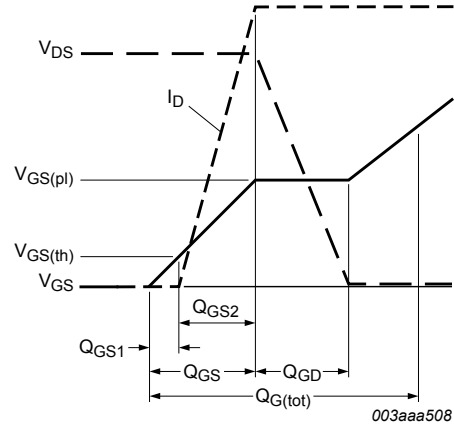


Fig. 13. Gate charge waveform definitions

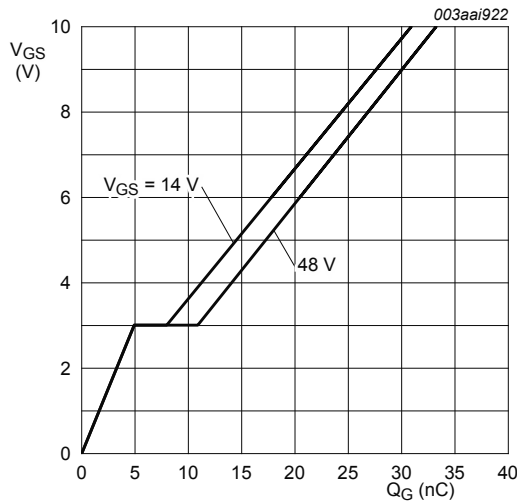


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^{\circ}C; I_D = 15A$

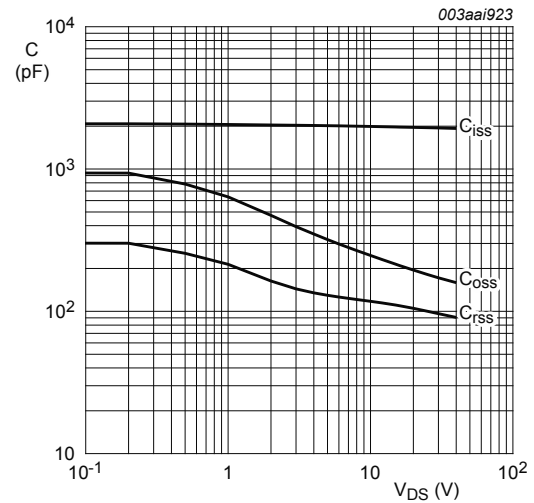


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

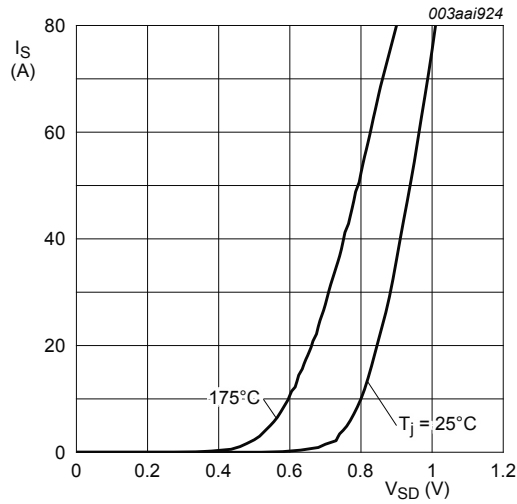


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

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11. Package outline

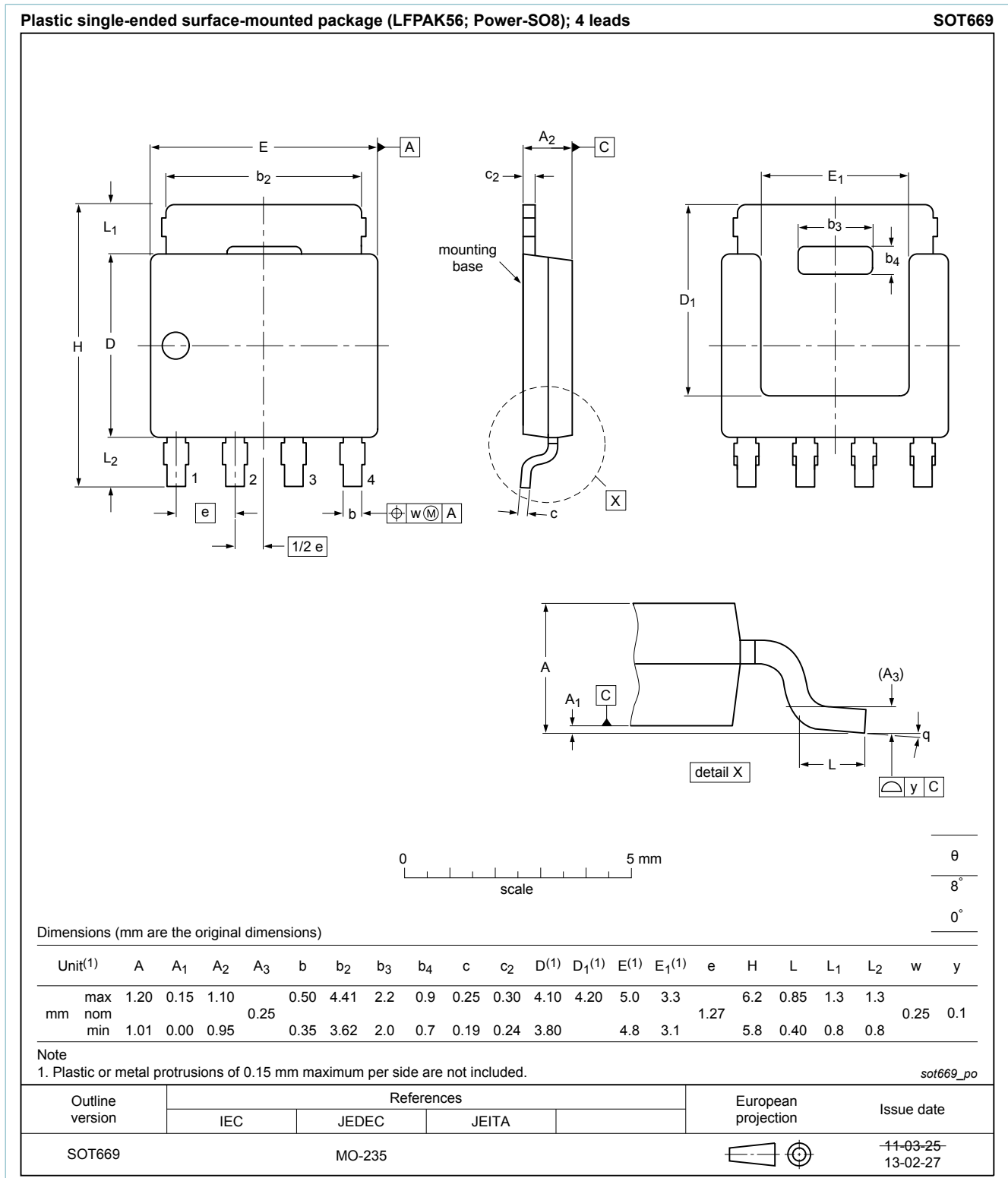


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 16 March 2016