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Texas Instruments SN75183N

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Datasheet of SN75183N - IC DUAL DIFF LINE DRIVER 14-DIP

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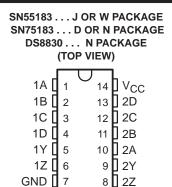
## DS8830, SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

SLLS093D - OCTOBER 1972 - REVISED APRIL 1998

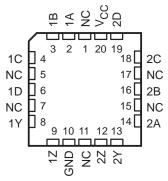
- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- Short-Circuit Protection of Outputs
- Output Clamp Diodes to Terminate Line Transients
- High-Current Outputs
- Quad Inputs
- Single-Ended or Differential AND/NAND Outputs
- Designed for Use With Dual Differential Drivers SN55182 and SN75182
- Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830

## description

The DS8830, SN55183, and SN75183 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. These devices can be used as TTL expander/phase splitters, because the output stages are similar to TTL totem-pole outputs.







NC - No internal connection

# THE DS8830 AND SN55183 ARE NOT RECOMMENDED FOR NEW DESIGNS

The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55183 is characterized for operation over the full military temperature range of –55°C to 125°C. The DS8830 and SN75183 are characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





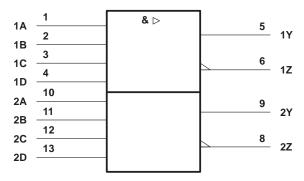
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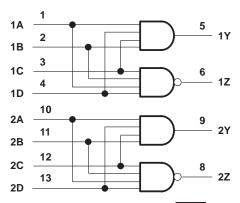
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## logic symbol†



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, and W packages.

## logic diagram (positive logic)



Positive logic: y = ABCD,  $Z = \overline{ABCD}$ 

Pin numbers shown are for the D, J, N, and W packages.



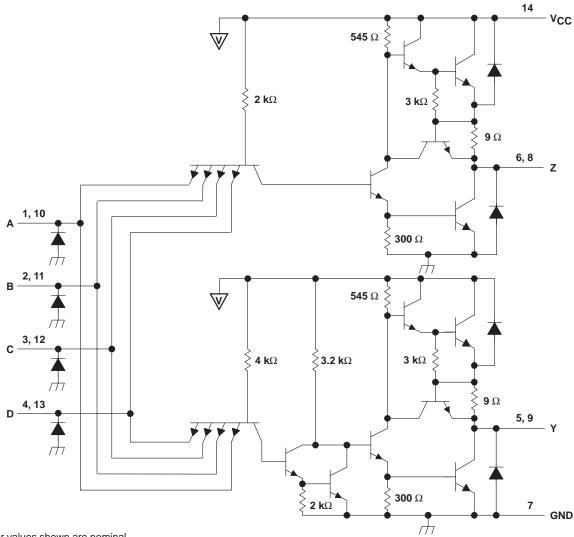


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# DS8830, SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

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## schematic (each driver)



Resistor values shown are nominal.

Pin numbers shown are for the D, J, N, and W packages.





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## DS8830, SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub> (see Note 1)	7 V
Input voltage, V <sub>I</sub> 5.	.5 V
Duration of output short circuit (see Note 2)	1 s
Continuous total power dissipation See Dissipation Rating Ta	able
Storage temperature range, T <sub>stq</sub> –65°C to 150	0°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	0°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	0°C
Case temperature for 60 seconds, T <sub>c</sub> : FK package	0°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.

2. Not more than one output should be shorted to ground at any one time.

### **DISSIPATION RATING TABLE**

PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	_
FK <sup>‡</sup>	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	_
w‡	1000 mW	8.0 mW/°C	640 mW	200 mW

<sup>‡</sup> In the FK, J, and W packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

### recommended operating conditions

	SN55183			1	UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, VIH	2			2			V
Low-level input voltage, V <sub>IL</sub>			8.0			0.8	V
High-level output current, IOH			-40			-40	mA
Low-level output current, IOL			40			40	mA
Operating free-air temperature, T <sub>A</sub>	-55		125	0		70	°C





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## DS8830, SN55183, SN75183 **DUAL DIFFERENTIAL LINE DRIVERS**

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## electrical characteristics over recommended ranges of V<sub>CC</sub> and operating free-air temperature (unless otherwise noted)

	PARAMETER		TE	ST CONDITIONS	MIN	TYP†	MAX	UNIT	
Va	High lovel output voltage	Y (AND) outputs	V 2 V	I <sub>OH</sub> = -0.8 mA	2.4			٧	
VOH	High-level output voltage	f (AND) outputs	V <sub>IH</sub> = 2 V	I <sub>OH</sub> = -40 mA	1.8	3.3		V	
V.01	Low-level output voltage	Y (AND) outputs	V <sub>II</sub> = 0.8 V	I <sub>OL</sub> = 32 mA		0.2		V	
VOL	Low-level output voltage	1 (AND) outputs	VIL = 0.0 V	I <sub>OL</sub> = 40 mA		0.22	0.4	V	
VOH	High-level output voltage	Z (NAND) outputs	V <sub>IL</sub> = 0.8 V	$I_{OH} = -0.8 \text{ mA}$	2.4			V	
VOH	r light-level output voltage	Z (NAND) outputs	VIL = 0.0 V	$I_{OH} = -40 \text{ mA}$	1.8	3.3		V	
Voi	Low-level output voltage	7 (NAND) outpute	Z (NAND) outputs	V <sub>IH</sub> = 2 V	$I_{OL} = 32 \text{ mA}$		0.2		V
VOL	Low-level output voltage	Z (NAND) outputs	VIH - Z V	$I_{OL} = 40 \text{ mA}$		0.22	0.4	V	
lн	I <sub>IH</sub> High-level input current						120	μΑ	
Ц	I <sub>I</sub> Input current at maximum input voltage						2	mA	
I <sub>IL</sub> Low-level input current			V <sub>IL</sub> = 0.4 V				-4.8	mA	
los	IOS Short-circuit output current‡			T <sub>A</sub> =125°C§	-40	-100	-120	mA	
ICC	Supply current (average pe	er driver)	V <sub>CC</sub> = 5 V,	All inputs at 5 V, No load		10	18	mA	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST C	CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low- to high-level Y output	AND gates	C <sub>L</sub> = 15 pF, See Figure 1(a)		8	12	ns
tPHL	Propagation delay time, high- to low-level Y output	AND gates	C <sub>L</sub> = 15 pF, See Figure 1(a)		12	18	ns
tPLH	Propagation delay time, low- to high-level Z output	NAND gates	C <sub>L</sub> = 15 pF, See Figure 1(a)		6	12	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level Z output	NAND gates	C <sub>L</sub> = 15 pF, See Figure 1(a)		6	8	ns
<sup>t</sup> PLH	Propagation delay time, low- to high-level differential output	Y output with re $R_L = 100 \Omega$ in s See Figure 1(b)		9	16	ns	
<sup>t</sup> PHL	Propagation delay time, high- to low-level differential output	Y output with respect to Z output, $R_L = 100 \ \Omega$ in series with 5000 pF, See Figure 1(b)			8	16	ns

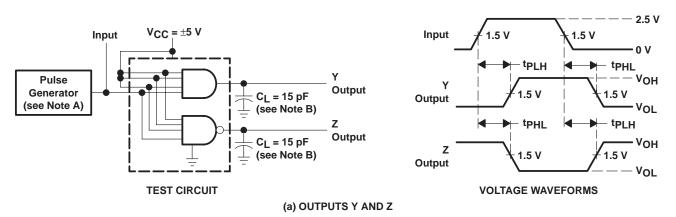


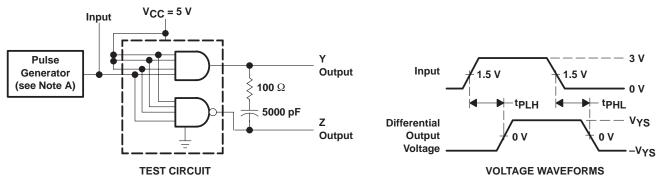
<sup>†</sup> Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second. § T<sub>A</sub> = 125°C is applicable to SN55183 only.

## DS8830, SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

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### PARAMETER MEASUREMENT INFORMATION





(b) DIFFERENTIAL OUTPUT

NOTES: A. The pulse generators have the following characteristics:  $Z_O = 50 \Omega$ ,  $t_f \le 10$  ns,  $t_W = 0.5 \mu$ s, PRR  $\le 1$  MHz.

- B. C<sub>L</sub> includes probe and jig capacitance.
- C. Waveforms are monitored on an oscilloscope with  $r_i \ge 1$  M $\Omega$ .

Figure 1. Test Circuits and Voltage Waveforms



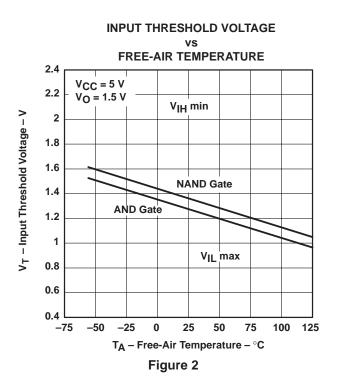


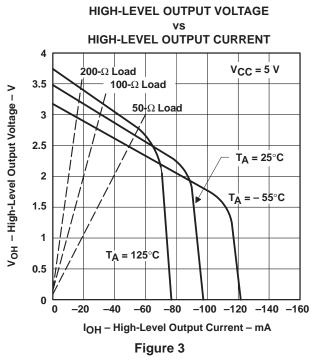
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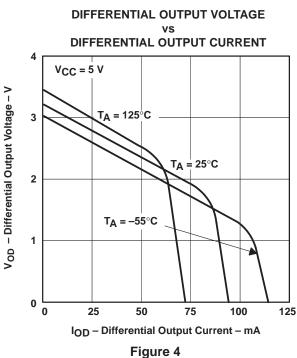
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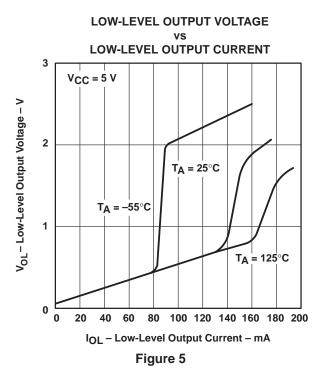
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### TYPICAL CHARACTERISTICS<sup>†</sup>









<sup>†</sup> Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.



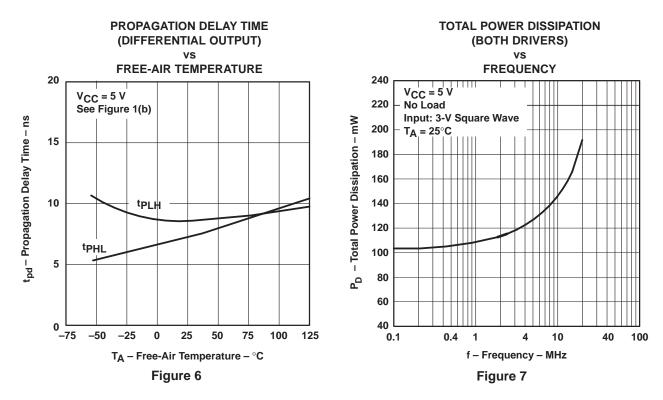
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### TYPICAL CHARACTERISTICS<sup>†</sup>



<sup>†</sup> Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.



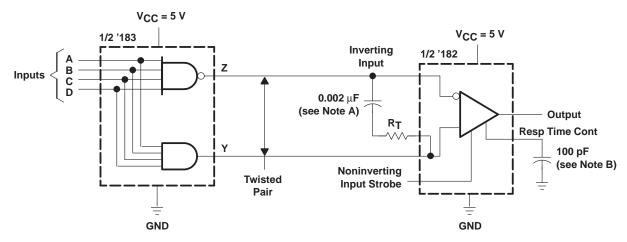
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## DS8830, SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

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### **APPLICATION INFORMATION**



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor.

At the frequency of operation, the impedance of the capacitor should be relatively small.

$$\begin{split} \text{Example: let} \quad & f = 5 \text{ MHz} \\ \quad & C = 0.002 \, \mu\text{F} \\ Z_{\text{(circuit)}} = \frac{1}{2\pi\text{fC}} = \frac{1}{2\pi(5\times10^6)(0.002\times10^{-6})} \\ Z_{\text{(circuit)}} \approx & 16\Omega \end{split}$$

B. Use of a capacitor to control response time is optional.

Figure 8. Transmission of Digital Data Over Twisted-Pair Line





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PACKAGE OPTION ADDENDUM

17-Dec-2015

### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing		Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7900901VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7900901VC A SNV55183J	Samples
7900901CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7900901CA SNJ55183J	Samples
DS8830N	OBSOLETI	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN55183J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55183J	Samples
SN75183D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183	Samples
SN75183DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183	Samples
SN75183N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75183N	Samples
SN75183NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75183N	Samples
SN75183NSR	ACTIVE	so	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183	Samples
SNJ55183J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7900901CA SNJ55183J	Samples

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design. PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

 $\begin{tabular}{ll} \textbf{OBSOLETE:} TI has discontinued the production of the device. \\ \end{tabular}$ 

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability

The Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight

Addendum-Page 1



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PACKAGE OPTION ADDENDUM

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF SN55183, SN55183-SP, SN75183:

- Catalog: SN75183, SN55183
- Military: SN55183
- Space: SN55183-SP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

Addendum-Page 2

Datasheet of SN75183N - IC DUAL DIFF LINE DRIVER 14-DIP

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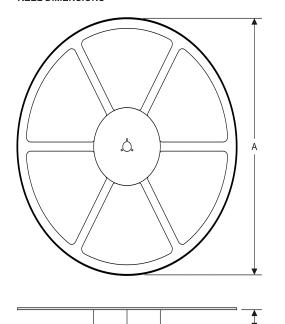


# **PACKAGE MATERIALS INFORMATION**

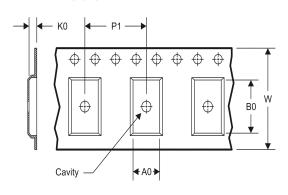
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### **TAPE AND REEL INFORMATION**

### **REEL DIMENSIONS**



### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75183NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



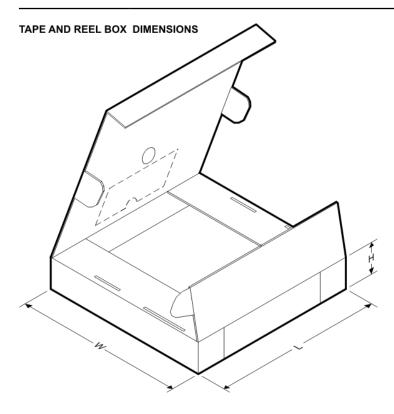
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# **PACKAGE MATERIALS INFORMATION**

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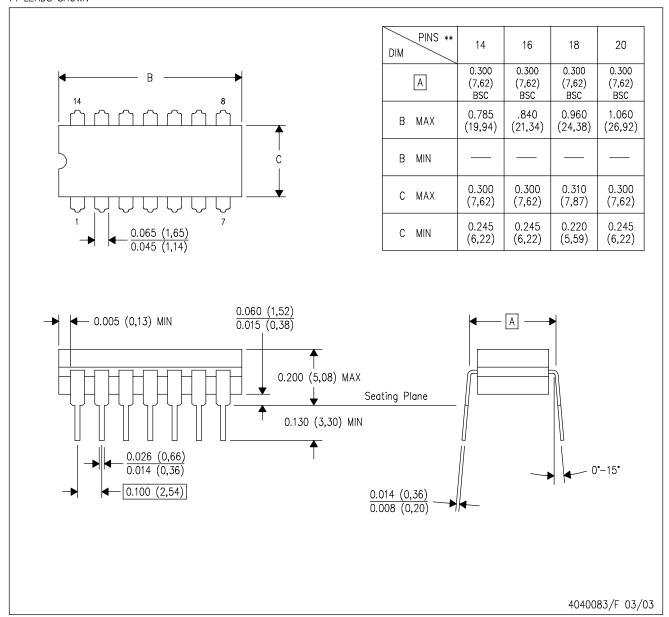
### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75183NSR	SO	NS	14	2000	367.0	367.0	38.0

# J (R-GDIP-T\*\*)

## CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

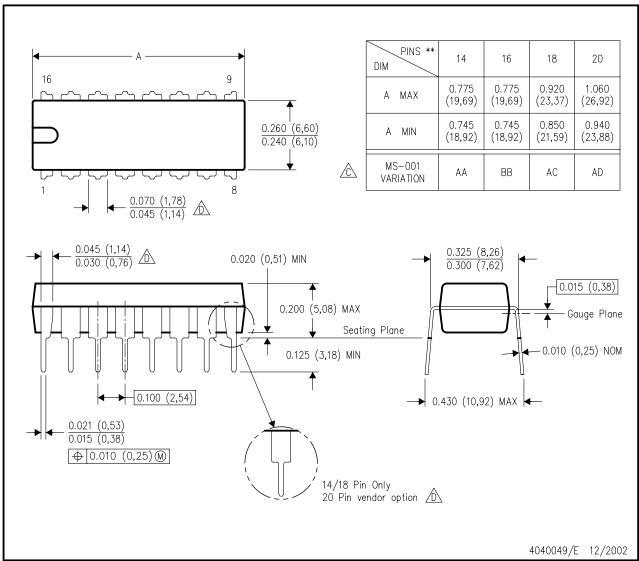


### **MECHANICAL DATA**

# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- . All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.

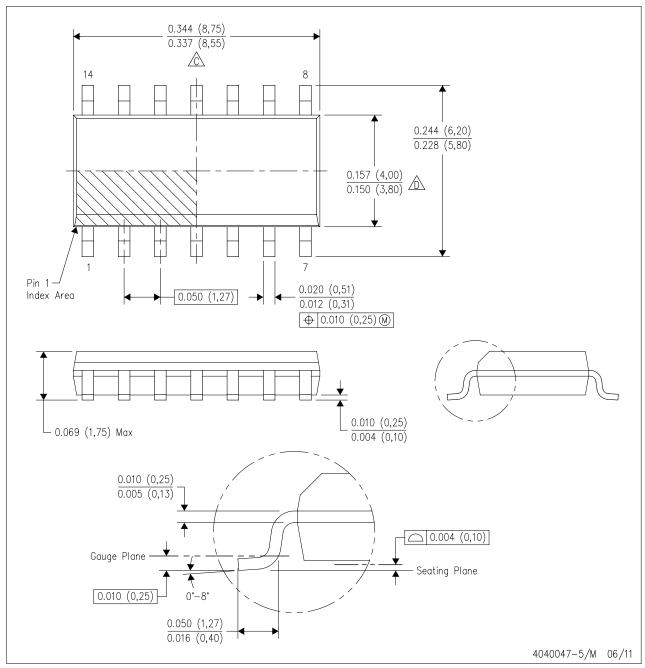




## **MECHANICAL DATA**

# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



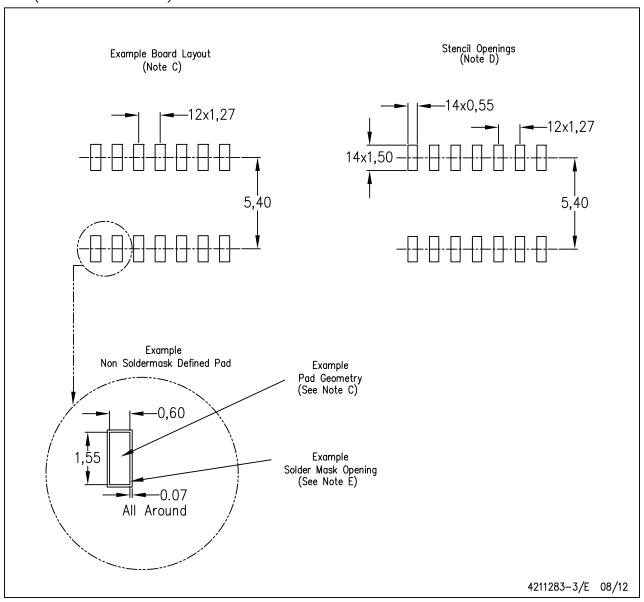




### LAND PATTERN DATA

# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

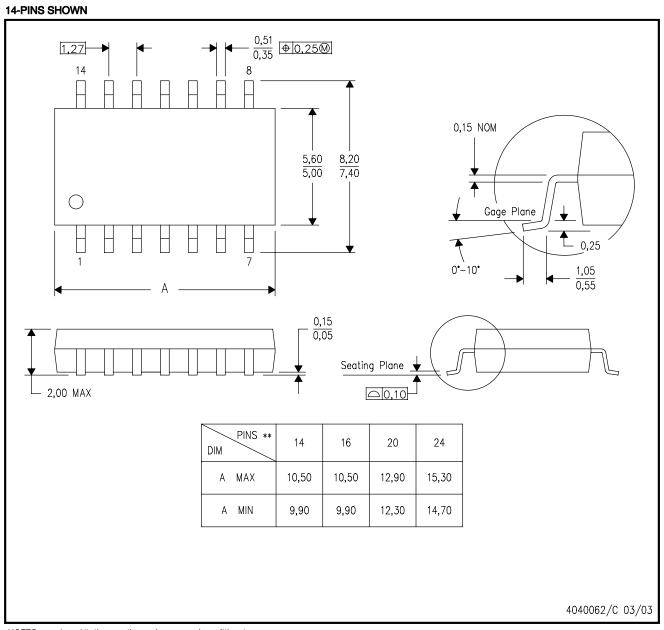


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### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE PACKAGE



- All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.





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