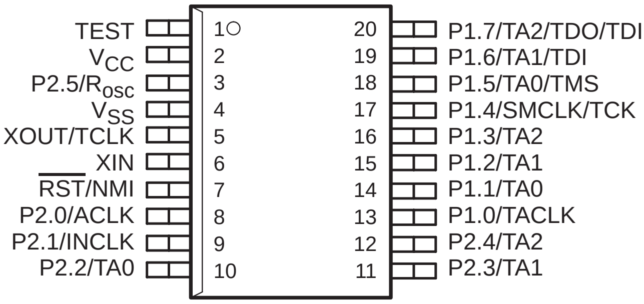
MSP430F11x
MIXED SIGNAL MICROCONTROLLER

SLAS256D − NOVEMBER 1999 − REVISED SEPTEMBER 2004

- **Low Supply Voltage Range 1.8 V to 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 200 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.8 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Wake-Up From Standby Mode in less than 6 µs**
- **16-Bit RISC Architecture, 125 ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Various Internal Resistors**
  - **Single External Resistor**
  - **32 kHz Crystal**
  - **High Frequency Crystal**
  - **Resonator**
  - **External Clock Source**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **Serial Onboard Programming, No External Programming Voltage Needed**
- **Family Members Include:**
  MSP430F110: 1KB + 128B Flash Memory 128B RAM
  MSP430F112: 4KB + 256B Flash Memory 256B RAM
- **Available in a 20-Pin Plastic Small-Outline Wide Body (SOWB) Package and 20-Pin Plastic Thin Shrink Small-Outline Package (TSSOP)**
- **For Complete Module Descriptions, Refer to the *MSP430x1xx Family User's Guide*, Literature Number SLAU049**

DW OR PW PACKAGE
(TOP VIEW)



description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6µs.

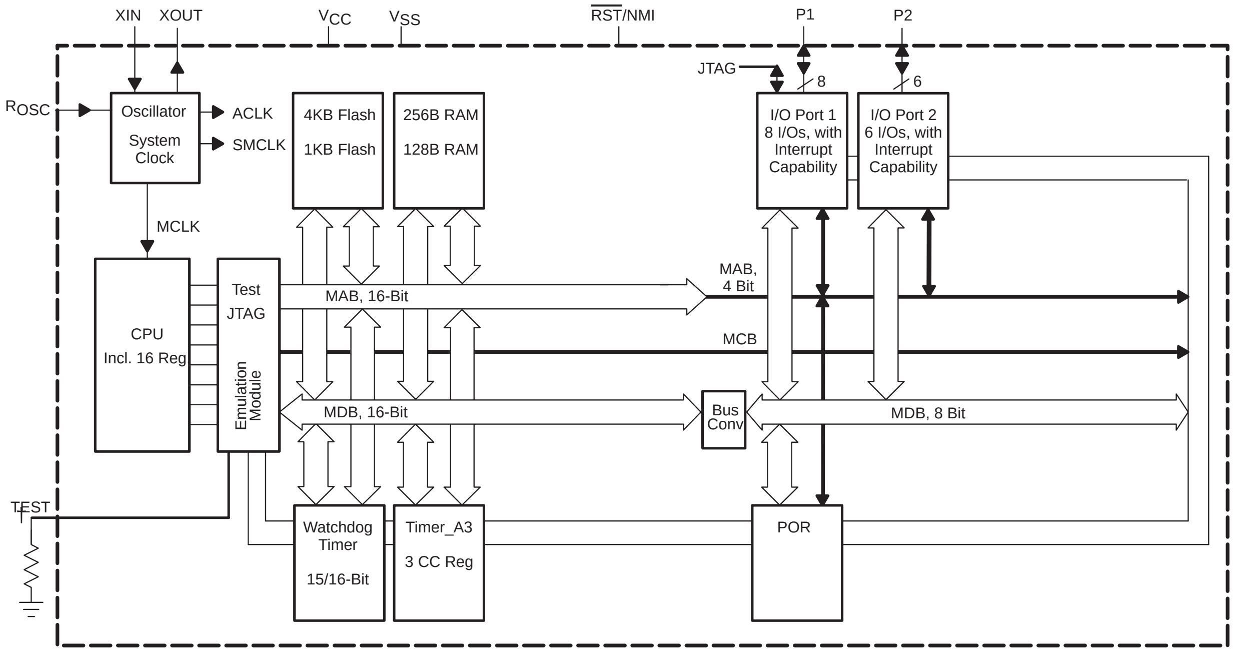
The MSP430F11x series is an ultralow-power mixed signal microcontroller with a built in 16-bit timer and fourteen I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data and display them or transmit them to a host system. Stand alone RF sensor front-end is another area of application.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 20-PIN SOWB (DW)	PLASTIC 20-PIN TSSOP (PW)
−40°C to 85°C	MSP430F110IDW MSP430F112IDW	MSP430F110IPW MSP430F112IPW

functional block diagram



† A pulldown resistor of 30 kΩ is needed on F11x devices.

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
P1.0/TACLK	13	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	16	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK/TCK	17	I/O	General-purpose digital I/O pin/SMCLK signal output/test clock, input terminal for device programming and test
P1.5/TA0/TMS	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output/test mode select, input terminal for device programming and test
P1.6/TA1/TDI	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/test data input terminal
P1.7/TA2/TDO/TDI†	20	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/test data output terminal or data input during programming
P2.0/ACLK	8	I/O	General-purpose digital I/O pin/ACLK output
P2.1/INCLK	9	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/TA0	10	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input, compare: Out0 output/BSL receive
P2.3/TA1	11	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1B input, compare: Out1 output
P2.4/TA2	12	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output
P2.5/R_{OSC}	3	I/O	General-purpose digital I/O pin/Input for external resistor that defines the DCO nominal frequency
$\overline{RST}$/NMI	7	I	Reset or nonmaskable interrupt input
TEST	1	I	Selects test mode for JTAG pins on Port1. Must be tied low with less than 30 kΩ.
V_{CC}	2		Supply voltage
V_{SS}	4		Ground reference
XIN	6	I	Input terminal of crystal oscillator
XOUT/TCLK	5	I/O	Output terminal of crystal oscillator or test clock input

† TDO or TDI is selected via JTAG instruction.

short-form description

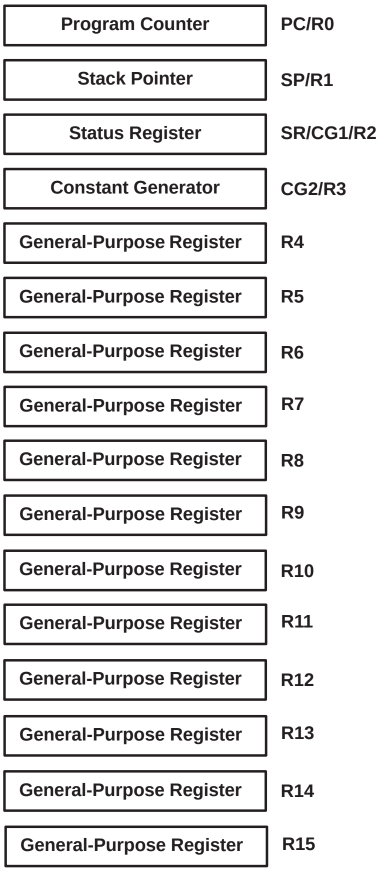
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 −−−> R5
Single operands, destination only	e.g. CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 −−> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)−−> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) −−> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) −−> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) −−> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) −−> R11 R10 + 2−−> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 −−> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the memory with an address range of 0FFFFh-0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog	WDTIFG (Note1) KEYV (Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator fault Flash memory access violation	NMIIFG (Notes 1 and 5) OFIFG (Notes 1 and 5) ACCVIFG (Notes 1 and 5)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	14
			0FFFAh	13
			0FFF8h	12
			0FFF6h	11
Watchdog timer	WDTIFG	maskable	0FFF4h	10
Timer_A3	TACCR0 CCIFG (Note 2)	maskable	0FFF2h	9
Timer_A3	TACCR1 and TACCR2 CCIFGs, TAIFG (Notes 1 and 2)	maskable	0FFF0h	8
			0FFEEh	7
			0FFECh	6
			0FFEAh	5
			0FFE8h	4
I/O Port P2 (eight flags − see Note 3)	P2IFG.0 to P2IFG.7 (Notes 1 and 2)	maskable	0FFE6h	3
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (Notes 1 and 2)	maskable	0FFE4h	2
			0FFE2h	1
			0FFE0h	0, lowest

NOTES:
1. Multiple source flags
2. Interrupt flags are located in the module
3. There are eight Port P2 interrupt flags, but only six Port P2 I/O pins (P2.0−5) are implemented on the ’11x devices.
4. Nonmaskable: neither the individual nor the general interrupt enable bit will disable an interrupt event.
5. (non)-maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE: Oscillator fault enable
NMIIE: Nonmaskable interrupt enable
ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h								

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw-0			rw-1	rw-(0)

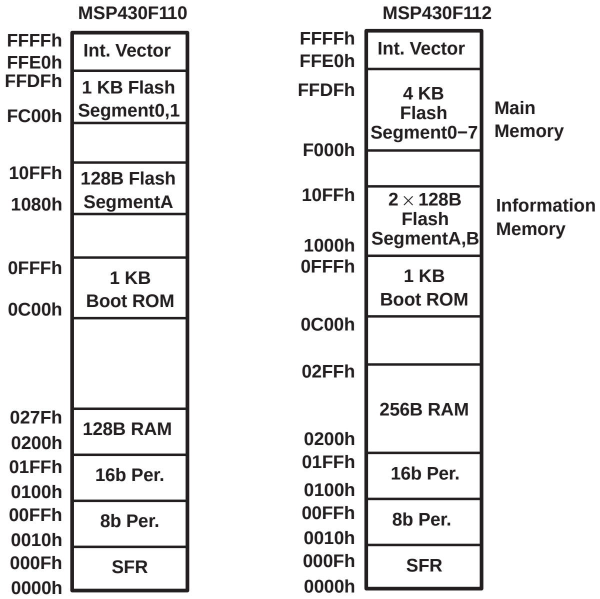
WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-up or a reset condition at RST/NMI pin in reset mode.
OFIFG: Flag set on oscillator fault
NMIIFG: Set via RST/NMI-pin

Address	7	6	5	4	3	2	1	0
03h								

Legend

rw:	Bit can be read and written.
rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
(shaded box)	SFR bit is not present in device.

memory organization



bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

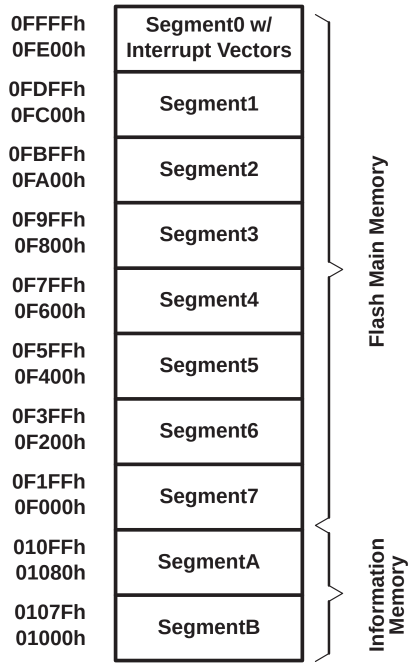
BSL Function	DW & PW Package Pins
Data Transmit	14 - P1.1
Data Receive	10 - P2.2

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0−n.
  Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

flash memory (continued)



NOTE: All segments not implemented on all devices.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x1xx Family User's Guide*, literature number SLAU049.

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

digital I/O

There are two 8-bit I/O ports implemented—ports P1 and P2 (only six P2 I/O signals are available on external pins):

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and six bits of port P2.
- Read/write access to port-control registers is supported by all instructions.

NOTE:
Six bits of port P2, P2.0 to P2.5, are available on external pins − but all control and data bits for port P2 are implemented.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections

Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
13 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
9 - P2.1	INCLK	INCLK			
14 - P1.1	TA0	CCI0A	CCR0	TA0	14 - P1.1
10 - P2.2	TA0	CCI0B			18 - P1.5
	DV_{SS}	GND			10 - P2.2
	DV_{CC}	V_{CC}			
15 - P1.2	TA1	CCI1A	CCR1	TA1	15 - P1.2
11 - P2.3	TA1	CCI1B			19 - P1.6
	DV_{SS}	GND			11 - P2.3
	DV_{CC}	V_{CC}			
16 - P1.3	TA2	CCI2A	CCR2	TA2	16 - P1.3
	ACLK (internal)	CCI2B			20 - P1.7
	DV_{SS}	GND			12 - P2.4
	DV_{CC}	V_{CC}			

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Timer_A	Reserved		017Eh
	Reserved		017Ch
	Reserved		017Ah
	Reserved		0178h
	Capture/compare register	TACCR2	0176h
	Capture/compare register	TACCR1	0174h
	Capture/compare register	TACCR0	0172h
	Timer_A register	TAR	0170h
	Reserved		016Eh
	Reserved		016Ch
	Reserved		016Ah
	Reserved		0168h
	Capture/compare control	TACCTL2	0166h
	Capture/compare control	TACCTL1	0164h
	Capture/compare control	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog	Watchdog/timer control	WDTCTL	0120h
PERIPHERALS WITH BYTE ACCESS			
Basic Clock	Basic clock sys. control2	BCSCTL2	058h
	Basic clock sys. control1	BCSCTL1	057h
	DCO clock freq. control	DCOCTL	056h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings†

Voltage applied at V_{CC} to V_{SS} . . . . −0.3 V to 4.1 V
Voltage applied to any pin (referenced to V_{SS}) . . . . −0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device) . . . . −55°C to 150°C
Storage temperature, T_{stg} (programmed device) . . . . −40°C to 85°C

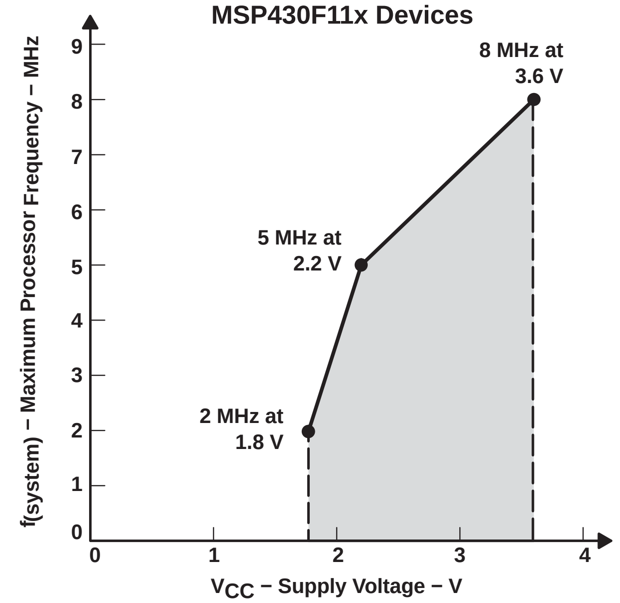
† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (see Note 1)			1.8		3.6	V
Supply voltage during program/erase flash memory, V_{CC}			2.7		3.6	V
Supply voltage, V_{SS}				0		V
Operating free-air temperature range, T_A			−40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)	LF mode selected, XTS=0	Watch crystal		32768		Hz
	XT1 mode selected, XTS=1	Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	kHz
Processor frequency $f_{(system)}$ (MCLK signal)		V_{CC} = 1.8 V	dc		2	MHz
		V_{CC} = 2.2 V	dc		5	MHz
		V_{CC} = 3.6 V	dc		8	MHz

NOTES: 1. The LFXT1 oscillator in LF-mode requires a resistor of 5.1 MΩ from XOUT to V_{SS} when V_{CC} <2.5 V.
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal frequency of 4 MHz at $V_{CC} \geq 2.2$ V.
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal frequency of 8 MHz at $V_{CC} \geq 2.8$ V.
2. The LFXT1 oscillator in LF-mode requires a watch crystal. The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or crystal.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.7 V.

Figure 1. Frequency vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current (into V_{CC}) excluding external current

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode	T_A = −40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 2.2 V		200	250	µA
				V_{CC} = 3 V		300	350	
		T_A = −40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz		V_{CC} = 2.2 V		1.6	3	µA
				V_{CC} = 3 V		3	4.3	
$I_{(CPUOff)}$	Low-power mode, (LPM0)	T_A = −40°C +85°C, $f_{(MCLK)}$ = 0, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 2.2 V		32	45	µA
				V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2)	T_A = −40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 0		V_{CC} = 2.2 V		11	14	µA
				V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3)	T_A = −40°C		V_{CC} = 2.2 V		0.8	1.2	µA
		T_A = 25°C				0.7	1	
		T_A = 85°C				1.6	2.3	
		T_A = −40°C		V_{CC} = 3 V		1.8	2.2	µA
		T_A = 25°C				1.6	1.9	
		T_A = 85°C				2.3	3.4	
$I_{(LPM4)}$	Low-power mode, (LPM4)	T_A = −40°C	$f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	V_{CC} = 2.2 V/3 V		0.1	0.5	µA
		T_A = 25°C				0.1	0.5	
		T_A = 85°C				0.8	1.9	

NOTE: All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

current consumption of active mode versus system frequency, F version

$$I_{AM} = I_{AM[1\ MHz]} \times f_{system}\ [MHz]$$

current consumption of active mode versus supply voltage, F version

$$I_{AM} = I_{AM[3\ V]} + 120\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Schmitt-trigger inputs Port 1 to Port P2; P1.0 to P1.7, P2.0 to P2.5

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.3	V
		V_{CC} = 3 V	1.5		1.8	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	.90		1.2	
V_{hys}	Input voltage hysteresis, ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1	V
		V_{CC} = 3 V	0.5		1.4	

standard inputs − $\overline{RST}$/NMI; TCK, TMS, TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 2.2 V / 3 V	V_{SS}		V_{SS}+0.6	V
V_{IH}	High-level input voltage		0.8×V_{CC}		V_{CC}	V

inputs Px.x, TAx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, capture timing	TA0, TA1, TA2 (see Note 2)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
			3 V			10	
$f_{(TAint)}$	Timer_A clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.
2. The external capture signal triggers the capture event every time the mimimum $t_{(cap)}$ cycle and time parameters are met. A capture may be triggered with capture signals even shorter than $t_{(cap)}$. Both the cycle and timing specifications must be met to ensure a correct capture of the 16-bit timer value and to ensure the flag is set.

leakage current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	Port P1: P1.x, 0 ≤ × ≤ 7 (see Notes 1 and 2)	V_{CC} = 2.2 V/3 V,			±50	nA
		Port P2: P2.x, 0 ≤ × ≤ 5 (see Notes 1 and 2)	V_{CC} = 2.2 V/3 V,			±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin must be selected for input and there must be no optional pullup or pulldown resistor.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

outputs Port 1 to Port 2; P1.0 to P1.7, P2.0 to P2.5

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage Port 1	$I_{(OHmax)}$ = −1.5 mA	V_{CC} = 2.2 V	See Note 1	V_{CC}−0.25		V_{CC}	V
		$I_{(OHmax)}$ = −6 mA		See Note 2	V_{CC}−0.6		V_{CC}	
		$I_{(OHmax)}$ = −1.5 mA	V_{CC} = 3 V	See Note 1	V_{CC}−0.25		V_{CC}	
		$I_{(OHmax)}$ = −6 mA		See Note 2	V_{CC}−0.6		V_{CC}	
V_{OH}	High-level output voltage Port 2	$I_{(OHmax)}$ = −1 mA	V_{CC} = 2.2 V	See Note 3	V_{CC}−0.25		V_{CC}	V
		$I_{(OHmax)}$ = −3.4 mA		See Note 3	V_{CC}−0.6		V_{CC}	
		$I_{(OHmax)}$ = −1 mA	V_{CC} = 3 V	See Note 3	V_{CC}−0.25		V_{CC}	
		$I_{(OHmax)}$ = −3.4 mA		See Note 3	V_{CC}−0.6		V_{CC}	
V_{OL}	Low-level output voltage Port 1 and Port 2	$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 2.2 V	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA		See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 3 V	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA		See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
3. One output loaded at a time.

outputs P1.x, P2.x, TAx

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{(P20)}$	Output frequency	P2.0/ACLK, C_L = 20 pF		2.2 V/3 V			f_{System}	MHz
$f_{(TAx)}$		TA0, TA1, TA2, C_L = 20 pF Internal clock source, SMCLK signal applied (See Note 1)		2.2 V/3 V	dc		f_{System}	
$t_{(Xdc)}$	Duty cycle of O/P frequency	P1.4/SMCLK, C_L = 20 pF	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	2.2 V/3 V	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$		35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$		50%− 15 ns	50%	50%+ 15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	2.2 V/3 V	50%− 15 ns	50%	50%+ 15 ns	
		P2.0/ACLK, C_L = 20 pF	$f_{P20} = f_{LFXT1} = f_{XT1}$	2.2 V/3 V	40%		60%	
			$f_{P20} = f_{LFXT1} = f_{LF}$		30%		70%	
			$f_{P20} = f_{LFXT1/n}$			50%		
$t_{(TAdc)}$		TA0, TA1, TA2, C_L = 20 pF, Duty cycle = 50%		2.2 V/3 V		0	±50	ns

NOTE 1: The limits of the system clock MCLK have to be met. MCLK and SMCLK can have different frequencies.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PUC/POR

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(POR\_Delay)}$	POR		V_{CC} = 2.2 V/3 V		150	250	µs
V_{POR}		T_A = −40°C		1.4		1.8	V
		T_A = 25°C		1.1		1.5	V
		T_A = 85°C		0.8		1.2	V
$V_{(min)}$				0		0.4	V
$t_{(reset)}$	PUC/POR	Reset is accepted internally		2			µs

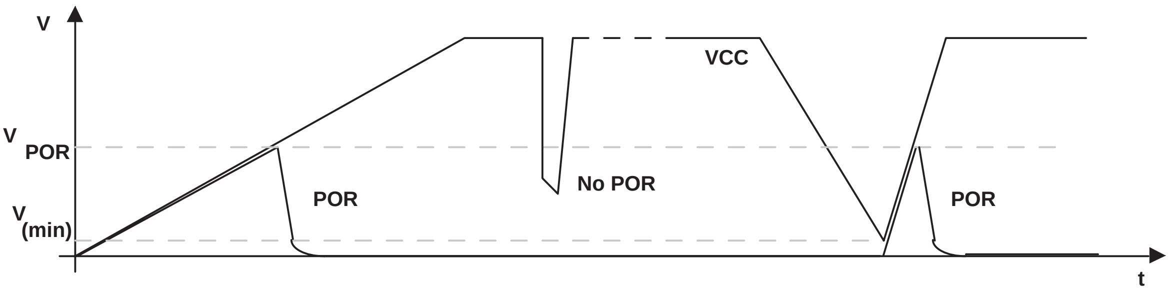


Figure 2. Power-On Reset (POR) vs Supply Voltage

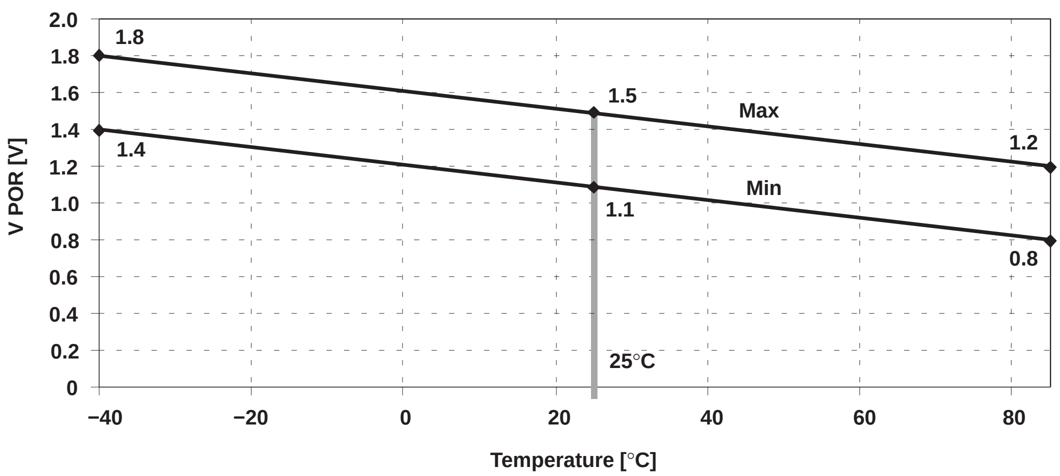


Figure 3. V_{POR} vs Temperature

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

wake-up from lower power modes (LPMx)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(LPM0)}$	Delay time (see Note 1)	V_{CC} = 2.2 V/3 V			100		ns
$t_{(LPM2)}$		V_{CC} = 2.2 V/3 V			100		
$t_{(LPM3)}$		$f_{(MCLK)}$ = 1 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 2 MHz,	V_{CC} = 2.2 V/3 V			6	
		$f_{(MCLK)}$ = 3 MHz,	V_{CC} = 2.2 V/3 V			6	
$t_{(LPM4)}$		$f_{(MCLK)}$ = 1 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 2 MHz,	V_{CC} = 2.2 V/3 V			6	
		$f_{(MCLK)}$ = 3 MHz,	V_{CC} = 2.2 V/3 V			6	

NOTE 1: Parameter applicable only if DCOCLK is used for MCLK.

RAM

PARAMETER		MIN	TYP	MAX	UNIT
$V_{(RAMh)}$	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V_{CC} = 3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V_{CC} = 3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V_{CC} = 3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V_{CC} = 3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V_{CC} = 3 V	0.61	0.75	0.9	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1	1.2	1.5	MHz
		V_{CC} = 3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1.6	1.9	2.2	MHz
		V_{CC} = 3 V	1.69	2.0	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	2.4	2.9	3.4	MHz
		V_{CC} = 3 V	2.7	3.2	3.65	
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	4	4.5	4.9	MHz
		V_{CC} = 3 V	4.4	4.9	5.4	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V/3 V	F_{DCO40} x1.7	F_{DCO40} x2.1	F_{DCO40} x2.5	MHz
$S_{(Rsel)}$	$S_R = f_{Rsel+1}/f_{Rsel}$	V_{CC} = 2.2 V/3 V	1.35	1.65	2	ratio
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1}/f_{DCO}$	V_{CC} = 2.2 V/3 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	V_{CC} = 2.2 V	−0.31	−0.36	−0.40	%/°C
		V_{CC} = 3 V	−0.33	−0.38	−0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	V_{CC} = 2.2 V/3 V	0	5	10	%/V

NOTE 1: These parameters are not production tested.

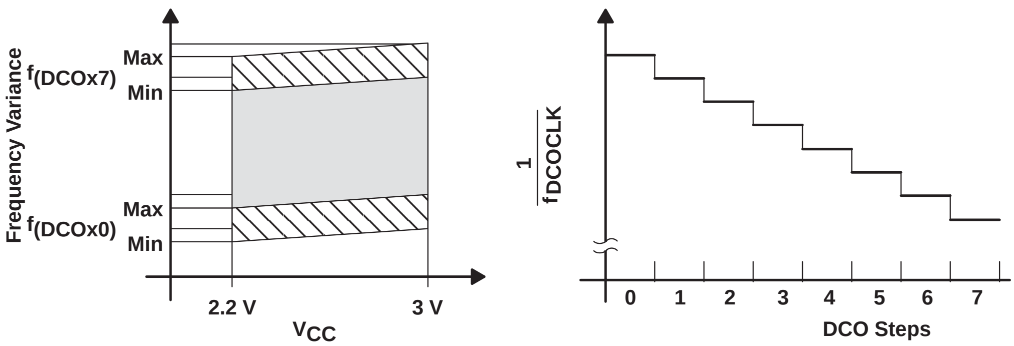


Figure 4. DCO Characteristics

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for $f_{(DCOx0)}$ to $f_{(DCOx7)}$ are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps Rsel1, ... Rsel6 overlaps Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often $f_{(DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{(DCO)} \times f_{(DCO+1)}}{MOD \times f_{(DCO)} + (32 - MOD) \times f_{(DCO+1)}}$$

crystal oscillator, LFXT1

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Input capacitance	XTS=0; LF mode selected. V_{CC} = 2.2 V / 3 V		12		pF
		XTS=1; XT1 mode selected. V_{CC} = 2.2 V / 3 V (Note 1)		2		
C_{XOUT}	Output capacitance	XTS=0; LF mode selected. V_{CC} = 2.2 V / 3 V		12		pF
		XTS=1; XT1 mode selected. V_{CC} = 2.2 V / 3 V (Note 1)		2		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 2)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	

NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Flash Memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.7		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.7 V/ 3.6 V		3	5	mA
t_{CPT}	Cumulative program time	see Note 1	2.7 V/ 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.7 V/ 3.6 V	200			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/$f_{FTG,max}$ = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG Interface

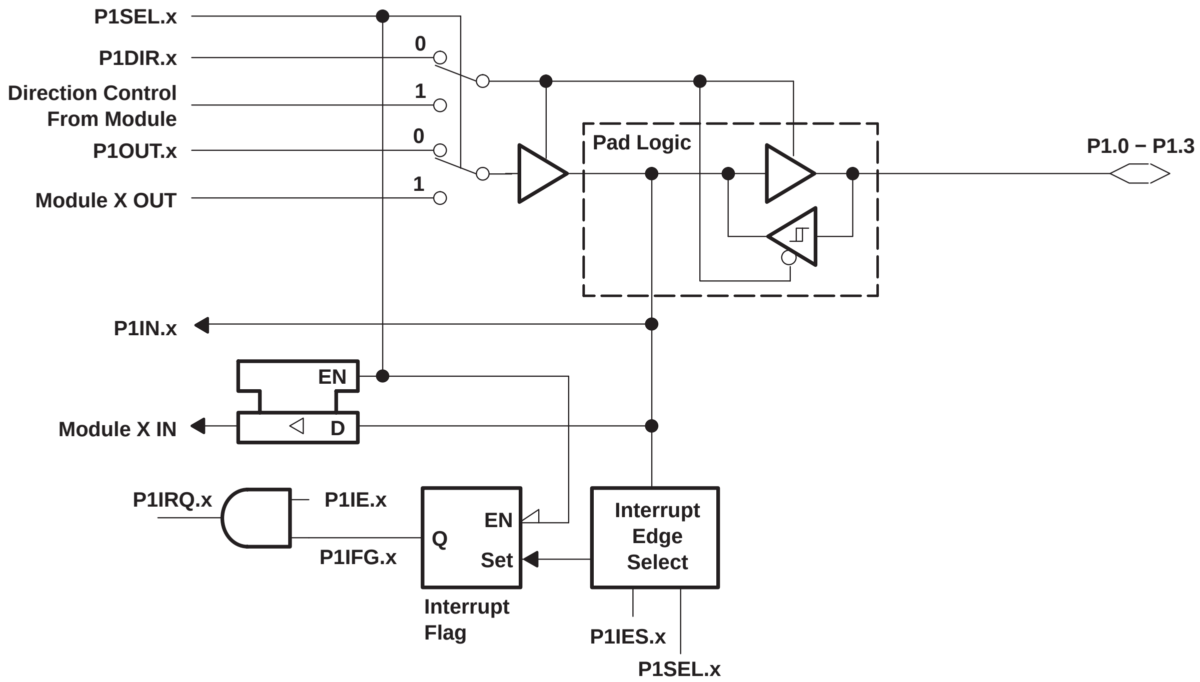
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.3, input/output with Schmitt-trigger



NOTE: x = Bit/identifier, 0 to 3 for port P1

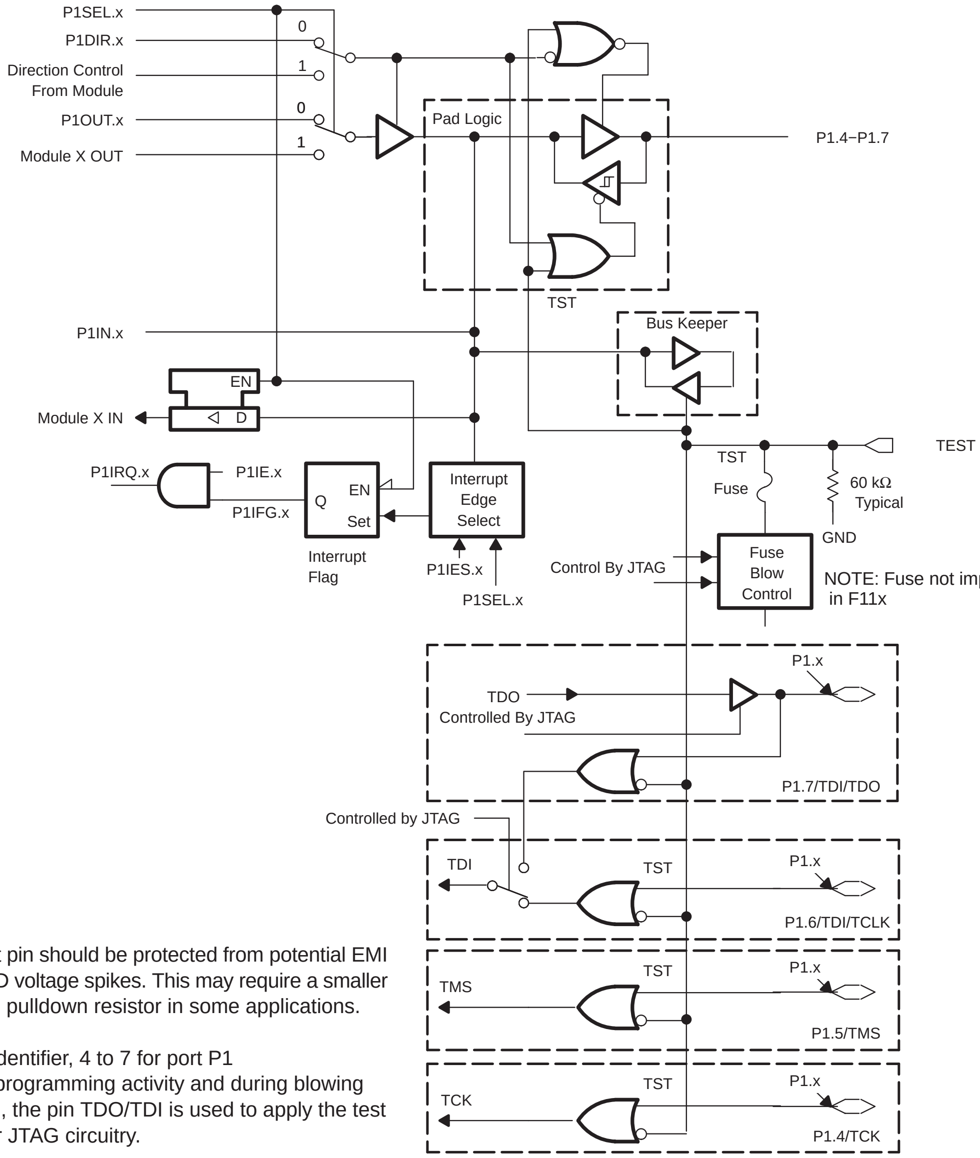
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	V_{SS}	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3

† Signal from or to Timer_A

APPLICATION INFORMATION

input/output schematic (continued)

Port P1, P1.4 to P1.7, input/output with Schmitt-trigger and in-system access features



NOTE: The test pin should be protected from potential EMI and ESD voltage spikes. This may require a smaller external pulldown resistor in some applications.

x = Bit identifier, 4 to 7 for port P1
During programming activity and during blowing the fuse, the pin TDO/TDI is used to apply the test input for JTAG circuitry.

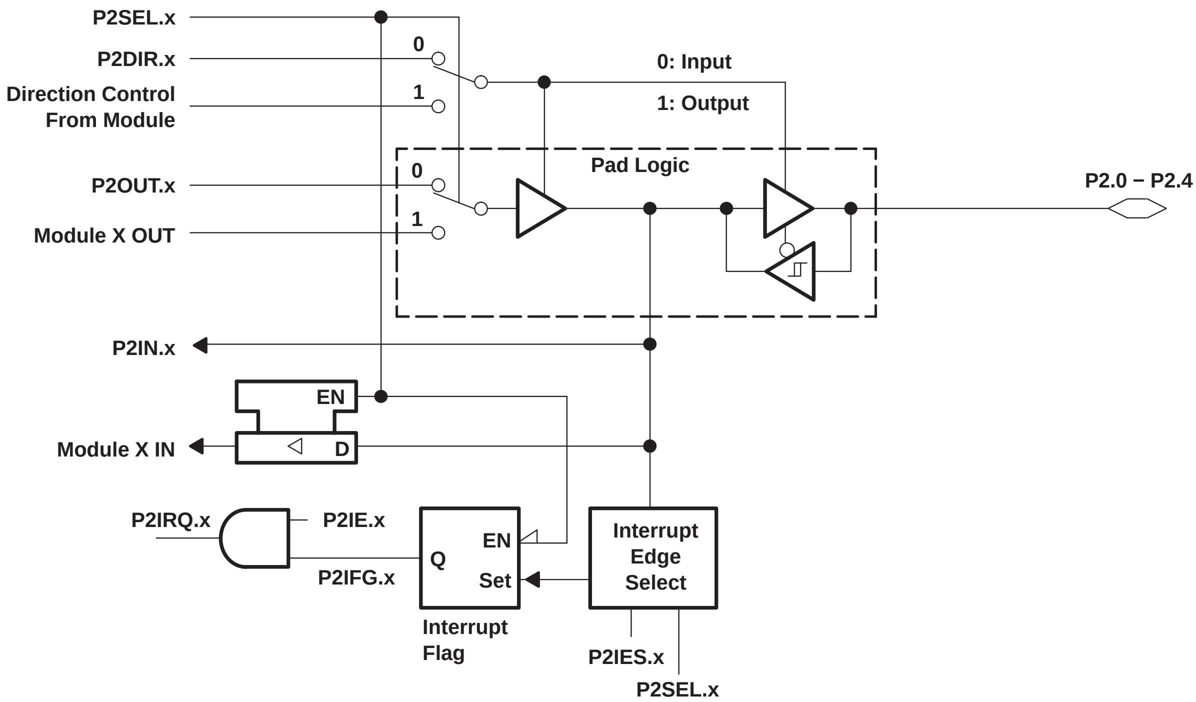
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

APPLICATION INFORMATION

input/output schematic (continued)

Port P2, P2.0 to P2.4, input/output with Schmitt-trigger



NOTE: x = Bit Identifier, 0 to 4 For Port P2

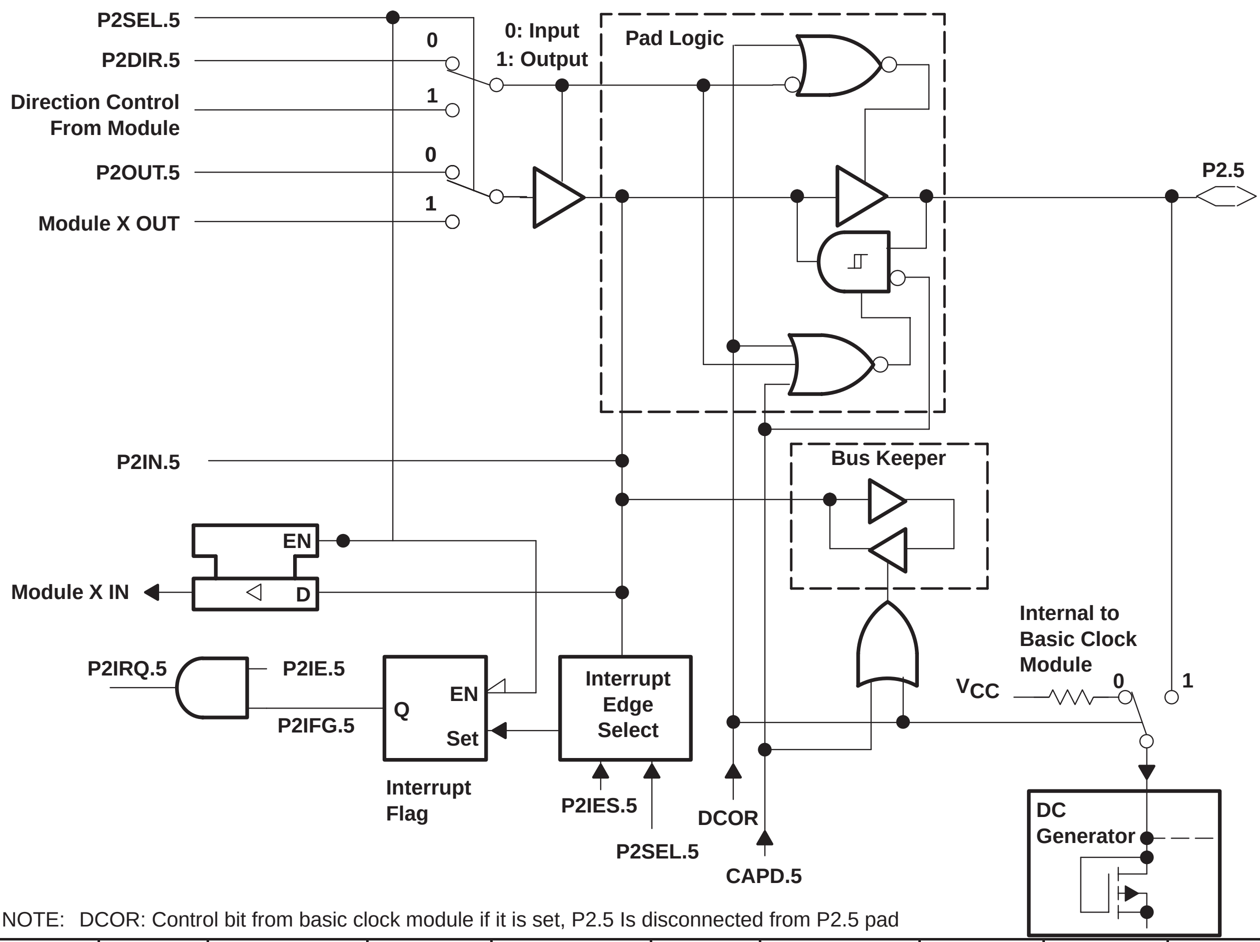
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P1IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	V_{SS}	P2IN.1	INCLK†	P2IE.1	P2IFG.1	P1IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	Out0 signal†	P2IN.2	CCI0B†	P2IE.2	P2IFG.2	P1IES.2
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	CCI1B†	P2IE.3	P2IFG.3	P1IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P1IES.4

† Signal from or to Timer_A

APPLICATION INFORMATION

input/output schematic (continued)

Port P2, P2.5, input/output with Schmitt-trigger and R_{OSC} function for the Basic Clock module



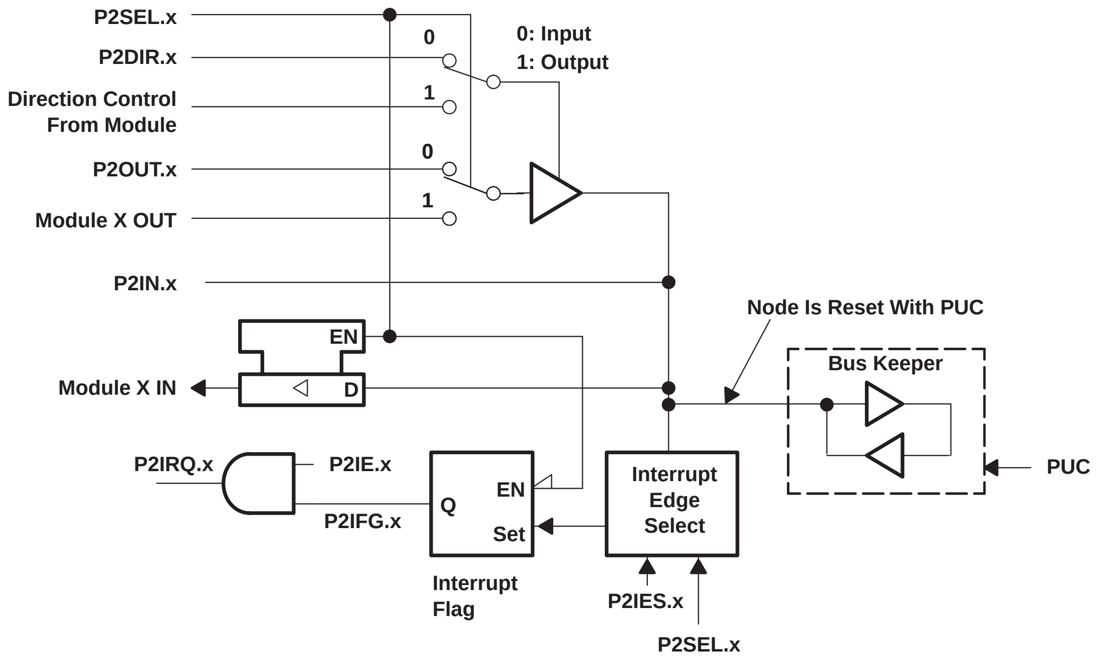
NOTE: DCOR: Control bit from basic clock module if it is set, P2.5 Is disconnected from P2.5 pad

PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	V_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

APPLICATION INFORMATION

input/output schematic (continued)

Port P2, unbonded bits P2.6 and P2.7



NOTE: x = Bit/identifier, 6 to 7 for port P2 without external pins

P2Sel.x	P2DIR.x	Direction control from module	P2OUT.x	Module X OUT	P2IN.x	Module X IN	P2IE.x	P2IFG.x	P2IES.x
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	V_{SS}	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	V_{SS}	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

NOTE: A good use of the unbonded bits 6 and 7 of port P2 is to use the interrupt flags. The interrupt flags can not be influenced from any signal other than from software. They work then as a soft interrupt.

APPLICATION INFORMATION

JTAG fuse check mode

The JTAG protection fuse is not implemented in the MSP430F11x devices.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F110AIDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		
MSP430F110AIDWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		
MSP430F110AIPW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
MSP430F110AIPWR	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
MSP430F110IDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		
MSP430F110IDWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	MSP430F110	
MSP430F110IPWR	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	430F110	
MSP430F112AIDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		
MSP430F112AIPW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
MSP430F112IDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		
MSP430F112IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MSP430F112	Samples
MSP430F112IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F112	Samples
MSP430F112IPWR	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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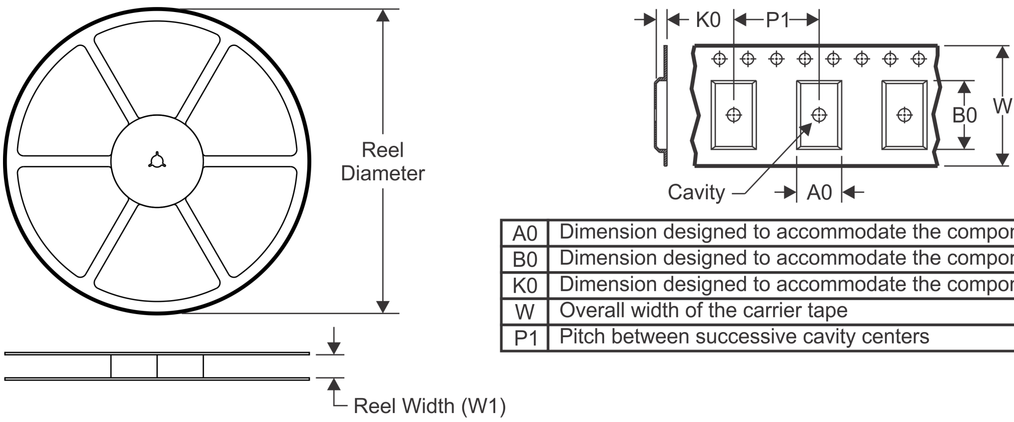
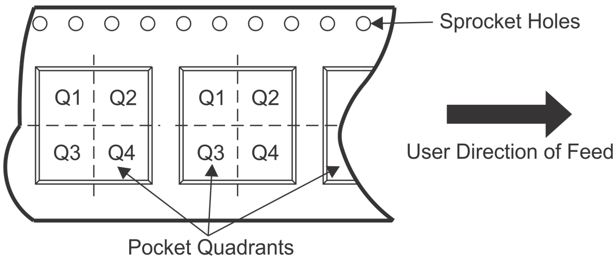
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

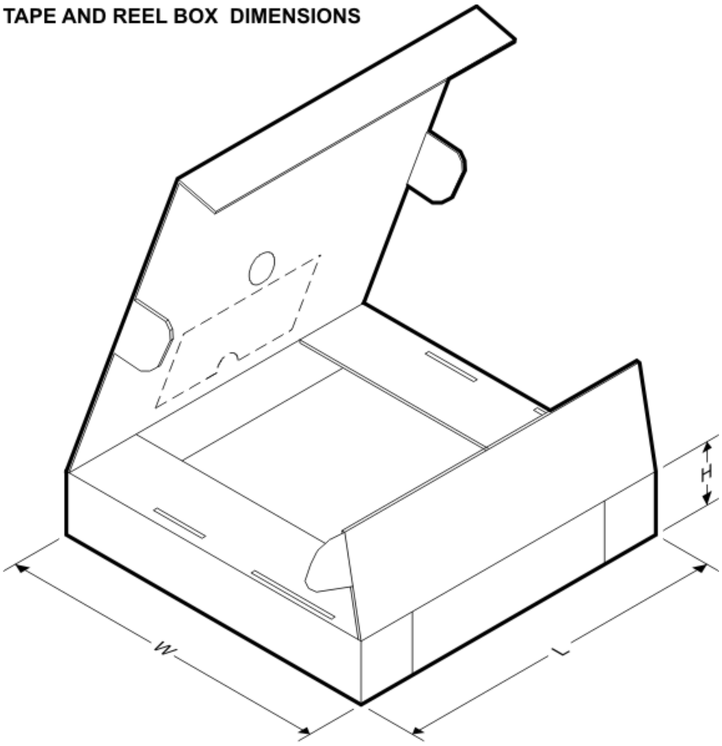
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F112IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

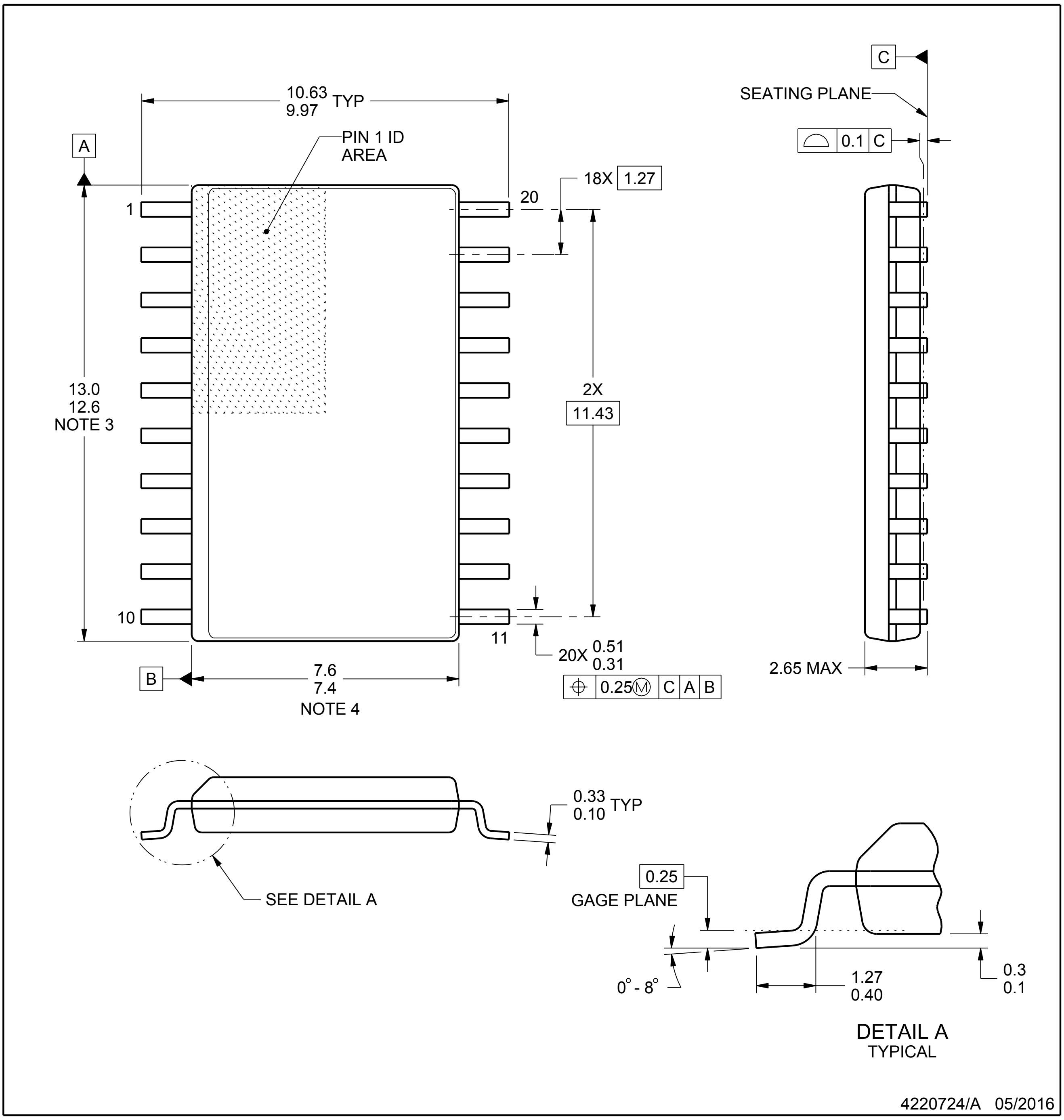
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F112IDWR	SOIC	DW	20	2000	367.0	367.0	45.0

PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



NOTES:

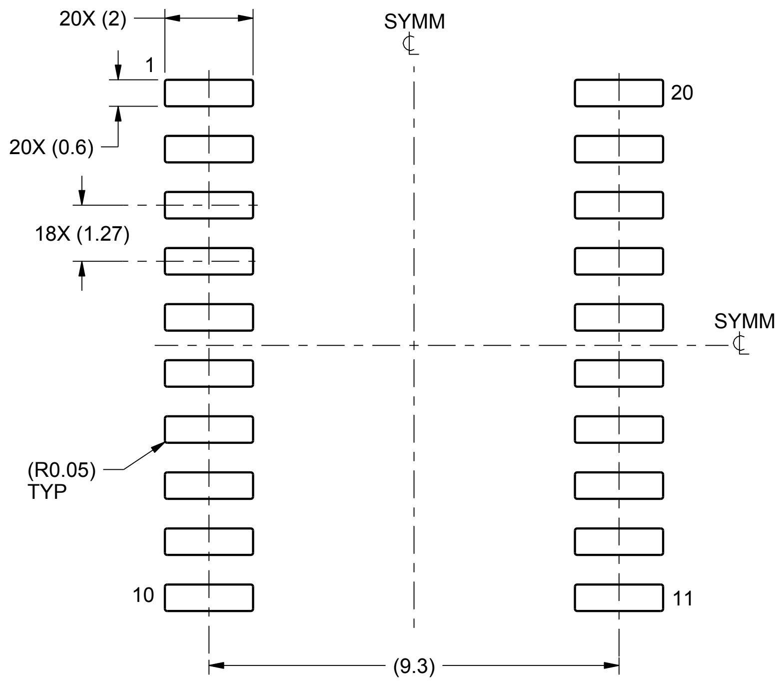
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

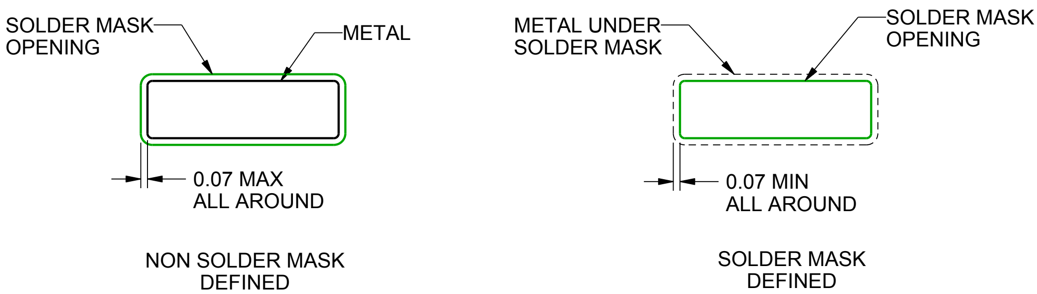
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

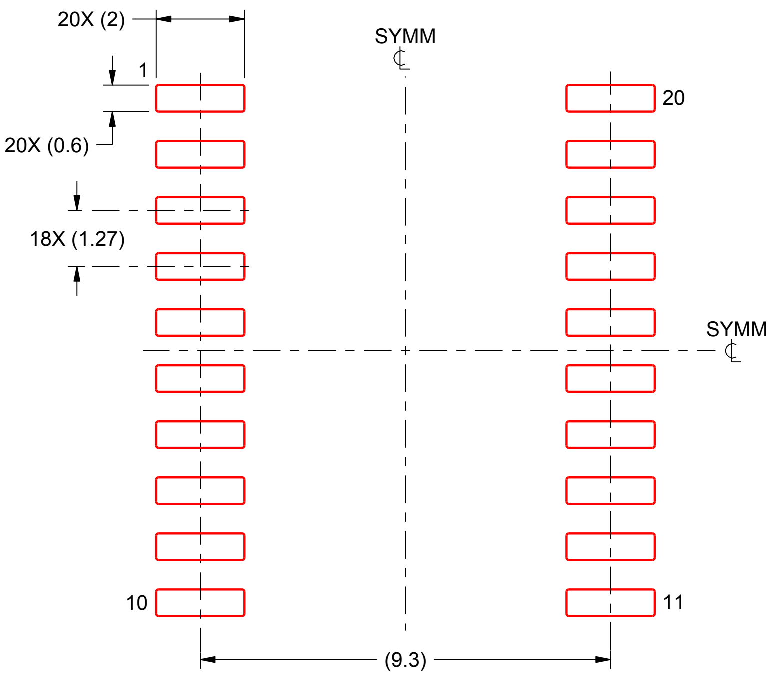
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



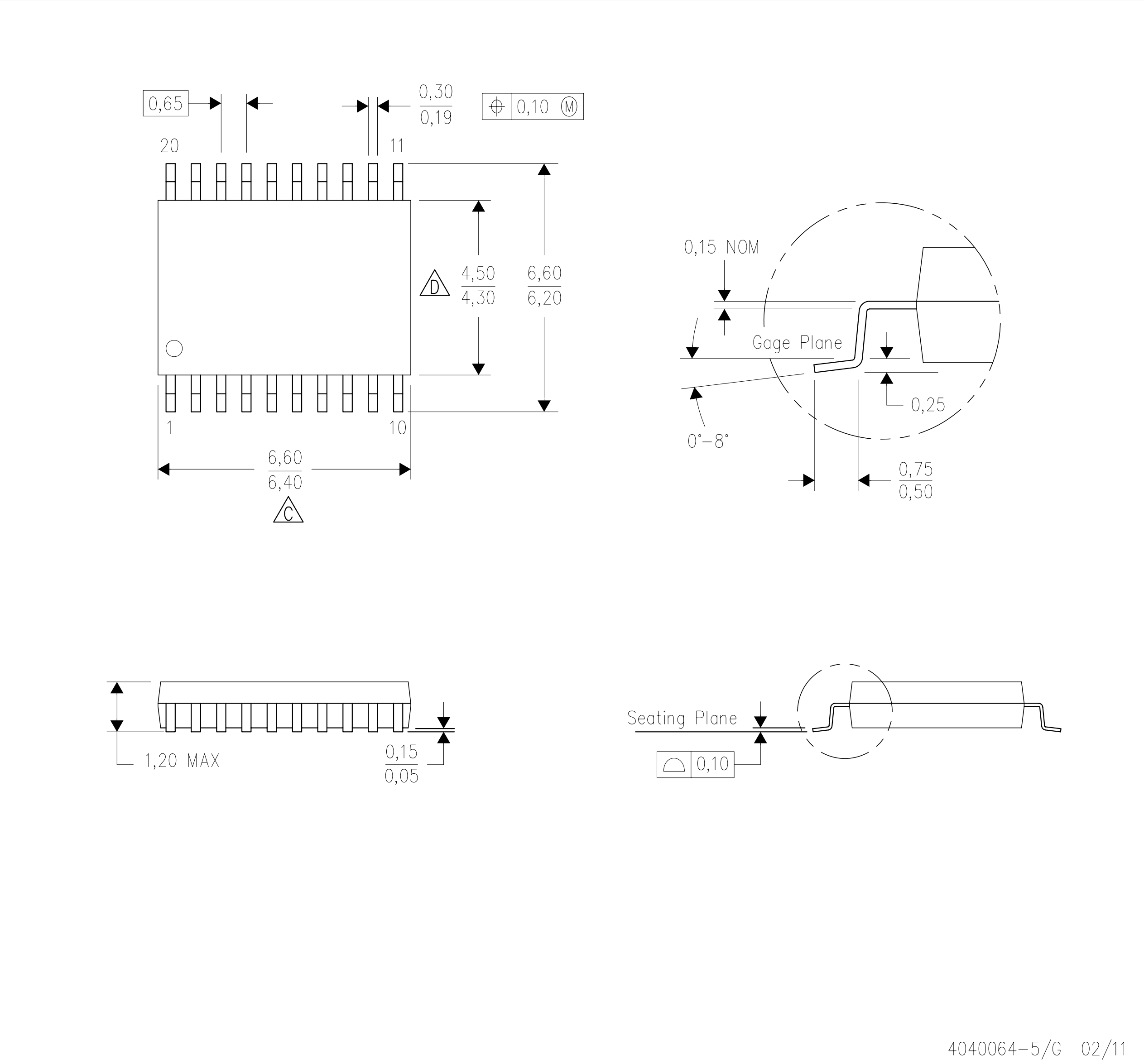
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

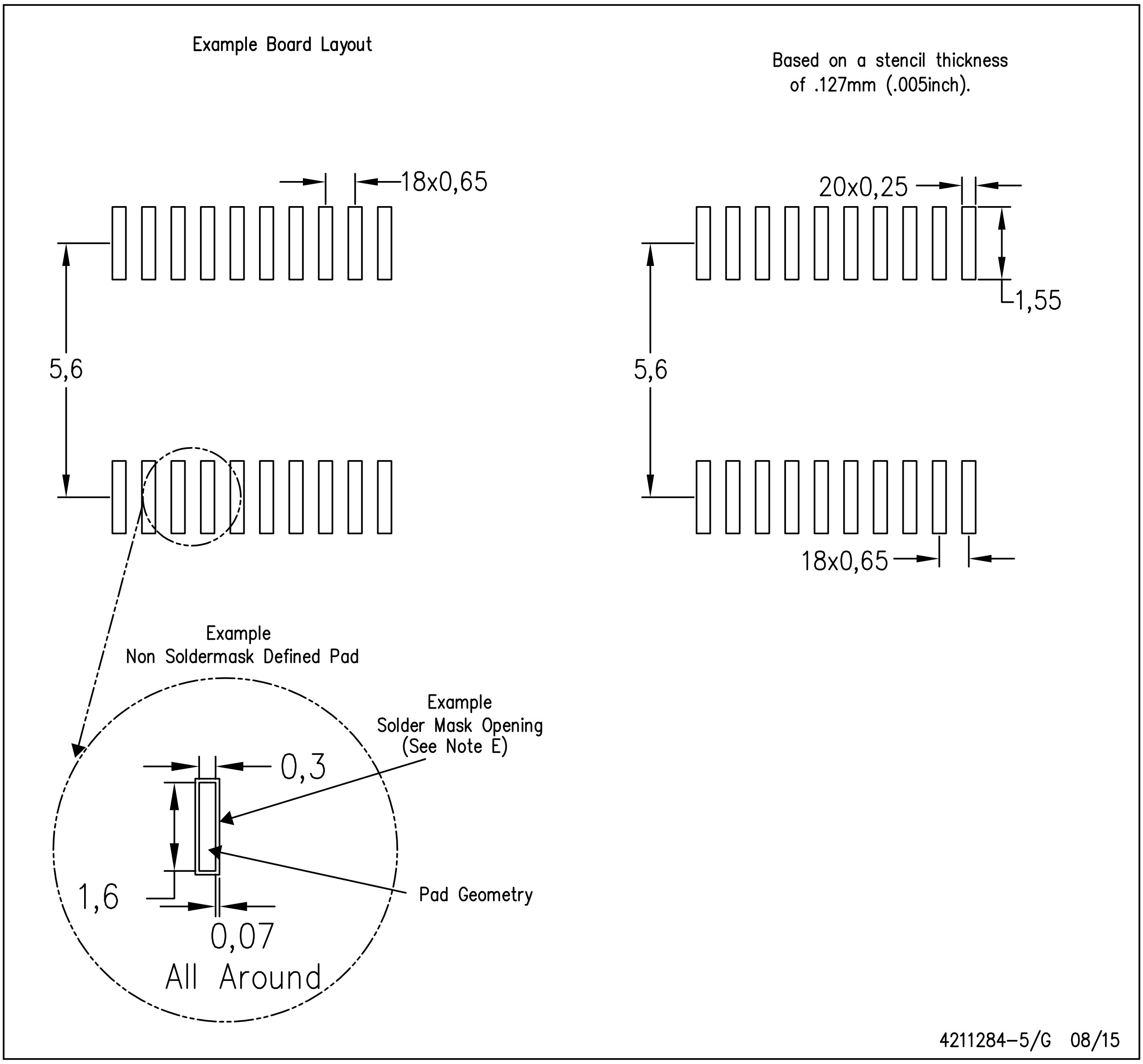
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

LAND PATTERN DATA

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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