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Texas Instruments
TPS56921PWP

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4.5V to 17V Input, 9A Synchronous Step Down SWIFT™ Converter With VID Control

Check for Samples: TPS56921

FEATURES

- **VID Control Range via I²C Compatible Interface: 0.72V to 1.48V in 10mV Steps**
- **I²C Addressing Flexibility: 2 Bits by IC pins**
- **±1.5% Output Voltage over Temperature for VID Control**
- **±1% Reference Voltage over Temperature for External Regulation Mode**
- **Integrated 26mΩ / 19mΩ MOSFETs**
- **Power Input PVIN Voltage Range: 1.6V to 17V**
- **Switching Frequency: 200kHz to 1.6MHz Internal Oscillator or Synchronizing to External Clock**
- **Shutdown Current: 2µA**
- **Monotonic Start-Up into Pre-biased Output Voltage**
- **Overcurrent Protection for Both MOSFETs with Hiccup Mode for Severe Fault Conditions**
- **Thermal and Overvoltage Protection**
- **Adjustable Soft Start**
- **Power Good Monitor for Under- and Over-Voltage Conditions**
- **Operating Junction Temperature Range: –40°C to 125°C**
- **Available in 20-Pin HTSSOP Package with PowerPAD™**

APPLICATIONS

- **Digital TVs**
- **Set Top Boxes**
- **SoC Power**
- **High Density Power Distribution Systems**

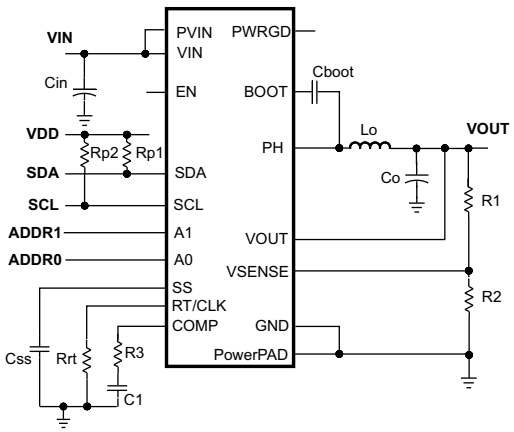
DESCRIPTION

The TPS56921 in thermally enhanced 20-pin HTSSOP package is a full featured 17V, 9A synchronous step down converter which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. After the initial power-up, the output voltage can be changed by codes sent to the IC via an I²C compatible VID Control bus. Current mode control provides space savings and easy compensation.

The output voltage startup ramp is controlled by the SS pin which helps to control startup inrush current. Power sequencing is supported by configuring the enable and the open drain power good pins. The output voltage is user-configurable at startup by external voltage divider.

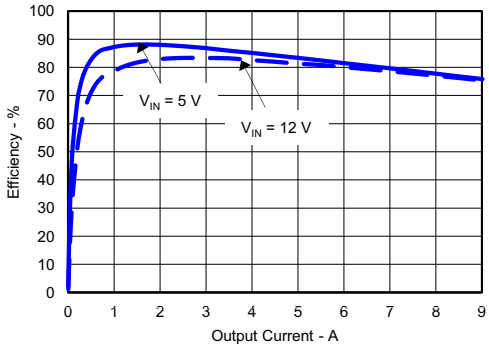
Cycle by cycle current limiting on the high-side fet protects the TPS56921 in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Hiccup protection will be triggered if the overcurrent condition has persisted for longer than the preset time. Thermal hiccup protection disables the part when die temperature exceeds thermal shutdown temperature and enables the part again after the built-in thermal hiccup time.

SIMPLIFIED SCHEMATIC



EFFICIENCY

Fsw = 500 kHz, V_{OUT}= 1.1 V



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_J	PACKAGE		PART NUMBER
–40°C to 125°C	20-Pin HTSSOP	Tube	TPS56921PWP
		Large Reel	TPS56921PWPR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)

		VALUE	UNIT
Input Voltage	VIN	–0.3 to 20	V
	PVIN	–0.3 to 20	
	EN	–0.3 to 6	
	BOOT	–0.3 to 27	
	VSENSE	–0.3 to 3	
	COMP	–0.3 to 3	
	PWRGD	–0.3 to 6	
	SS	–0.3 to 3	
	RT/CLK	–0.3 to 6	
	VOUT	–0.3 to 3.6	
	SDA	–0.3 to 3.6	
	SCL	–0.3 to 3.6	
	A0	–0.3 to 2.5	
	A1	–0.3 to 2.5	
Output Voltage	BOOT-PH	0 to 7.5	V
	PH	–1 to 20	
	PH 10ns Transient	–3 to 20	
Vdiff (GND to exposed thermal pad)		–0.2 to 0.2	V
Source Current	RT/CLK	±100	µA
	PH	Current Limit	A
Sink Current	PH	Current Limit	A
	PVIN	Current Limit	A
	COMP	±200	µA
	PWRGD	–0.1 to 5	mA
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)		2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)		500	V
Operating Junction Temperature		–40 to 125	°C
Storage Temperature		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS56921 HTSSOP (20 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	39.4	°C/W
θ_{JA}	Junction-to-ambient thermal resistance(3)	26	
θ_{JCtop}	Junction-to-case (top) thermal resistance	26.5	
θ_{JB}	Junction-to-board thermal resistance	23.1	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	22.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.1	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See power dissipation estimate in application section of this data sheet for more information.
(3) Test board conditions:
(a) 3 inches × 3 inches, 4 layers, thickness: 0.062 inch
(b) 2 oz. copper traces located on the top of the PCB
(c) 2 oz. copper ground planes on the 2 internal layers and bottom layer of the PCB
(d) 21 thermal vias located under the device package and 9 of them located under the device exposed thermal pad

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, VIN = 4.5V to 17V, PVIN = 1.6V to 17V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN AND PVIN PINS)					
PVIN operating input voltage		1.6		17	V
VIN operating input voltage		4.5		17	V
VIN internal UVLO threshold	VIN rising		4.0	4.5	V
VIN internal UVLO hysteresis			150		mV
VIN shutdown supply Current	EN = 0 V		2	7	µA
VIN operating – non switching supply current	VSENSE = 810 mV		770	1000	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.21	1.26	V
Enable threshold	Falling	1.10	1.17		
Input current	EN = 1.1 V		1.15		µA
Hysteresis current	EN = 1.3 V		3.3		µA
OUTPUT VOLTAGE					
Voltage reference	0 A ≤ I_{OUT} ≤ 9 A Voltage at VSENSE pin in regulation before first I^2C write	0.792	0.	0.808	V
Output Voltage	Relative to ideal VOUT after first I^2C write; (shown in Ideal VOUT vs. Code table)	Ideal VOUT –1.5%	Ideal VOUT	Ideal VOUT +1.5%	V
MOSFET					
High-side switch resistance(1)	BOOT-PH = 3 V		30	60	mΩ
High-side switch resistance(1)	BOOT-PH = 6 V		26	40	mΩ
Low-side Switch Resistance(1)			19	30	mΩ
ERROR AMPLIFIER					
Error amplifier Transconductance (gm)	–2 µA < I_{COMP} < 2 µA, $V_{(COMP)}$ = 1 V		1300		µMhos
Error amplifier dc gain (production test)	VSENSE = 0.8 V	1000	3000		V/V

(1) Measured at pins

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, VIN = 4.5V to 17V, PVIN = 1.6V to 17V (unless otherwise noted)

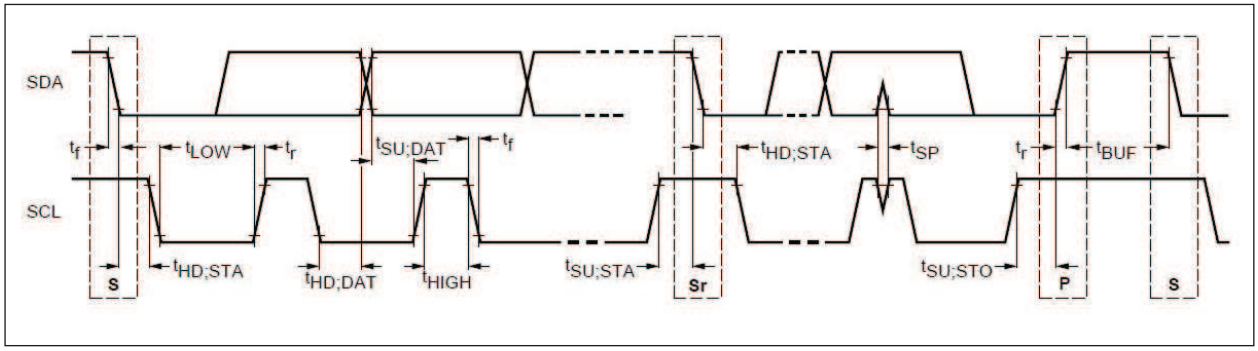
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV input overdrive		±110		µA
Start Switching Threshold			0.25		V
COMP to Iswitch gm			24		A/V
CURRENT LIMIT					
High-side switch current limit threshold		11.5	17.5	22	A
Low-side switch sourcing current limit		10	15.5	21	A
Low-side switch sinking current limit		2.5	4.5	6.5	A
Hiccup wait time			512		Cycles
Hiccup time before re-start			16384		Cycles
THERMAL SHUTDOWN					
Thermal shutdown		150	170		°C
Thermal shutdown hysteresis			10		°C
Thermal shutdown hiccup time			32768		Cycles
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Maximum operating switching frequency	R(RT/CLK) = 240 kΩ (1%)	160	200	240	kHz
Minimum operating switching frequency	R(RT/CLK) = 100 kΩ (1%)	400	480	560	kHz
Switching frequency	R(RT/CLK) = 29kΩ (1%	1440	1600	1760	kHz
Minimum pulse width			20		ns
RT/CLK high threshold				2	V
RT/CLK low threshold		0.78			V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		66		ns
PLL frequency range		200		1600	kHz
PH (PH PIN)					
Minimum on time	Measured at 90% to 90% of VIN, 25°C, I_{PH} = 2A		94	150	ns
Minimum off time	BOOT-PH ≥ 3 V		0		%
BOOT (BOOT PIN)					
BOOT-PH UVLO			2.1	3	V
SLOW START (SS PIN)					
SS charge current			2.3		µA
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		92		% Vreg
VSENSE rising (Good)			94		% Vreg
VSENSE rising (Fault)			106		% Vreg
VSENSE falling (Good)			104		% Vreg
Output high leakage	VSENSE = Vref, $V_{(PWRGD)}$ = 5.5 V		30	100	nA
Output low	$I_{(PWRGD)}$ = 2 mA			0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5V at 100 µA		0.6	1	V
Minimum SS voltage for PWRGD				1.4	V
VOUT (VOUT PIN)					
Output voltage VID control minimum			0.72		V
Output voltage VID control maximum			1.48		V
Output voltage step			10		mV

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, VIN = 4.5V to 17V, PVIN = 1.6V to 17V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL INTERFACE (SDA AND SCL PINS) (2) (3)					
LOW level input voltage, V_{IL}				0.9	V
HIGH level input voltage, V_{IH}		2.5			V
Hysteresis of schmitt trigger inputs, V_{hys}		0.16			V
LOW level SDA output voltage (Open drain, 3mA sink current), V_{OL1}				0.4	V
Pulse width of spikes suppressed by input filter, t_{SP}		50			ns
SCL clock frequency, f_{scl}				400	kHz
Hold time (repeated) START condition, $t_{HD;STA}$		0.6			µs
LOW period of SCL clock, t_{LOW}		1.3			µs
HIGH period of SCL clock, t_{HIGH}		0.6			µs
Set-up time for a repeated START condition, $t_{SU;STA}$		0.6			µs
Data hold time, $t_{HD;DAT}$		50		900	ns
Data set-up time, $t_{SU;DAT}$		100			ns
Rise time (SDA or SCL), t_r		20+0.1Cb (4)		300	ns
Fall time (SDA or SCL), t_f		20+0.1Cb (4)		300	ns
Set-up time for STOP condition, $t_{SU;STO}$		0.6			µs
Bus free time between STOP and START condition, t_{BUF}		1.3			µs
Capacitive load for each bus line, C_b				400	pF

(2) Refer to the I²C Timing diagram below for I²C Timing Definitions
(3) Specified by design. Not tested in production.
(4) Cb = capacitance of bus line in pF

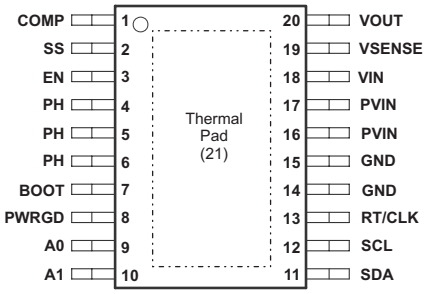


I²C Timing Definitions (Reproduced from Philips I²C specification Version 1.1)

DEVICE INFORMATION

PIN ASSIGNMENTS

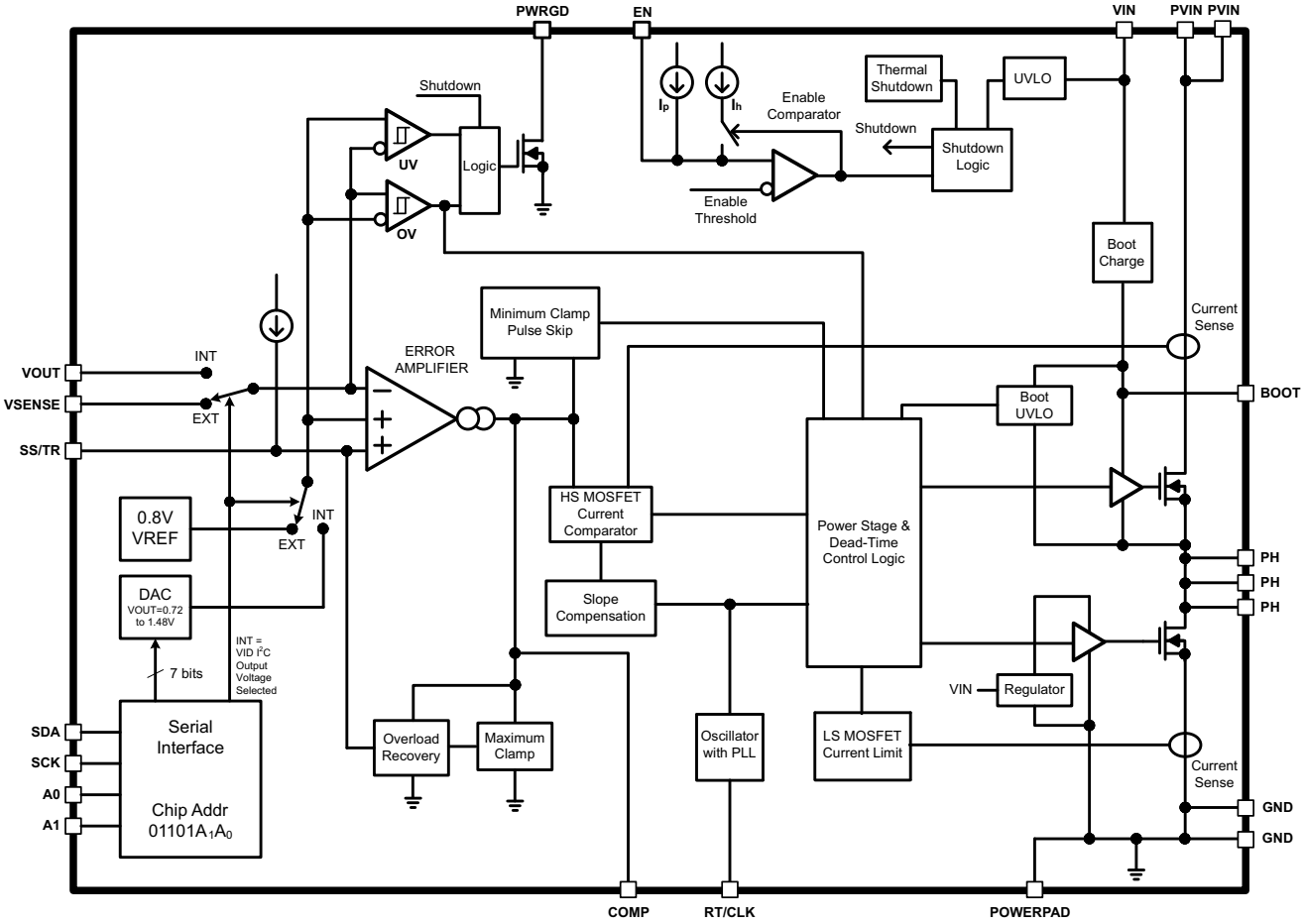
PWP PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NUMBER	
COMP	1	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
SS	2	An external capacitor connected to this pin sets the internal voltage reference rise time.
EN	3	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
PH	4, 5, 6	The switch node.
BOOT	7	A bootstrap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
PWRGD	8	Power Good fault pin. Asserts low if output is low due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.
A0	9	LSB of chip address. Tie to GND for 0, leave floating for 1.
A1	10	LSB+1 of chip address. Tie to GND for 0, leave floating for 1.
SDA	11	Data I/O pin
SCL	12	Clock I/O pin.
RT/CLK	13	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device; In CLK mode, the device synchronizes to an external clock.
GND	14, 15	Return for control circuitry and low side power MOSFET.
PVIN	16, 17	Power input. Supplies the power switches of the power converter.
VIN	18	Supplies the control circuitry of the power converter.
VSENSE	19	Inverting node of the gm error amplifier input.
VOUT	20	Output voltage controlled by VID
Exposed Thermal Pad	21	Must be connected to GND and soldered down for proper electrical and thermal operation.

FUNCTIONAL BLOCK DIAGRAM



EXT – External Regulation Mode INT- Internal Regulation Mode

TYPICAL CHARACTERISTICS

CHARACTERISTIC CURVES

HIGH-SIDE MOSFET ON RESISTANCE vs JUNCTION TEMPERATURE

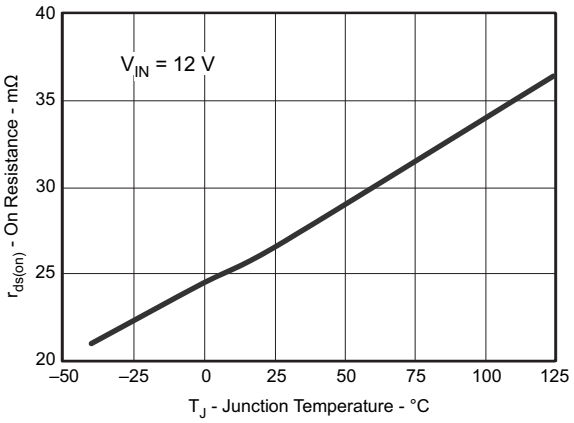


Figure 1.

LOW-SIDE MOSFET ON RESISTANCE vs JUNCTION TEMPERATURE

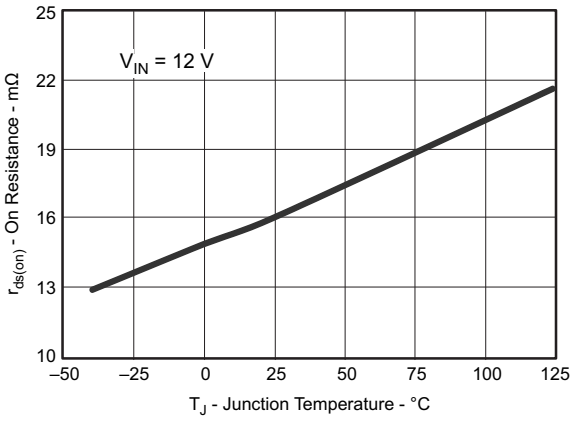


Figure 2.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

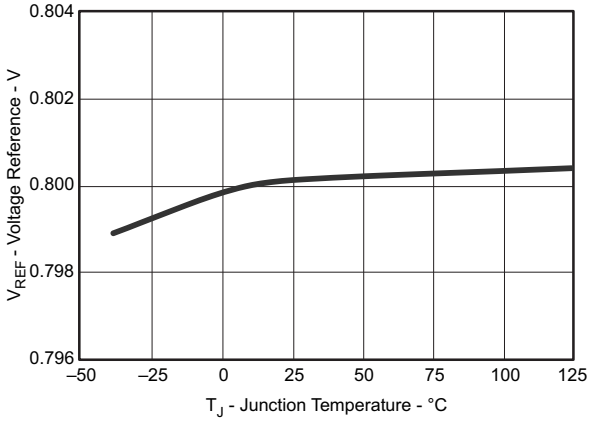


Figure 3.

OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

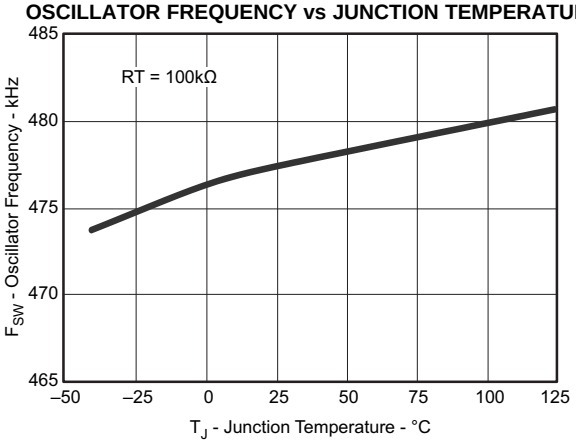


Figure 4.

SHUTDOWN QUIESCENT CURRENT vs INPUT VOLTAGE

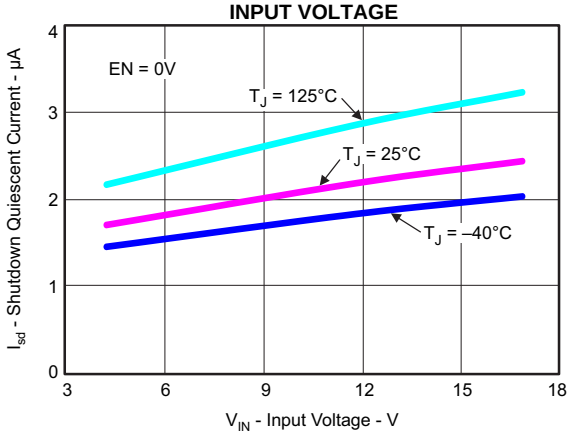


Figure 5.

EN PIN HYSTERESIS CURRENT vs JUNCTION TEMPERATURE

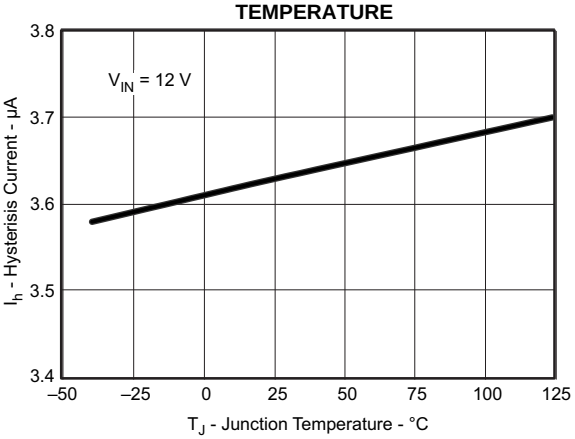


Figure 6.

TYPICAL CHARACTERISTICS (continued)

EN PIN PULLUP CURRENT vs JUNCTION TEMPERATURE

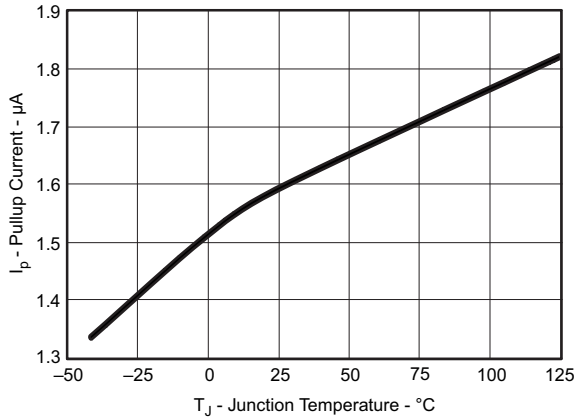


Figure 7.

EN PIN UVLO THRESHOLD vs JUNCTION TEMPERATURE

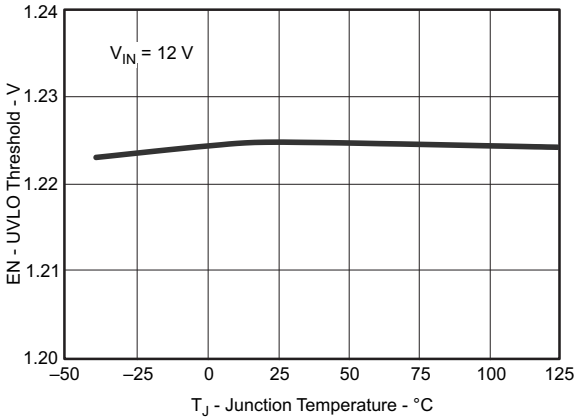


Figure 8.

V_{IN} NON-SWITCHING OPERATING QUIESCENT CURRENT vs INPUT VOLTAGE

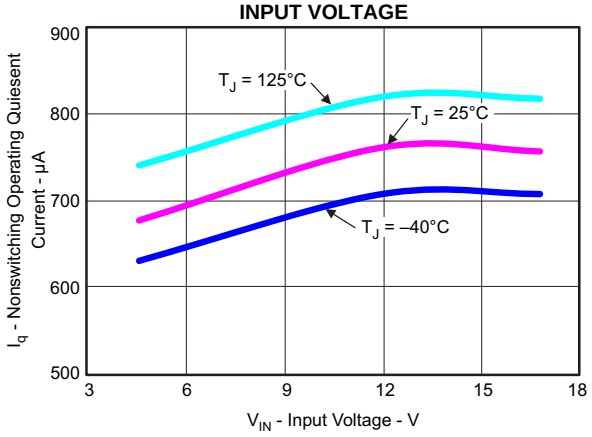


Figure 9.

SLOW START CHARGE CURRENT vs JUNCTION TEMPERATURE

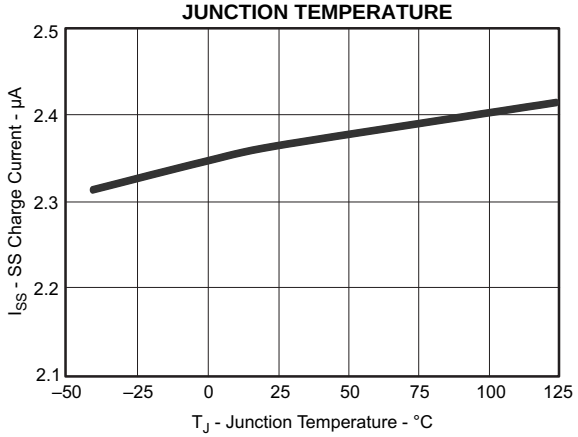


Figure 10.

PWRGD THRESHOLD vs JUNCTION TEMPERATURE

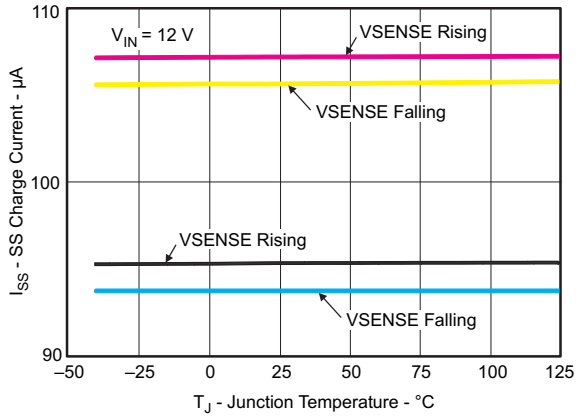


Figure 11.

HIGH-SIDE CURRENT LIMIT THRESHOLD vs INPUT VOLTAGE

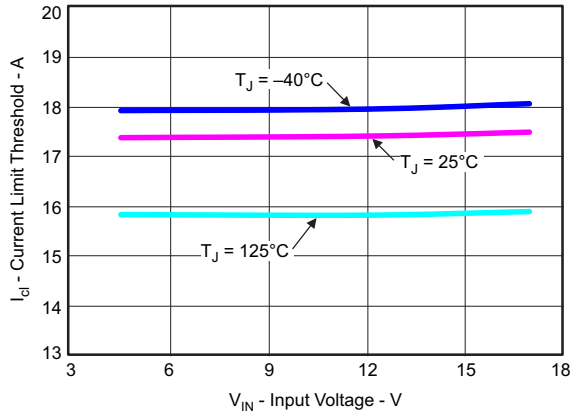


Figure 12.

TYPICAL CHARACTERISTICS (continued)

MINIMUM CONTROLLABLE ON TIME vs JUNCTION TEMPERATURE

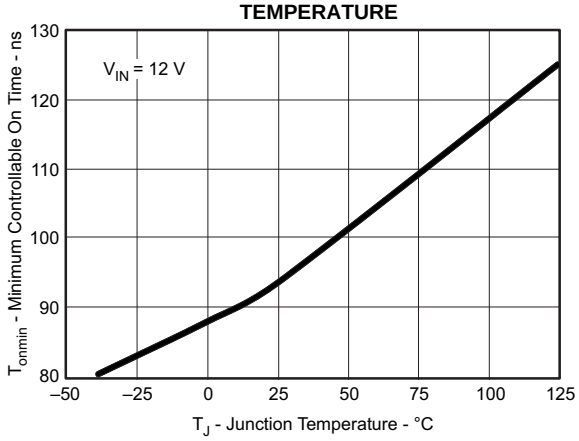


Figure 13.

MINIMUM CONTROLLABLE DUTY RATIO vs JUNCTION TEMPERATURE

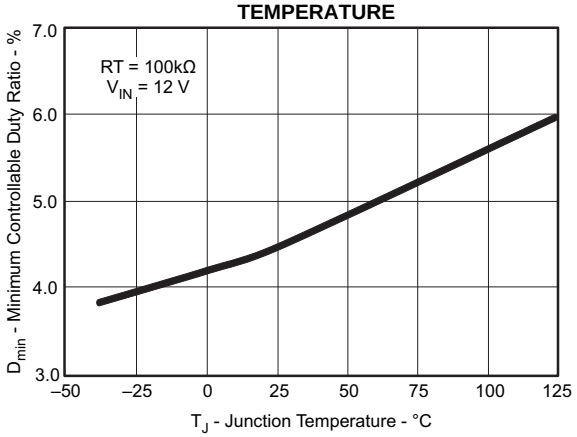


Figure 14.

BOOT-PH UVLO THRESHOLD vs JUNCTION TEMPERATURE

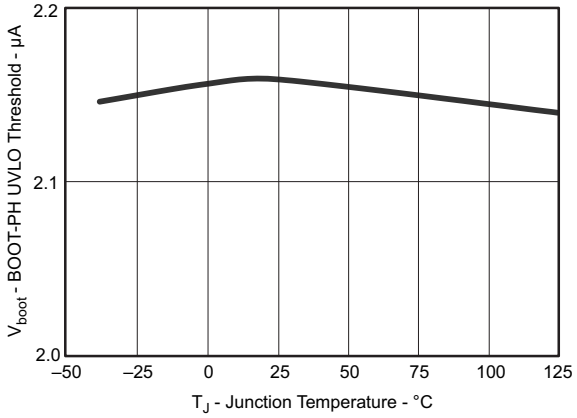


Figure 15.

OVERVIEW

The TPS56921 is a 17-V, 9-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the TPS56921 implements a fixed frequency, peak current mode control which also simplifies external frequency compensation. The output voltage of the TPS56921 can be set by either VSENSE with divider resistors (Adjusting the Output Voltage by External Regulation Mode) or I^2C compatible interface (Programming the Output Voltage by Internal Regulation Mode) to as low as the 0.8V reference voltage in external regulation mode or 0.72V in internal regulation mode. It operates in CCM (Continuous current mode) at any load conditions unless the COMP pin voltage drops below the COMP pin start switching threshold (typically 0.25V).

The wide switching frequency of 200 kHz to 1600 kHz allows for efficiency and size optimization when selecting the output filter components. The RT/CLK pin is dual-functional with two modes. In RT mode, the switching frequency is adjusted using a resistor to ground on the RT/CLK pin. In CLK mode, the TPS56921 can be controlled by the RT/CLK pin to synchronize the switching cycle to the falling edge of an external system clock.

The TPS56921 has been designed for safe startup into pre-biased outputs. The default start up is when VIN is typically 4.0V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under-voltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the TPS56921 to operate with the internal pull up current. The total operating current for the TPS56921 is approximately 770µA when not switching and under no load. When the TPS56921 is disabled, the supply current is typically less than 2µA.

The integrated MOSFETs allow for high efficiency power supply designs with continuous output currents up to 9 amperes. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The TPS56921 reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The bootstrap voltage is monitored by a BOOT to PH UVLO (BOOT-PH UVLO) circuit allowing PH pin to be pulled low to recharge the boot capacitor. The TPS56921 can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold which is typically 2.1V.

The TPS56921 has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open drain MOSFET which is pulled low when the VSENSE pin voltage is less than 92% or greater than 106% of the internal reference voltage and asserts high when it is 94% to 104% of the internal reference voltage.

The slow start (SS) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for slow start or critical power supply sequencing requirements.

The TPS56921 is protected from output overvoltage, overcurrent and overheat conditions. The TPS56921 minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 104% of the Vref. The TPS56921 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. If the overcurrent condition has lasted for more than the hiccup wait time, the TPS56921 will shut down and re-start after the hiccup time. The TPS56921 also shuts down if the junction temperature is higher than thermal shutdown trip point. When the junction temperature drops 10°C typically below the thermal shutdown trip point, the built-in thermal shutdown hiccup timer is triggered. The TPS56921 will be restarted under control of the slow start circuit automatically after the thermal shutdown hiccup time is over.

Furthermore, if the overcurrent condition has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the TPS56921 will shut down itself and re-start after the hiccup time which is set for 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

DETAILED DESCRIPTION

Fixed Frequency PWM Control

The device uses a adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches current reference generated by the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on.

Continuous Current Mode Operation (CCM)

As a synchronous buck converter, the device normally works in CCM (Continuous Conduction Mode) under load all conditions.

VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system.

If tied together, the input voltage for VIN and PVIN can range from 4.5V to 17V. If using the VIN separately from PVIN, the VIN pin must be between 4.5V and 17V, and the PVIN pin can range from as low as 1.6V to 17V. A voltage divider connected to the EN pin can adjust the either input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power up behavior.

Setting the Output Voltage

The output voltage can be set via Adjusting the Output Voltage by External Regulation Mode or Programming the Output Voltage by Internal Regulation Mode. In the external regulation mode, the output voltage is determined by the output voltage resistor divider and it can never be lower than the internal voltage reference of 0.8 V. In the internal regulation mode, the output voltage is controlled by I^2C compatible interface via SDA, SCL, A0 and A1 pins between 0.72V and 1.48V.

The device always starts up into external regulation mode. The first I^2C write will not be taken until the VSENSE pin achieves regulation at the conclusion of soft start. Use Equation 1 to calculation the nominal time between the device start and the conclusion of soft start where Css is the slow start capacitor and the slow start charge current (Iss) is 2.3µA.

$$t_{WAIT}\ (ms) = \frac{C_{SS}\ (nF) \times 1.2\ (V)}{I_{SS}\ (\mu A)} \quad (1)$$

The device stays in external regulation mode until the first successful I^2C write excluding the special control codes listed in Table 4, then the device switches to internal regulation mode.

If the serial interface is to be used, the VOUT pin should be connected to the output of the converter and the output voltage at VOUT pin overrides the output voltage resistor divider setting. In this configuration, the output of the converter can not go above 3.3V.

If the serial interface will not be used, the VOUT pin should be floating and the output of the converter can be set greater than 3.3V by the output voltage resistor divider.

Adjusting the Output Voltage by External Regulation Mode

The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Referring to the application schematic of Figure 25, start with a 10 kΩ for R10 and use Equation 25 to calculate R11. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

The minimum output voltage and maximum output voltage can be limited by the minimum on time of the high-side MOSFET and bootstrap voltage (BOOT-PH voltage) respectively. More discussions are located in Minimum On Time and Maximum Switching Frequency Limitations and Bootstrap Voltage (BOOT) and Low Dropout Operation.

Minimum On Time and Maximum Switching Frequency Limitations

The current-mode architecture of the device requires a settling time before accurate current measurements can occur, therefore a minimum on-time spec exists. The output voltage may be limited by the minimum controllable on time depending on the input voltage, load current and switching frequency, and so on. The minimum output voltage is given by Equation 2.

$$Voutmin = Ontimemin \bullet Fsmax \left(Vinmax + Ioutmin(Rds,ls - Rds,hs)\right) - Ioutmin(RL + Rds,ls) \quad (2)$$

Where:

Voutmin = minimum achievable output voltage

Ontimemin = minimum controllable on-time (150 nsec maximum @ 2A load current)

Fsmax = maximum switching frequency including tolerance

Vinmax = maximum input voltage

Ioutmin = minimum load current

Rds,hs = high side MOSFET on resistance (26 mΩ typical)

Rds,ls = low side MOSFET on resistance (19 mΩ typical)

RL = series resistance of output inductor

If the minimum on-time limitation is exceeded, the device may begin pulse-skipping. In this case, the device will act as if the operational switching frequency has dropped, but in reality it may probably only skip a few cycles. Though this will increase the output ripple, the output of the converter will remain in regulation. It is up to the user to determine whether to choose a switching frequency that keeps the operation away from the pulse-skipping regime of operation or to run at a reduced input voltage to keep the operation away from pulse-skipping mode or to run a higher frequency that may pulse-skip if the duty ratio becomes too low.

Safe Start-up into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to sink current until the SS pin voltage is higher than 1.4V.

Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS pin voltage or the internal 0.8V voltage reference. The transconductance of the error amplifier is 1300 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

Enable and Adjusting Under-Voltage Lockout (EN and UVLO)

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150mV.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN, in split rail applications, then the EN pin can be configured as shown in Figure 16, Figure 17 and Figure 18. When using the external UVLO function it is recommended to set the hysteresis to be greater than 500mV.

The EN pin has a small pull-up current Ip which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by I_h once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 3 and Equation 4.

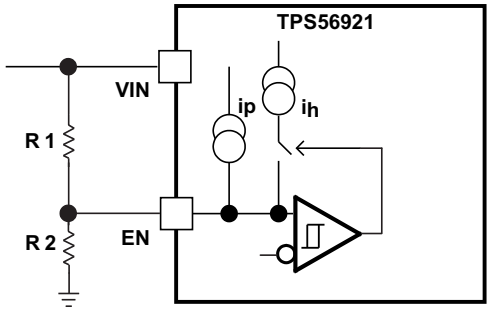


Figure 16. Adjustable VIN Under Voltage Lock Out

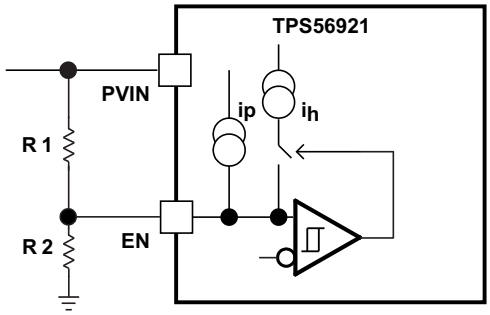


Figure 17. Adjustable PVIN Under Voltage Lock Out, VIN ≥ 4.5V

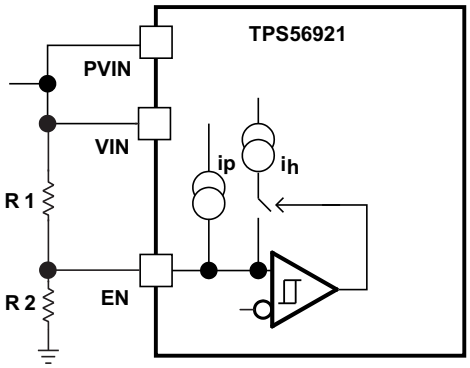


Figure 18. Adjustable VIN and PVIN Under Voltage Lock Out

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (3)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (4)$$

Where I_h = 3.3 µA, I_p = 1.15 µA, $V_{ENRISING}$ = 1.21 V, $V_{ENFALLING}$ = 1.17 V

Setting Switching Frequency and Synchronization (RT/CLK)

The RT/CLK pin can be used to set the switching frequency of the device in two modes.

In RT mode, a resistor (RT resistor) is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1600 kHz by placing a maximum of 240 kΩ and minimum of 29 kΩ respectively. In CLK mode, an external clock is connected directly to the RT/CLK pin. The device is synchronized to the external clock frequency with PLL.

The CLK mode overrides the RT mode. The device is able to detect the proper mode automatically and switch from the RT mode to CLK mode.

Adjustable Switching Frequency (RT Mode)

To determine the RT resistance for a given switching frequency, use Equation 5 or the curve in Figure 19. To reduce the solution size one would set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time should be considered.

$$Rrt(k\Omega) = 48000 \cdot Fsw\,(kHz)^{-0.997} - 2 \quad (5)$$

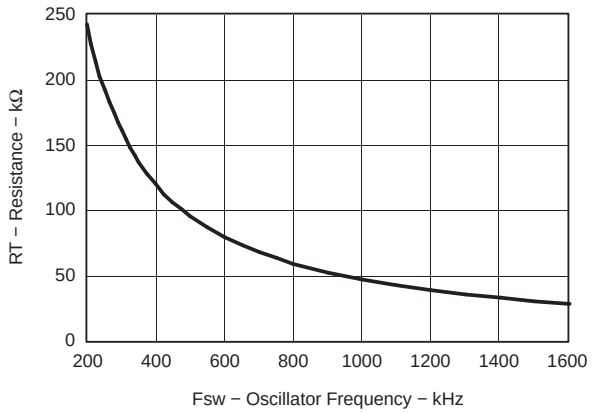


Figure 19. RT Set Resistor vs Switching Frequency

Synchronization (CLK mode)

An internal Phase Locked Loop (PLL) has been implemented to allow synchronization between 200kHz and 1600kHz, and to easily switch from RT mode to CLK mode.

To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.78V and higher than 2.0V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin.

In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 20. Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the SYNC pin is pulled above the RT/CLK high threshold (2.0V), the device switches from the RT mode to the CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from the CLK mode back to the RT mode because the internal switching frequency drops to 100kHz first before returning to the switching frequency set by RT resistor.

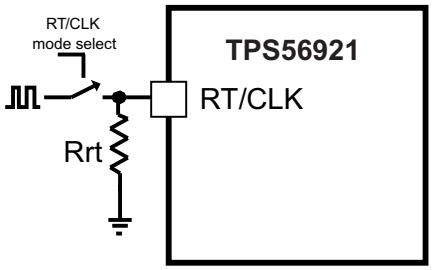


Figure 20. Works with Both RT mode and CLK mode

Slow Start (SS)

The device uses the lower voltage of the internal voltage reference or the SS pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS pin to ground implements a slow start time. The device has an internal pull-up current source of 2.3µA that charges the external slow start capacitor. The calculations for the slow start time (Tss, 10% to 90%) and slow start capacitor (Css) are shown in Equation 6. The voltage reference (Vref) is 0.8 V and the slow start charge current (Iss) is 2.3µA.

$$Tss(ms) = \frac{Css(nF) \times Vref(V)}{Iss(\mu A)} \quad (6)$$

When the input UVLO is triggered, the EN pin is pulled below 1.21V, or a thermal shutdown event occurs the device stops switching and enters low current operation. At the subsequent power up, when the shutdown condition is removed, the device does not start switching until it has discharged its SS pin to ground ensuring proper soft start behavior.

Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the VSENSE pin is between 94% and 104% of the internal voltage reference the PWRGD pin pull-down is de-asserted and the pin floats. It is recommended to use a pull-up resistor between the values of 10kΩ and 100kΩ to a voltage source that is 5.5V or less. The PWRGD is in a defined state once the VIN input voltage is greater than 1V but with reduced current sinking capability. The PWRGD achieves full current sinking capability once the VIN input voltage is above 4.5V.

The PWRGD pin is pulled low when VSENSE is lower than 92% or greater than 106% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the input UVLO or thermal shutdown are asserted, the EN pin is pulled low or the SS pin is below 1.4V.

In internal regulation mode, to avoid PWRGD jitters due to large jumps in the I^2C-controlled Vout setting, it is possible to “blank” the PWRGD being pulled down for some number of CLK cycles. Please refer to Explanation of Special Codes - PWRGD Blanking Control Codes for the details.

Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than the BOOT-PH UVLO threshold which is typically 2.1V. When the voltage between BOOT and PH drops below the BOOT-PH UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails 100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4V.

Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

High-side MOSFET overcurrent protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

Low-side MOSFET overcurrent protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the device will shut down itself and restart after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

Overheat Protection

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 170°C typically. Once the junction temperature drops below 160°C typically, the internal thermal hiccup timer will start to count. The device reinitiates the power up sequence after the built-in thermal shutdown hiccup time (32768 cycles) is over.

Programming the Output Voltage by Internal Regulation Mode

On the TPS56921, the serial bus is inactive until the chip is enabled and the soft start time has elapsed. Until then, the serial bus will ignore communications and will not acknowledge. During this time, the TPS56921's output voltage will be determined by the external resistor divider feedback to the **VSENSE** pin. When SS crosses 1.2V the serial interface becomes active and the user may program VOUT by writing to the interface via SDA and SCL. On the first successful I^2C write, the device switches to internal regulation mode. In internal regulation mode, the VOUT pin serves as the feedback path, and the VSENSE pin voltage is ignored.

I^2C Compatible Interface

The TPS56921 implements a subset of the Philips I^2C specification Ver. 1.1. The TPS56921 is a slave-only (it does not write data to the I^2C bus), and a complete I^2C transaction consists of writing the TPS56921's 8-bit address / direction byte followed by a single 8-bit data byte. Long-form address modes and multi-byte data transfers are not supported in this implementation. If the TPS56921 fails to acknowledge either of these two bytes, the master should consider the transfer to be a failure, and should issue a STOP command and try again.

The serial interface pins are composed of the **SDA** (Data) and **SCL** (Clock) pins, and the **A0** and **A1** pins to set up the chip's address. **SDA** and **SCL** are designed to be used with pullup resistors to 3.3V. **A0** and **A1** are designed to be either grounded (logic LOW) or left open (logic HIGH) and should not tie to a high voltage.

I^2C Compatible Protocol

Input voltage

Logic levels for the serial interface are not fixed. For the TPS56921, a logic "0" (LOW) should be 0V and a logic "1" (HIGH) can be any voltage between 2.5V and 3.3V. Logic HIGH is generated by external pullup resistors (see next paragraph).

Output voltage

The serial bus has external pullup resistors, one for SCL and one for SDA. These pull up to a voltage called VDD which must lie between 2.5V and 3.3V. The outputs are pulled down to their logic LOW levels by open-drain outputs and pulled up to their logic HIGH levels by these external pullups. The pullups must be selected so that the current into any chip when pulled LOW by that chip's open drain output (=VDD/RPULLUP) is less than 3mA.

Data format

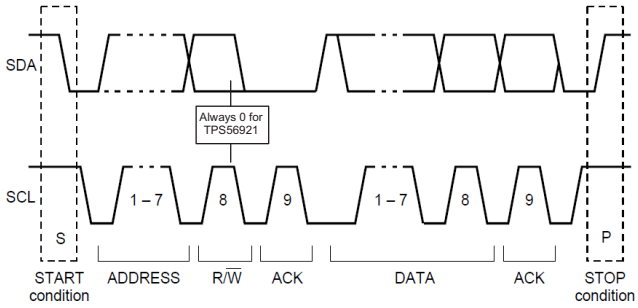
One clock pulse on the **SCL** clock line is generated for each bit of data to be transferred. The data on the **SDA** line must be stable during the HIGH period of the SCK clock line. The HIGH or LOW state of the data line can only change when the clock signal on the **SCL** line is LOW. The MSB of the address and data bytes are sent first, that is D[6] of the address byte and the ChkSum bit for the data byte.

Start and Stop conditions

A HIGH to LOW transition on the **SDA** line while the **SCL** line is HIGH defines a START condition. A LOW to HIGH transition on the **SDA** line while the **SCL** line is HIGH defines a STOP condition. START and STOP conditions are always generated by the Master. The bus is considered to be BUSY after the condition. It is considered to be free again after a minimum of 1.3µS after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. START and repeated START are functionally identical.

Every byte of data out on the **SDA** line is 8 bits long. 9 clocks occur for each byte (the additional clock being for an ACK signal put onto the bus by the TPS56921 pulling down on the bus to acknowledge receipt of the data). Exactly two bytes should be transferred to the TPS56921 per transfer, a 7-bit address and R/W byte followed by a data byte as shown in the following waveform:



A Complete Address and Data Transfer - Adapted from Philips I²C Specification

When the TPS56921 receives an address code it recognizes to be its own, it will respond by sending an ACK (pulling down on the **SDA** bus during clock 9 on the **SCL** bus). If the address is not recognized, the TPS56921 assumes that the I²C message is intended for another chip on the bus, and it takes no action. It will disregard data sent thereafter until the next START is begun.

If, after recognizing its address, the TPS56921 receives a valid data byte (checked by comparing the ChkSum sent to the D[6:0] data), it will send an ACK and will set the output voltage to the desired value. If the byte is deemed invalid, ACK will not be sent and the Master will need to retry by sending a new START sequence and an initiating resend of the entire address/data packet.

I²C Address Byte

The 7-bit address of the TPS56921 can be any number between 34h (0110100) and 37h (0110111). The 5 MSBs are set internally and the 2 LSBs are customer-selectable via the **A1** and **A0** pins, allowing up to 4 TPS56921s to be controlled on the same serial bus. When the Master is sending the address as an 8-bit value, the 7-bit address should be sent followed by a trailing 0 to indicate this is a WRITE operation. The following codes assume this trailing zero.

Table 1. TPS56921 Address as a Function of A1 and A0 Pins

A1	A0	TPS56921 Address (binary)	TPS56921 Address (hex)
Ground (0)	Ground (0)	01101000	68h
Ground (0)	Open (1)	01101010	6Ah
Open (1)	Ground (0)	01101100	6Ch
Open (1)	Open (1)	01101110	6Eh

I²C Data Byte

The 8 bits of data sent over the serial bus controls the VOUT of the TPS56921. After the SoftStart time has elapsed (SS pin voltage goes above approx. 1.23V), the serial interface becomes active and the user may program VOUT by writing to the interface. The data is structured thus:

Table 2. Structure of TPS56921 Data byte

8	7	6	5	4	3	2	1
ChkSum	D6	D5	D4	D3	D2	D1	D0

D[6:0] – These bits are the 7-bit selector for one of 77 output voltages. The voltages are selected from the following table:

Table 3. Ideal VOUT vs. Code

Code	Binary	VOUT	Code	Binary	VOUT	Code	Binary	VOUT
0	0000000	0.720	26	0011010	0.980	52	0110100	1.240

Table 3. Ideal VOUT vs. Code (continued)

Code	Binary	VOUT	Code	Binary	VOUT	Code	Binary	VOUT
0	0000000	0.720	26	0011010	0.980	52	0110100	1.240
1	0000001	0.730	27	0011011	0.990	53	0110101	1.250
2	0000010	0.740	28	0011100	1.000	54	0110110	1.260
3	0000011	0.750	29	0011101	1.010	55	0110111	1.270
4	0000100	0.760	30	0011110	1.020	56	0111000	1.280
5	0000101	0.770	31	0011111	1.030	57	0111001	1.290
6	0000110	0.780	32	0100000	1.040	58	0111010	1.300
7	0000111	0.790	33	0100001	1.050	59	0111011	1.310
8	0001000	0.800	34	0100010	1.060	60	0111100	1.320
9	0001001	0.810	35	0100011	1.070	61	0111101	1.330
10	0001010	0.820	36	0100100	1.080	62	0111110	1.340
11	0001011	0.830	37	0100101	1.090	63	0111111	1.350
12	0001100	0.840	38	0100110	1.100	64	1000000	1.360
13	0001101	0.850	39	0100111	1.110	65	1000001	1.370
14	0001110	0.860	40	0101000	1.120	66	1000010	1.380
15	0001111	0.870	41	0101001	1.130	67	1000011	1.390
16	0010000	0.880	42	0101010	1.140	68	1000100	1.400
17	0010001	0.890	43	0101011	1.150	69	1000101	1.410
18	0010010	0.900	44	0101100	1.160	70	1000110	1.420
19	0010011	0.910	45	0101101	1.170	71	1000111	1.430
20	0010100	0.920	46	0101110	1.180	72	1001000	1.440
21	0010101	0.930	47	0101111	1.190	73	1001001	1.450
22	0010110	0.940	48	0110000	1.200	74	1001010	1.460
23	0010111	0.950	49	0110001	1.210	75	1001011	1.470
24	0011000	0.960	50	0110010	1.220	76	1001100	1.480
25	0011001	0.970	51	0110011	1.230	>76	>1001100	Illegal / Special

Any code >76 is illegal except for the following special control codes:

Table 4. Special Control Codes

Special Code	Function
1111000	Set delay from PWRGD fault to PWRGD pin pulldown to zero
1111001	Set delay from PWRGD fault to PWRGD pin pulldown to 4 CLK cycles (default)
1111010	Set delay from PWRGD fault to PWRGD pin pulldown to 8 CLK cycles
1111011	Set delay from PWRGD fault to PWRGD pin pulldown to 4 CLK cycles (default)
1111111	Change back to external regulation mode

Explanation of Special Codes - PWRGD Blanking Control Codes

Especially for low load currents, large jumps in the I^2C-controlled Vout setting may have a long settling time compared to the UV/OV thresholds. If this happens, it will cause the PWRGD signal to temporarily indicate a fault condition.

If this is not the desired behavior, it is possible to “blank” the PWRGD being pulled down for some number of CLK cycles, whether the CLK frequency is being set by an RT resistor or by an external CLK at the RT/CLK pin. The user can set this delay to 4, 8 or 16 CLK cycles using the 11110xx codes shown on the previous page. On power-up, the delay defaults to 4 clock cycles. The user can reset the blanking time using these codes at any time without affecting any other device behavior.

Alternatively, the user can avoid this by sequentially programming the VOUT in smaller steps. This method allows the system enough time to respond to large VOUT transitions. The same behavior can occur when changing from external to internal mode, so the user should first select a VOUT equal to the externally-set VOUT, then move in small steps to the desired VOUT.

Explanation of Special Codes – Return to External Control Mode

It may be desired to return the IC to being controlled by the external resistor divider feeding back to the VSENSE pin rather than using the I^2C codes. If so, the user may send code 1111111 to the serial interface, and the TPS56921 will switch back to external feedback mode. The next write of a valid VOUT code to the serial interface will return the part to internal regulation mode.

None of the other special codes change the VOUT voltage, nor will they cause a switch from External to Internal regulation modes. Note that code 1111000 puts the part into no-delay mode if it is desired that PWRGD indicates that the output is temporarily out of regulation.

ChkSum Bit

The ChkSum bit should be set by the Master controller to be the exclusive-OR of the D[6:0] bits (even parity). This will be used by the TPS56921 to check that a valid data byte was received. If ChkSum is not equal to the exclusive-OR of the D[6:0] bits, the TPS56921 assumes that an error occurred during the data transmission, and it will not send an ACK bit, nor will it reset the VOUT to the received code. The Master should try again to send the data.

Unless they are among the previously-discussed “Special Codes”, sending D[6:0] bits outside of the range 0 to 76 decimal causes the TPS56921 to assume that an error occurred during the data transmission, and it will not send an ACK bit, nor will it change the VOUT. The Master should try again to send the data.

Small Signal Model for Loop Response

Figure 21 shows an equivalent model for the device control loop which can be modeled in a circuit simulation program to check frequency response and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Roea (2.38 MΩ) and capacitor Coea (20.7 pF) model the open loop gain and frequency response of the error amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c and c/b show the small signal responses of the power stage and frequency compensation respectively. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

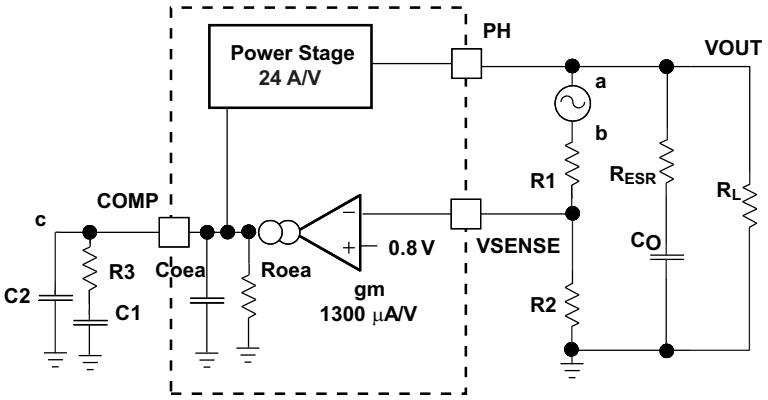


Figure 21. Small Signal Model for Loop Response

Simple Small Signal Model for Peak Current Mode Control

Figure 22 is a simple small signal model that can be used to understand how to design the frequency compensation. The device power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 7 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 21) is the power stage transconductance (gm_{ps}) which is 24 A/V for the device. The DC gain of the power stage is the product of gm_{ps} and the load resistance, R_L, as shown in Equation 8 with resistive loads. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see Equation 9). The combined effect is highlighted by the dashed line in Figure 23. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

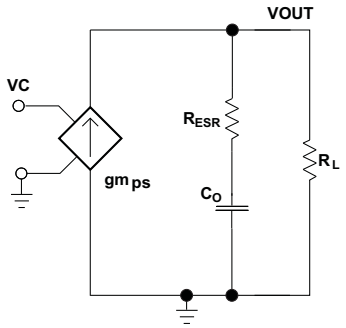


Figure 22. Simplified Small Signal Model for Peak Current Mode Control

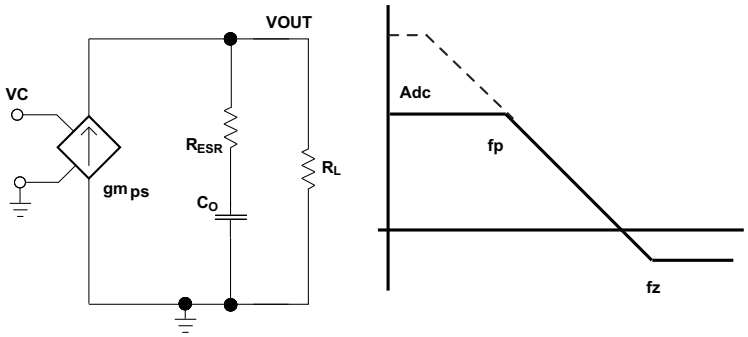


Figure 23. Simplified Frequency Response for Peak Current Mode Control

$$\frac{VOUT}{VC} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (7)$$

$$Adc = gm_{ps} \times R_L \quad (8)$$

$$fp = \frac{1}{C_O \times R_L \times 2\pi} \quad (9)$$

$$fz = \frac{1}{C_O \times R_{ESR} \times 2\pi} \quad (10)$$

Where

gm_{ea} is the GM amplifier gain (1300µA/V)
gm_{ps} is the power stage gain (24A/V).
R_L is the load resistance
C_O is the output capacitance.
R_{ESR} is the equivalent series resistance of the output capacitor.

Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used Type II compensation circuits and a Type III frequency compensation circuit, as shown in Figure 24. In Type 2A, one additional high frequency pole, C6, is added to attenuate high frequency noise. In Type III, one additional capacitor, C11, is added to provide a phase boost at the crossover frequency and it will only work for external regulation mode.

The design guidelines below are provided for advanced users who prefer to compensate using the general method. The below equations only apply to designs whose ESR zero is above the bandwidth of the control loop. This is usually true with ceramic output capacitors. See the Application Information section for a step-by-step design procedure using higher ESR output capacitors with lower ESR zero frequencies.

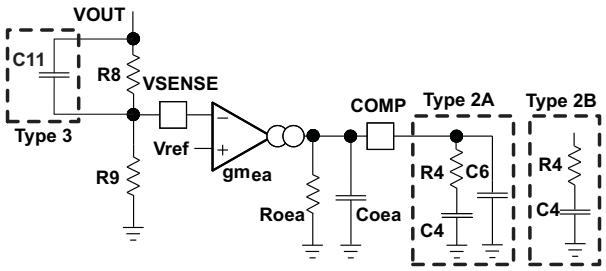


Figure 24. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency, fc. A good starting point is 1/10th of the switching frequency, fsw.
2. R4 can be determined by:

$$R4 = \frac{2\pi \times fc \times VOUT \times Co}{gm_{ea} \times Vref \times gm_{ps}} \quad (11)$$

Where:

gm_{ea} is the GM amplifier gain (1300µA/V)
gm_{ps} is the power stage gain (24A/V)
Vref is the reference voltage (0.8V)

3. Place a compensation zero at the dominant pole: $\left(fp = \frac{1}{C_O \times R_L \times 2\pi} \right)$
   C4 can be determined by:

$$C4 = \frac{R_L \times Co}{R4} \quad (12)$$

4. C6 is optional. It can be used to cancel the zero from the ESR (Equivalent Series Resistance) of the output capacitor Co.

$$C6 = \frac{R_{ESR} \times Co}{R4} \quad (13)$$

APPLICATION INFORMATION

Design Guide – Step-By-Step Design Procedure

This example details the design of a high frequency switching regulator design using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

Table 5.

Parameter	Value
Output Voltage	1.1 V
Output Current	9 A
Transient Response 4.5 A load step	ΔVout = +/- 9 %
Input Voltage	12 V nominal, 4.5 V to 17 V
Output Voltage Ripple	20 mV p-p
Start Input Voltage (Rising Vin)	Internal UVLO
Stop Input Voltage (Falling Vin)	Internal UVLO
Switching Frequency	500 kHz

Typical Application Schematic

The application schematic of Figure 25 was developed to meet the requirements above. This circuit is available as the TPS56921EVM-188 evaluation module. The design procedure is given in this section.

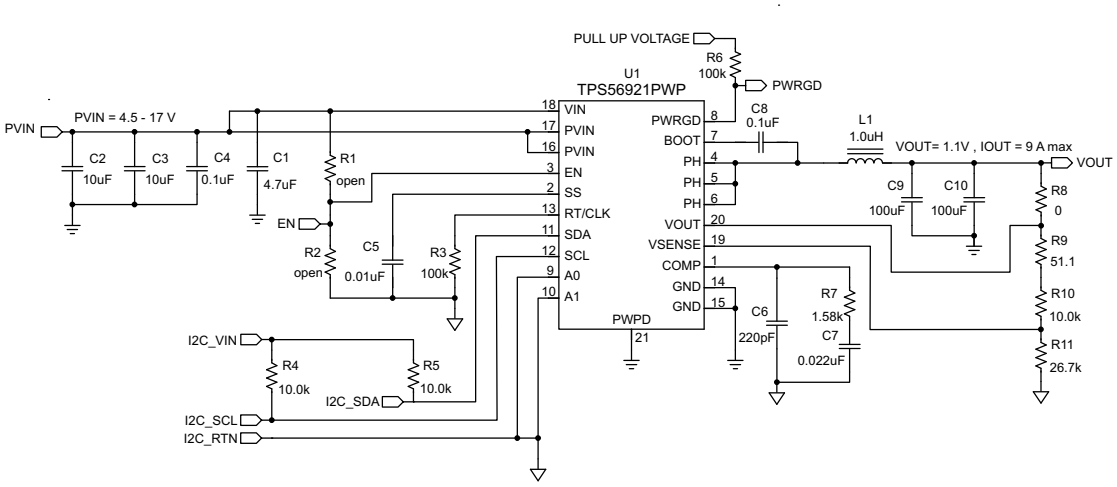


Figure 25. Typical Application Circuit

Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade off between higher and lower switching frequencies. Higher switching frequencies may produce smaller a solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which hurt the converter's efficiency and thermal performance. Also the minimum controllable on time must be considered. Make sure the chosen operating frequency will allow proper operation without pulse skipping at the maximum input voltage. In this design, a moderate switching frequency of 500 kHz is selected to achieve both a small solution size and a high efficiency operation.

Output Inductor Selection

To calculate the value of the output inductor, use Equation 14. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, KIND is normally from 0.1 to 0.3 for the majority of applications.

$$L1 = \frac{Vinmax - Vout}{Io \cdot Kind} \cdot \frac{Vout}{Vinmax \cdot fsw} \quad (14)$$

For this design example, use KIND = 0.3 and the minimum inductor value is calculated to be 0.76 µH. For this design, a standard value above the calculated minimum was chosen: 1.0 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 16 and Equation 17.

$$Iripple = \frac{Vinmax - Vout}{L1} \cdot \frac{Vout}{Vinmax \cdot fsw} \quad (15)$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \cdot \left(\frac{V_o \cdot (Vinmax - Vo)}{Vinmax \cdot L1 \cdot fsw} \right)^2} \quad (16)$$

$$ILpeak = Iout + \frac{Iripple}{2} \quad (17)$$

For this design, the RMS inductor current is 9.02 A and the peak inductor current is 10.03 A. The chosen inductor is a Wurth 744311100 1.0 µH. It has a saturation current rating of 19 A and a RMS current rating of 15 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 18 shows the minimum output capacitance necessary to accomplish this.

$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout} \quad (18)$$

Where ΔIout is the change in output current, Fsw is the regulators switching frequency and ΔVout is the allowable change in the output voltage. For this example, the transient load response is specified as a 9% change in Vout for a load step of 4.5 A. For this example, ΔIout = 4.5 A and ΔVout = 0.09 x 1.1 = 0.099 V. Using these numbers gives a minimum capacitance of 182 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 19 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 20 mV. Under this requirement, Equation 19 yields 26 µF.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{Vripple}{Iripple}} \tag{19}$$

Equation 20 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 20 indicates the ESR should be less than 9.7 mΩ. In this case, the ceramic caps' ESR is much smaller than 9.7 mΩ.

$$Resr < \frac{Vripple}{Iripple} \tag{20}$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, two 100 µF 6.3V X5R ceramic capacitor with 3 mΩ of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation 21 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 21 yields 594 mA.

$$Icorms = \frac{Vout \cdot (Vinmax - Vout)}{\sqrt{12} \cdot Vinmax \cdot L1 \cdot fsw} \tag{21}$$

Input Capacitor Selection

The TPS56921 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance on the PVIN input voltage pins and 4.7 µF on the Vin input voltage pin. In some applications additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS56921. The input ripple current can be calculated using Equation 22.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vinmin} \cdot \frac{(Vinmin - Vout)}{Vinmin}} \tag{22}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25 V voltage rating is required to support the maximum input voltage. For this example, two 10 µF and one 4.7 µF 25 V capacitors in parallel have been selected as the VIN and PVIN inputs are tied together so the TPS56921 may operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 23. Using the design example values, Ioutmax = 9 A, Cin = 24.7 µF, Fsw=500 kHz, yields an input voltage ripple of 182 mV and a RMS input ripple current of 3.87 A.

$$\Delta Vin = \frac{Ioutmax \cdot 0.25}{Cin \cdot fsw} \tag{23}$$

Slow Start Capacitor Selection

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS56921 reach the current limit or excessive current draw from the input power supply may cause the input

voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft start capacitor value can be calculated using Equation 24. For the example circuit, the soft start time is not too critical since the output capacitor value is 2 x 100 µF which does not require much current to charge to 1.1 V. The example circuit has the soft start time set to an arbitrary value of 3.5 ms which requires a 10 nF capacitor. In TPS56921, Iss is 2.3 µA and Vref is 0.8V.

$$C5(nF) = \frac{Tss(mS) \bullet Iss(\mu A)}{Vref(V)} \quad (24)$$

Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10V or higher voltage rating.

Under Voltage Lockout Set Point

The Under Voltage Lock Out (UVLO) can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between VIN and the EN pin of the TPS56921 and R2 is connected between EN and GND . The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the minimum input voltage is 4.5 V, so the internal UVLO thresholds are used and R1 and R2 are open. Equation 3 and Equation 4 can be used to calculate the values for the upper and lower resistor values.

Output Voltage Feedback Resistor Selection

The resistor divider network R10 and R11 is used to set the output voltage. For the example design, 10 kΩ was selected for R10. Using Equation 25, R11 is calculated as 26.67 kΩ. The nearest standard 1% resistor is 26.7 kΩ.

$$R11 = \frac{R10 \cdot Vref}{Vo - Vref} \quad (25)$$

Compensation Component Selection

There are several possible methods to design closed loop compensation for dc/dc converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at -20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and starts to fall one decade below the modulator pole frequency reaching a minimum of -90 degrees one decade above the modulator pole frequency. The modulator pole is a simple pole shown in Equation 26

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \quad (26)$$

For the TPS56921 most circuits will have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics will deviate from the ideal approximations. The phase loss of the power stage will now approach -180 degrees, making compensation more difficult. The power stage transfer function can be solved but it is a tedious hand calculation that does not lend itself to simple approximations. It is best to use Pspice or TINA-TI to accurately model the power stage gain and phase so that a reliable compensation circuit can be designed. That is the technique used in this design procedure. Using the pspice model of (insert link here). Apply the values calculated previously to the output filter components of L1, C9 and C10. Set Rload to the appropriate value. For this design, L1 = 1.0 µH. C9 and C10 are set to 100µF each, and the ESR is set to 3 mΩ. The Rload resistor is 1.1 V / 4 A = 275 mΩ for approximately one half rated load. Now the power stage characteristic can be plotted as shown in Figure 26.

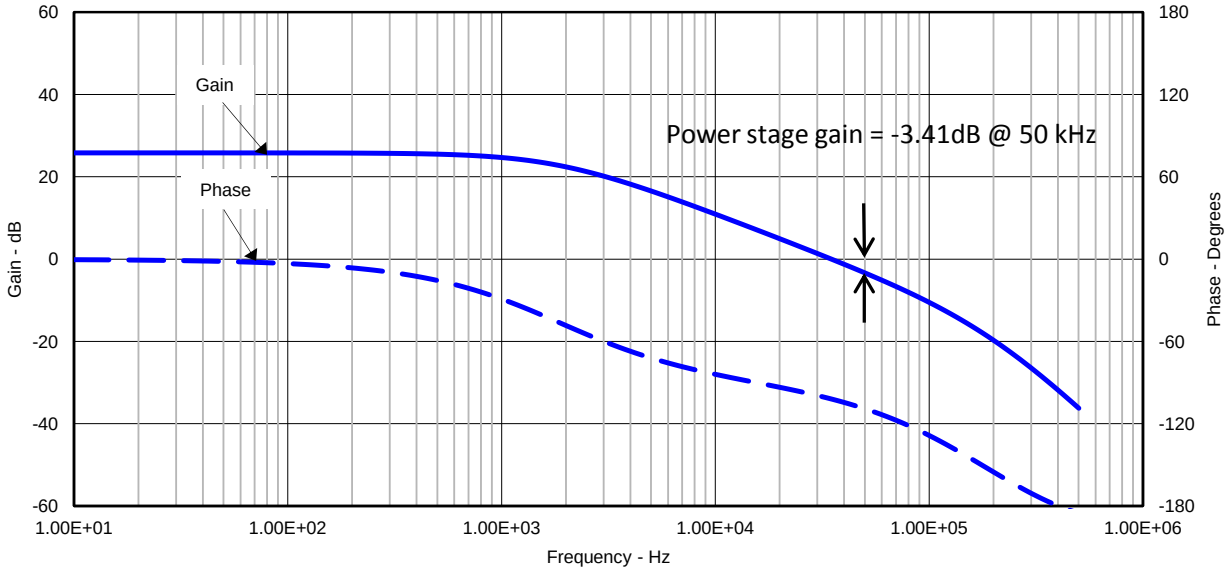


Figure 26. Power stage Gain and Phase Characteristics

For this design, the intended crossover frequency is 50 kHz. From the power stage gain and phase plots, the gain at 50 kHz is -3.41 dB and the phase is about -110 degrees. For 60 degrees of phase margin, additional phase boost from a feed forward capacitor in parallel with the upper resistor of the voltage set point divider is not needed. R7 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. The required value of R7 can be calculated from Equation 27.

$$R7 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{EA}} \cdot \frac{V_{REF}}{V_{OUT}} \quad (27)$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 50 kHz. The required value for C7 is given by Equation 28.

$$C7 = \frac{1}{2 \cdot \pi \cdot R7 \cdot \frac{F_{CO}}{10}} \quad (28)$$

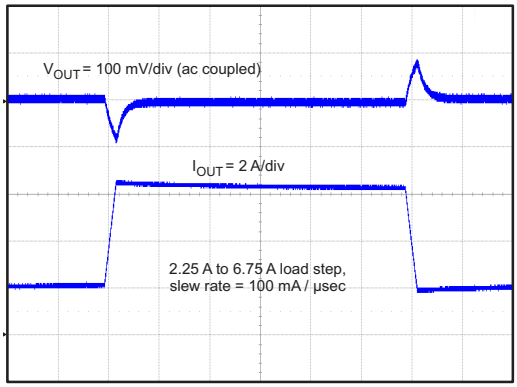
To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 50 kHz. The pole can also be useful to offset the ESR of aluminum electrolytic output capacitors. The value for C6 can be calculated from Equation 29.

$$C6 = \frac{1}{2 \cdot \pi \cdot R7 \cdot 10 \cdot F_{CO}} \quad (29)$$

For this design the calculated values for the compensation components are R7 = 1.58 kΩ ,C7 = 0.022 µF and C6 = 220 pF.

Application Curves

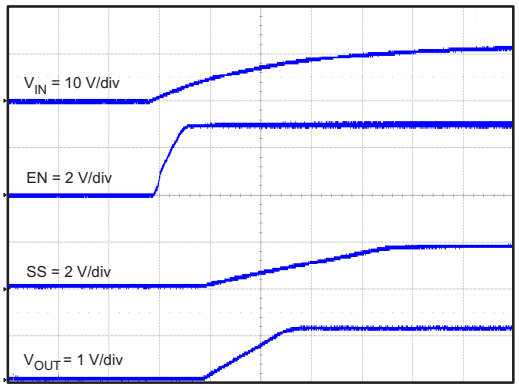
LOAD TRANSIENT



Time = 200 µs/div

Figure 27.

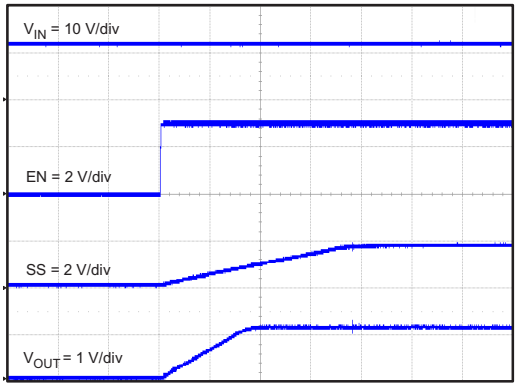
STARTUP with VIN



Time = 2 ms/div

Figure 28.

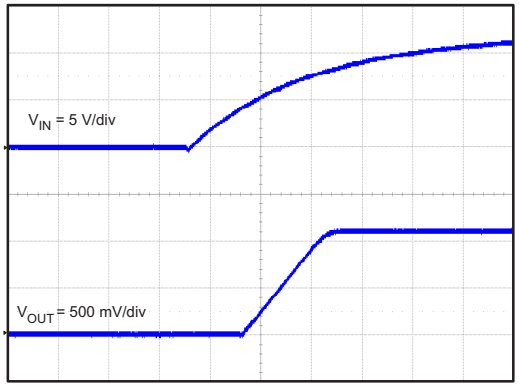
STARTUP with EN



Time = 2 ms/div

Figure 29.

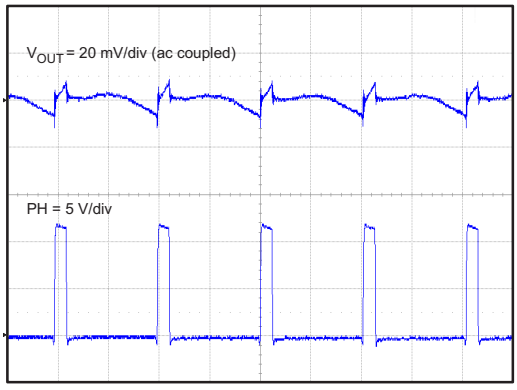
STARTUP VOUT DETAIL



Time = 2 ms/div

Figure 30.

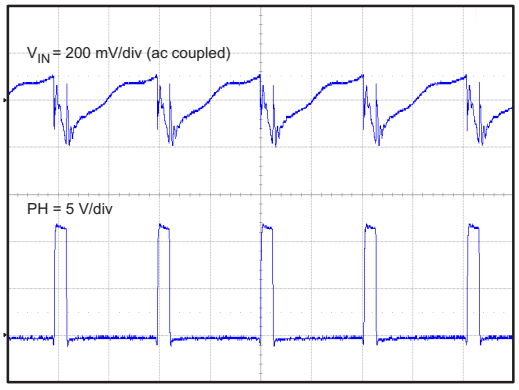
OUTPUT VOLTAGE RIPPLE with FULL LOAD



Time = 1 µs/div

Figure 31.

INPUT VOLTAGE RIPPLE with FULL LOAD



Time = 1 µs/div

Figure 32.

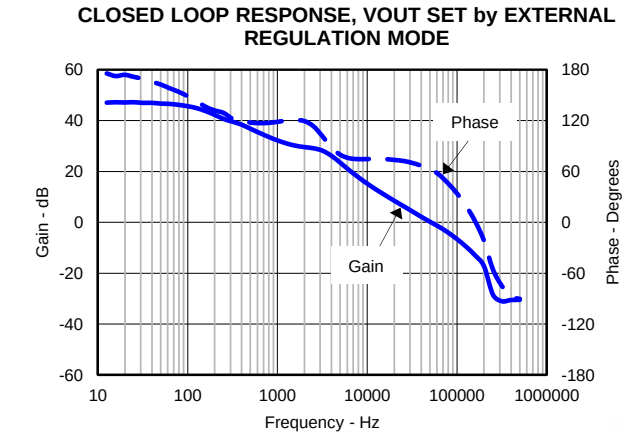


Figure 33.

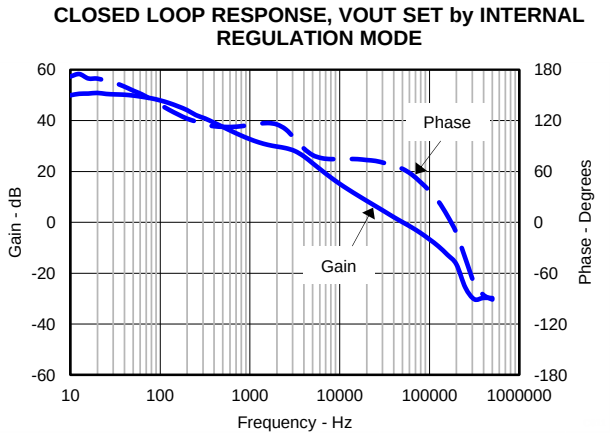


Figure 34.

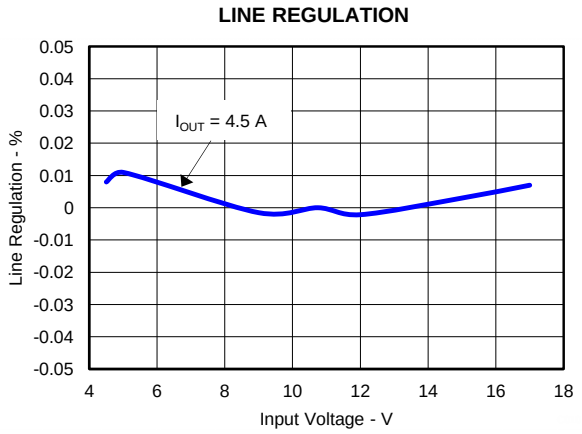


Figure 35.

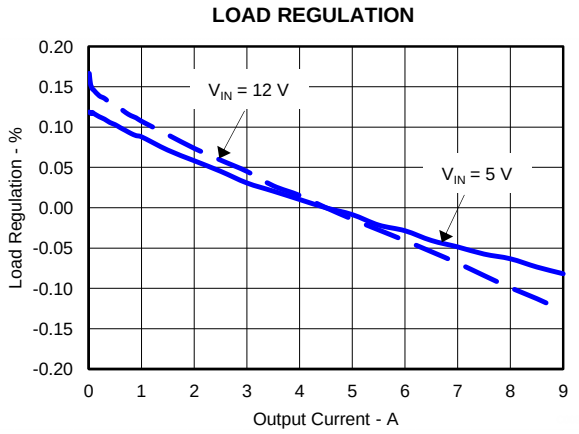


Figure 36.

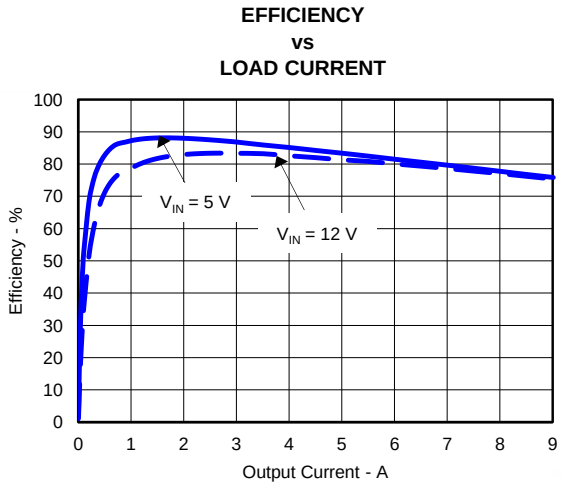


Figure 37.

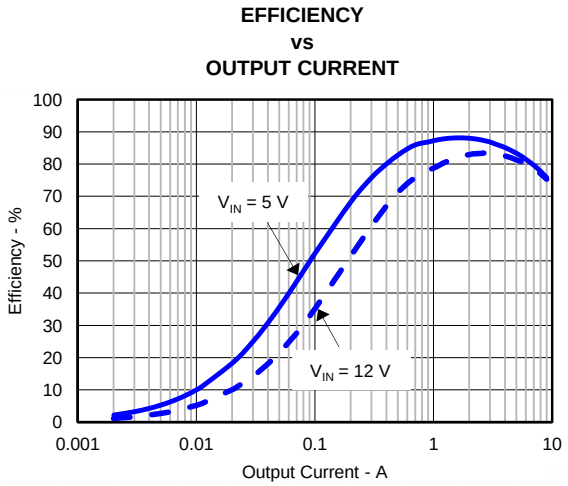


Figure 38.

PCB Layout Guidelines

Layout is a critical portion of good power supply design. See Figure 39 for a PCB layout example. The top layer contains the main power traces for VIN, VOUT, and PH (switching node). Also on the top layer are connections for the remaining pins of the TPS56921 and a large top side area filled with ground. The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS56921. The vias under the device provide a thermal path from the exposed thermal pad land to ground additional vias are included adjacent to the exposed thermal pad. The GND pins should be tied directly to the power pad under the IC and the power pad. For operation at full rated load, the top side ground area together with the internal and / or bottom side ground planes, must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric. Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components should be grounded to a separate analog ground path as shown. In this example, the analog ground (AGND) is located on an internal layer. Connect the AGND and PGND together at a single point only. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. The VOUT pin is required to be connected to the output voltage if the serial interface is used to set the output voltage. The A0 and A1 lines should both be connected to AGND. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

Land pattern and stencil information is provided in the data sheet addendum.

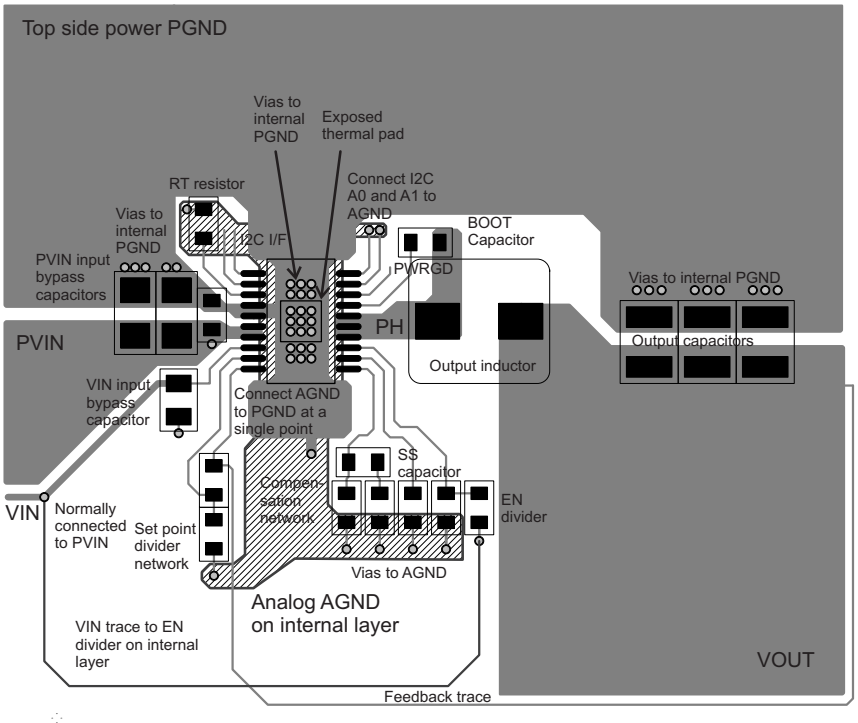


Figure 39. PCB Layout

Estimated Circuit Area

The estimated printed circuit board area for the components used in the design of Figure 25 is 0.737 in^2 (475mm^2). This area does not include test points or connectors.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS56921PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	56921	Samples
TPS56921PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	56921	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

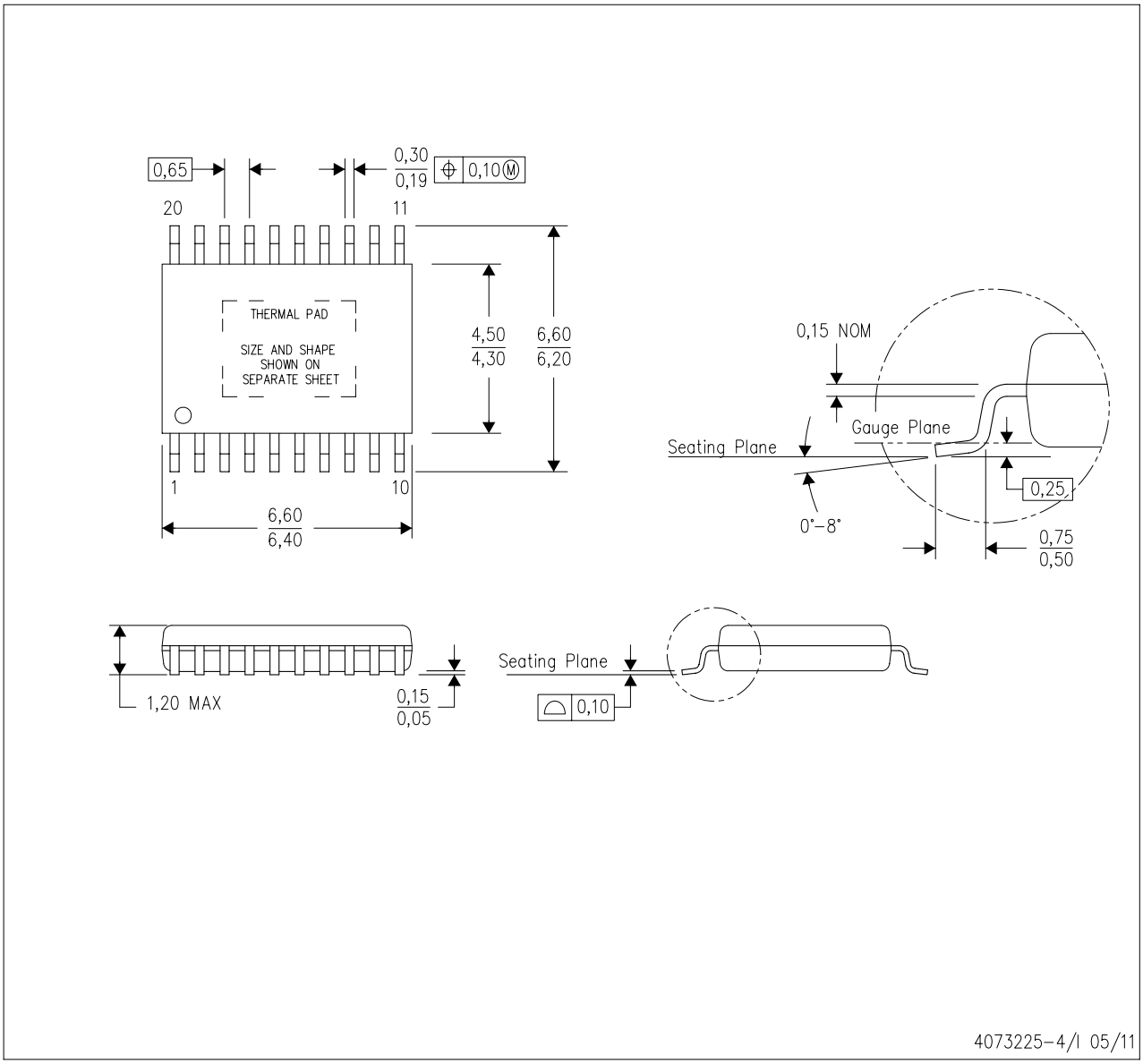
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

MECHANICAL DATA

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

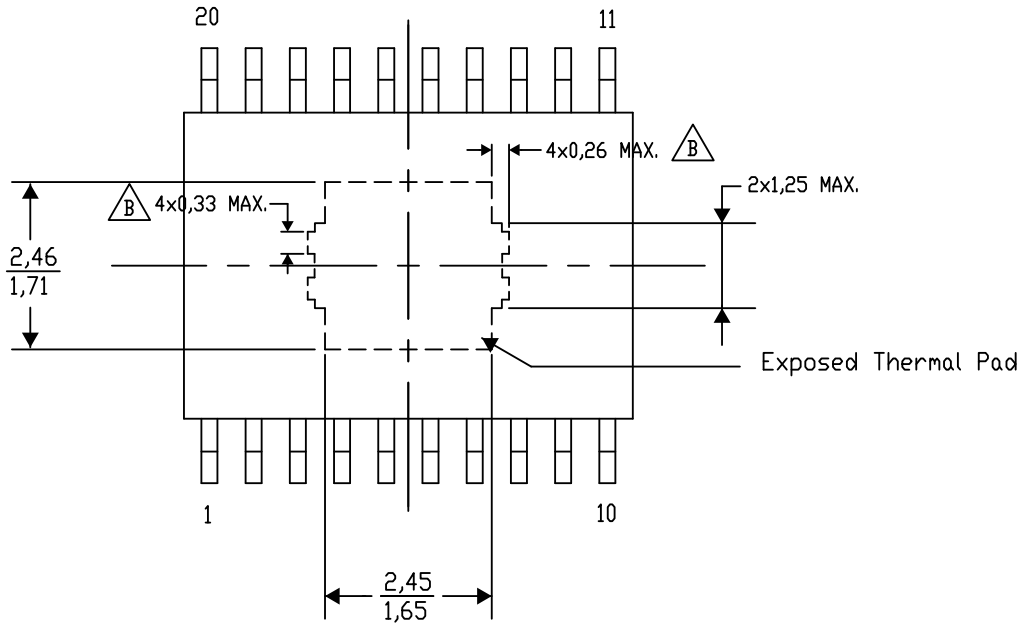
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–43/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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