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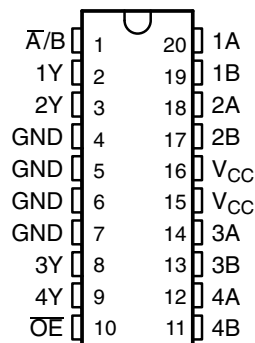
sales@integrated-circuit.com

74ACT11257 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS053B – JANUARY 1989 – REVISED APRIL 1996

- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Interface Directly With System Bus
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Provides Bus Interface From Multiple Sources in High-Performance Systems
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (N)

DB, DW, OR N PACKAGE
(TOP VIEW)



description

The 74ACT11257 is designed to multiplex signals from 4-bit data sources to four output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable (\overline{OE}) input is at a high logic level.

The 74ACT11257 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

| INPUTS | | | | OUTPUT Y |
|--------|---------------|------|---|-------------|
| OE | SELECT A/B | DATA | | |
| | | A | B | |
| H | X | X | X | Z |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |



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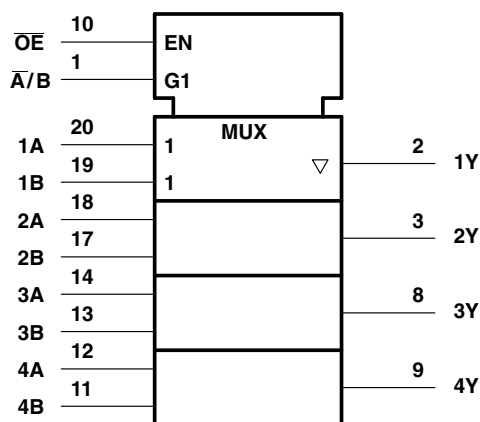
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74ACT11257

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

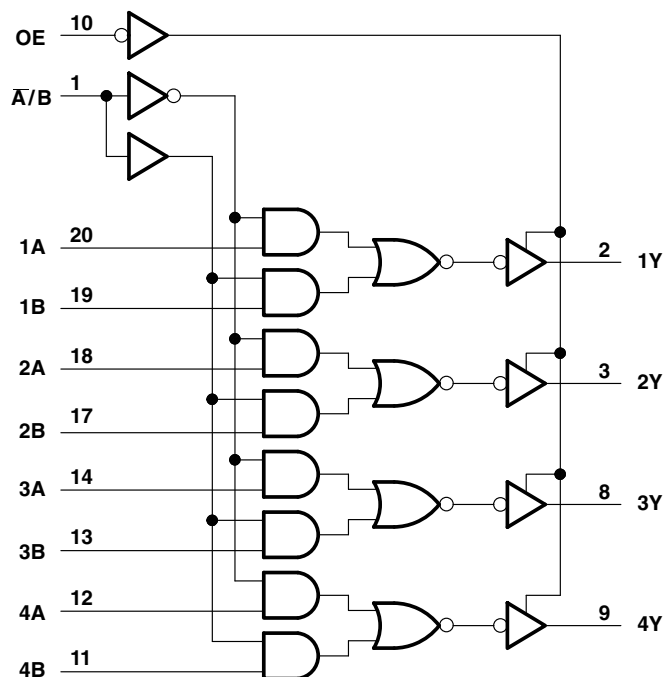
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



74ACT11257 QUADRUPL 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±50 mA |
| Continuous current through V_{CC} or GND | ±100 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package | 0.6 W |
| DW package | 1.6 W |
| N package | 1.3 W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

| | MIN | MAX | UNIT |
|--|-----|----------|------|
| V_{CC} Supply voltage | 4.5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | V |
| V_I Input voltage | 0 | V_{CC} | V |
| V_O Output voltage | 0 | V_{CC} | V |
| I_{OH} High-level output current | | –24 | mA |
| I_{OL} Low-level output current | | 24 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | 0 | 10 | ns/V |
| T_A Operating free-air temperature | –40 | 85 | °C |



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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETERS | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-------------------------------|---|-----------------|-----------------------|-----|------|------|------|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | I _{OH} = -50 µA | 4.5 V | 4.4 | | | 4.4 | | V |
| | | 5.5 V | 5.4 | | | 5.4 | | |
| | I _{OH} = -24 mA | 4.5 V | 3.94 | | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.8 | | |
| | I _{OH} = -75 mA [†] | 5.5 V | | | | 3.85 | | |
| V _{OL} | I _{OL} = 50 µA | 4.5 V | | | 0.1 | | 0.1 | V |
| | | 5.5 V | | | 0.1 | | 0.1 | |
| | I _{OL} = 24 mA | 4.5 V | | | 0.36 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.44 | |
| | I _{OL} = 75 mA [†] | 5.5 V | | | | | 1.65 | |
| I _{OZ} | V _O = V _{CC} or GND | 5.5 V | | | ±0.5 | | ±5 | µA |
| I _I | V _I = V _{CC} or GND | 5.5 V | | | ±0.1 | | ±1 | µA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 8 | | 80 | µA |
| ΔI _{CC} [‡] | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 0.9 | | 1 | mA |
| C _i | V _I = V _{CC} or GND | 5 V | | 3.5 | | | | pF |
| C _o | V _O = V _{CC} or GND | 5 V | | 8 | | | | pF |

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | MIN | MAX | UNIT |
|------------------|--------------|-------------|-----------------------|-----|-----|-----|-----|------|
| | | | MIN | TYP | MAX | | | |
| t _{PLH} | A or B | Y | 1.5 | 4.4 | 6.4 | 1.5 | 6.9 | ns |
| t _{PHL} | | | 1.5 | 5 | 8 | 1.5 | 8.7 | |
| t _{PLH} | A/B | Any Y | 1.5 | 4.7 | 7.6 | 1.5 | 8.2 | ns |
| t _{PHL} | | | 1.5 | 5.7 | 8.5 | 1.5 | 9.4 | |
| t _{PZH} | OE | Any Y | 1.5 | 4.2 | 6.9 | 1.5 | 7.3 | ns |
| t _{PZL} | | | 1.5 | 5.5 | 8.7 | 1.5 | 9.6 | |
| t _{PHZ} | OE | Any Y | 1.5 | 5.7 | 7.6 | 1.5 | 8.4 | ns |
| t _{PLZ} | | | 1.5 | 6 | 7.9 | 1.5 | 8.5 | |

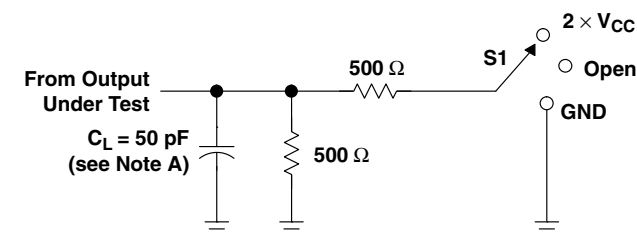
operating characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|-----------------|-------------------------------|------------------|-----------------------------------|-----|------|
| C _{pd} | Power dissipation capacitance | Outputs enabled | C _L = 50 pF, f = 1 MHz | 41 | pF |
| | | Outputs disabled | | 13 | |

74ACT11257 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

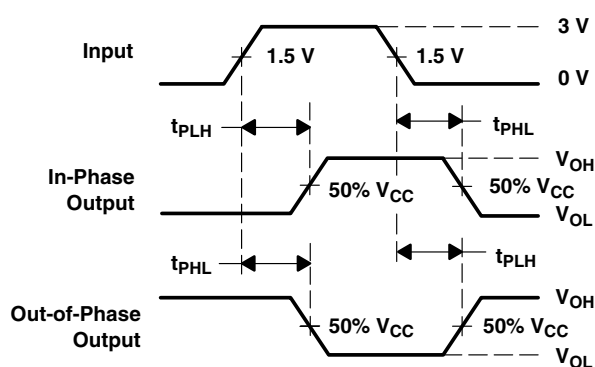
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PARAMETER MEASUREMENT INFORMATION

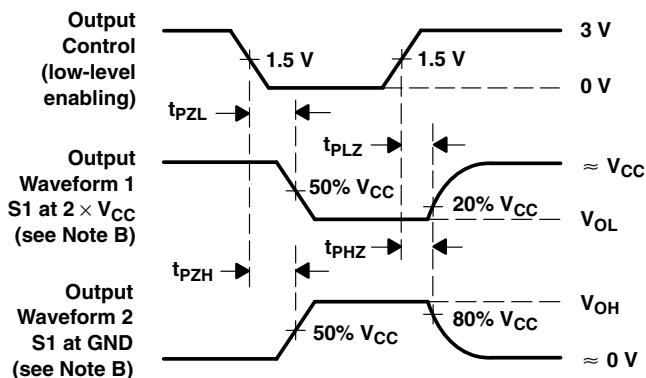


| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74ACT11257DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT11257 | Samples |
| 74ACT11257DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT11257 | Samples |
| 74ACT11257PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AT257 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

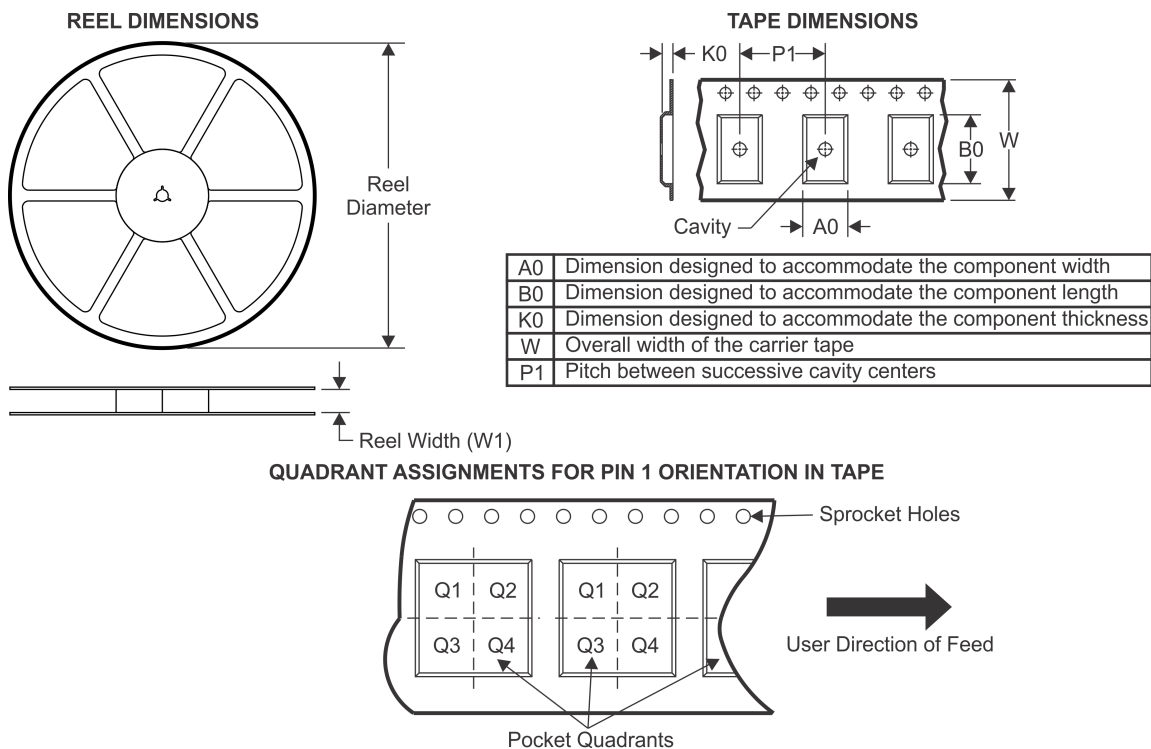
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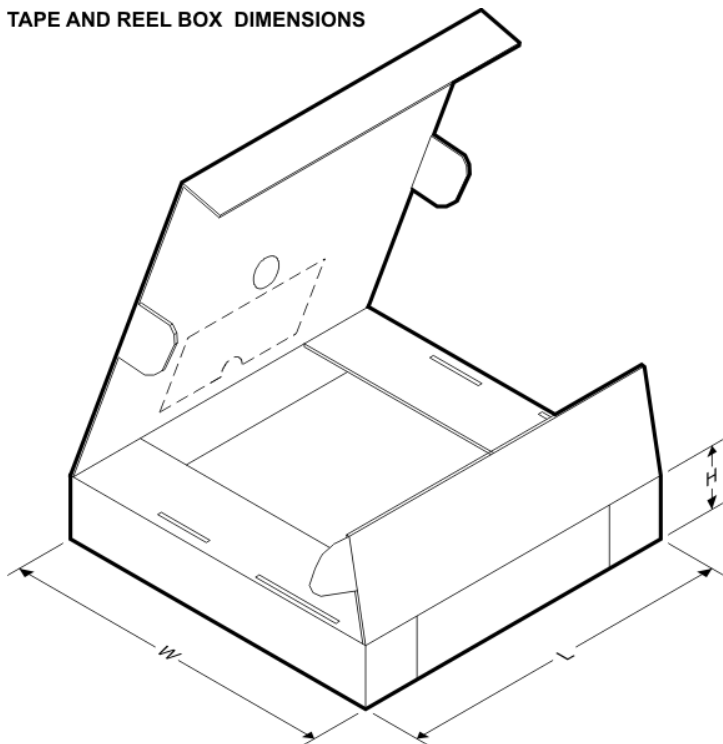
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74ACT11257DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74ACT11257DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

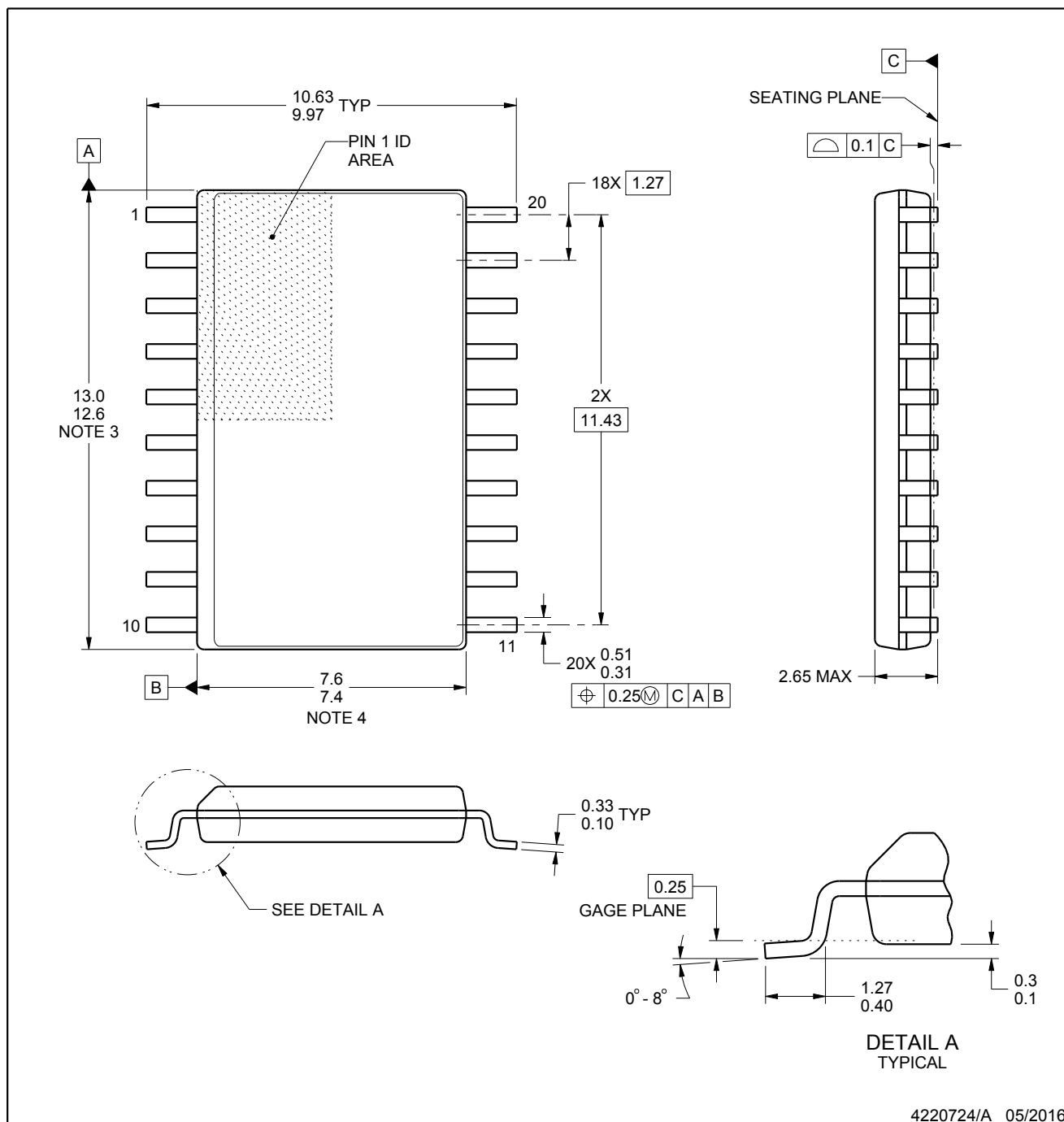


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



NOTES:

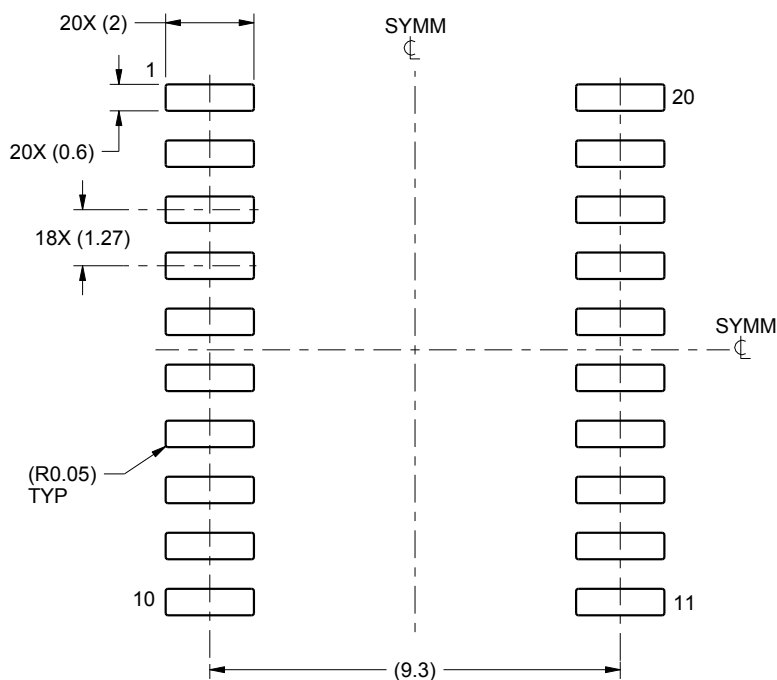
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

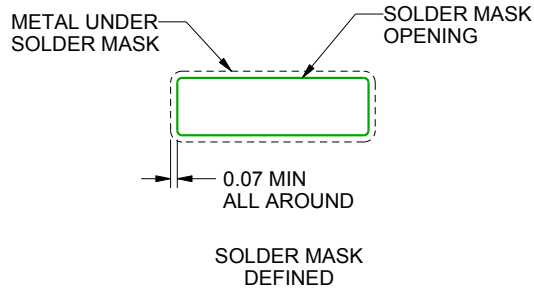
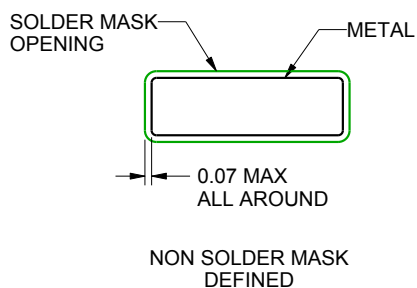
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

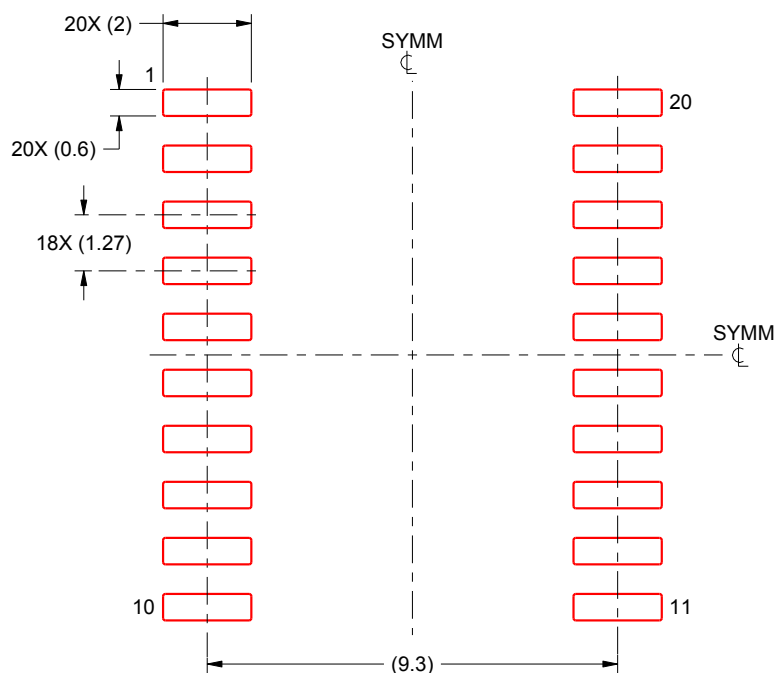
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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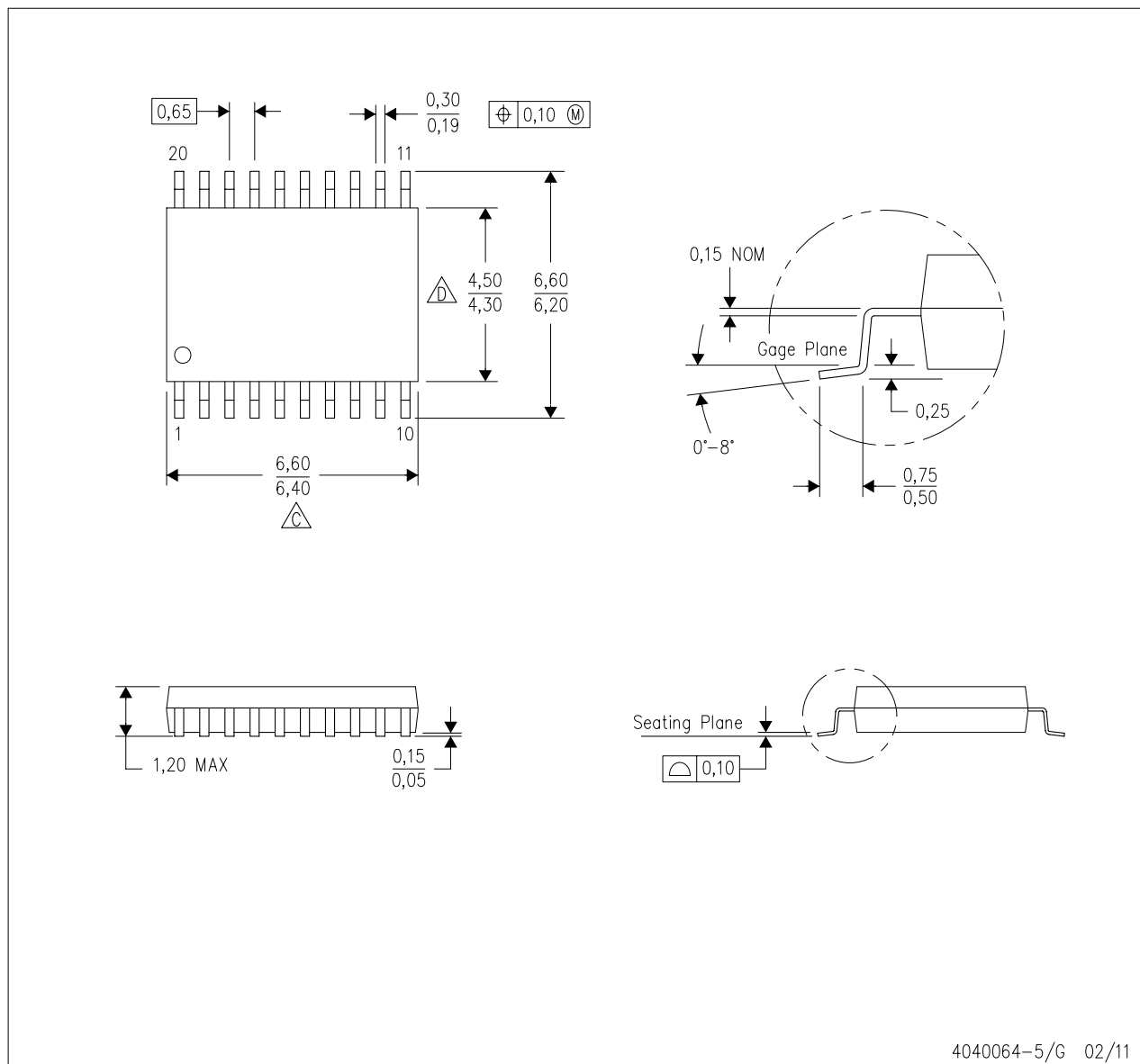
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

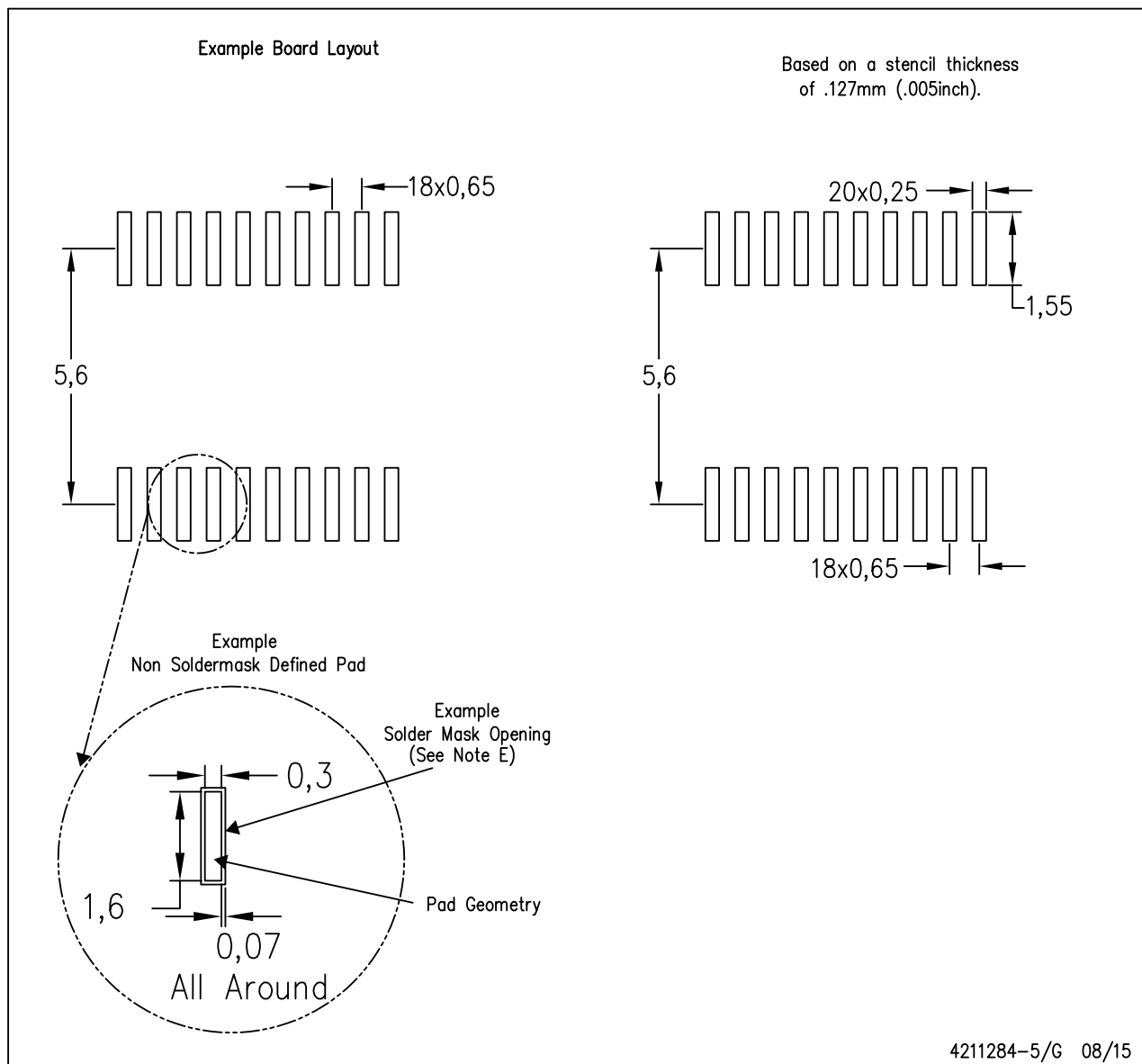


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

LAND PATTERN DATA

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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