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Texas Instruments
CD74HC373M

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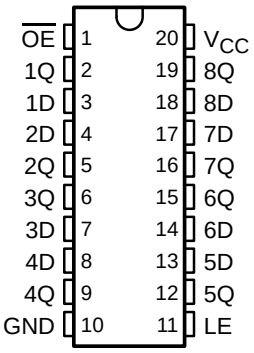
# CD54HC373, CD74HC373
# OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS452A – FEBRUARY 2001 – REVISED APRIL 2003

- **2-V to 6-V $V_{CC}$ Operation**
- **Wide Operating Temperature Range of –55°C to 125°C**
- **Balanced Propagation Delays and Transition Times**
- **Standard Outputs Drive up to 15 LS-TTL Loads**
- **Significant Power Reduction Compared to LS-TTL Logic ICs**

**CD54HC373 . . . F PACKAGE**
**CD74HC373 . . . E OR M PACKAGE**
**(TOP VIEW)**




## description/ordering information

The ’HC373 devices are octal transparent D-type latches designed for 2-V to 6-V $V_{CC}$ operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

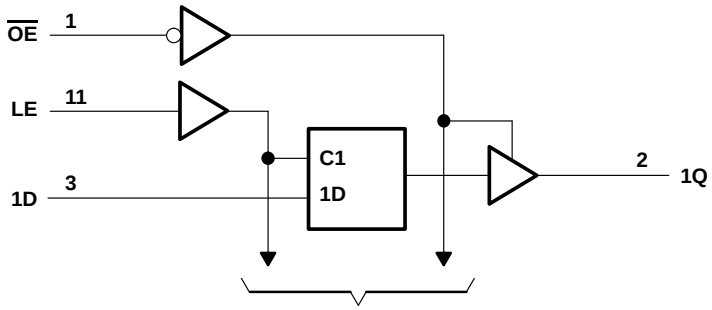
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –55°C to 125°C | PDIP – E | Tube | CD74HC373E | CD74HC373E |
| | SOIC – M | Tube | CD74HC373M | HC373M |
| | | Tape and reel | CD74HC373M96 | |
| | CDIP – F | Tube | CD54HC373F3A | CD54HC373F3A |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output drain current per output, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±35 mA
Continuous output source or sink current per output, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package . . . . . 69°C/W
M package . . . . . 58°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | |
| | | $V_{CC}$ = 6 V | 4.2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | | 1.35 | |
| | | $V_{CC}$ = 6 V | | 1.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $t_t$ | Input transition (rise and fall) time | $V_{CC}$ = 2 V | | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | | 500 | |
| | | $V_{CC}$ = 6 V | | 400 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 µA | 2 V | 1.9 | | 1.9 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | | 5.9 | | 5.9 | | |
| | | $I_{OH}$ = –6 mA | 4.5 V | 3.98 | | 3.7 | | 3.84 | | |
| | | $I_{OH}$ = –7.8 mA | 6 V | 5.48 | | 5.2 | | 5.34 | | |
| $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 6 mA | 4.5 V | | 0.26 | | 0.4 | | 0.33 | |
| | | $I_{OL}$ = 7.8 mA | 6 V | | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | | 6 V | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or 0 | | 6 V | | ±0.5 | | ±10 | | ±5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0, | $I_O$ = 0 | 6 V | | 8 | | 160 | | 80 | µA |
| $C_i$ | | | | | 10 | | 10 | | 10 | pF |
| $C_o$ | | | | | 20 | | 20 | | 20 | pF |

### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | $V_{CC}$ | $T_A$ = 25°C | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 2 V | 80 | | 120 | | 100 | | ns |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| $t_{su}$ | Setup time, data before LE↓ | 2 V | 50 | | 75 | | 65 | | ns |
| | | 4.5 V | 10 | | 15 | | 13 | | |
| | | 6 V | 9 | | 13 | | 11 | | |
| $t_h$ | Hold time, data after LE↓ | 2 V | 5 | | 5 | | 5 | | ns |
| | | 4.5 V | 5 | | 5 | | 5 | | |
| | | 6 V | 5 | | 5 | | 5 | | |

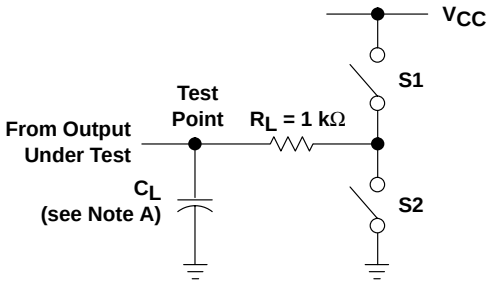
### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $V_{CC}$ | $T_A$ = 25°C | | $T_A$ = –55°C TO 125°C | | $T_A$ = –40°C TO 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | $C_L$ = 50 pF | 2 V | | 150 | | 225 | | 190 | ns |
| | | | | 4.5 V | | 30 | | 45 | | 38 | |
| | | | | 6 V | | 26 | | 38 | | 33 | |
| | LE | Q | $C_L$ = 50 pF | 2 V | | 175 | | 265 | | 220 | |
| | | | | 4.5 V | | 35 | | 53 | | 44 | |
| | | | | 6 V | | 30 | | 45 | | 37 | |
| $t_{en}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | 2 V | | 150 | | 225 | | 190 | ns |
| | | | | 4.5 V | | 30 | | 45 | | 38 | |
| | | | | 6 V | | 26 | | 38 | | 33 | |
| $t_{dis}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | 2 V | | 150 | | 225 | | 190 | ns |
| | | | | 4.5 V | | 30 | | 45 | | 38 | |
| | | | | 6 V | | 26 | | 38 | | 33 | |
| $t_t$ | | Q | $C_L$ = 50 pF | 2 V | | 60 | | 90 | | 75 | ns |
| | | | | 4.5 V | | 12 | | 18 | | 15 | |
| | | | | 6 V | | 10 | | 15 | | 13 | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

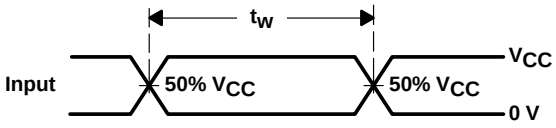
| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | 51 | pF |

## PARAMETER MEASUREMENT INFORMATION

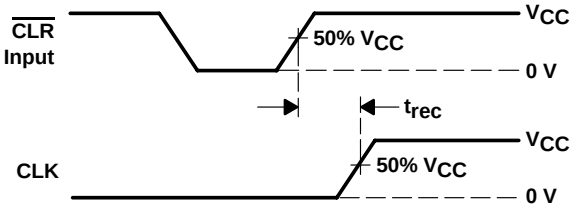



LOAD CIRCUIT

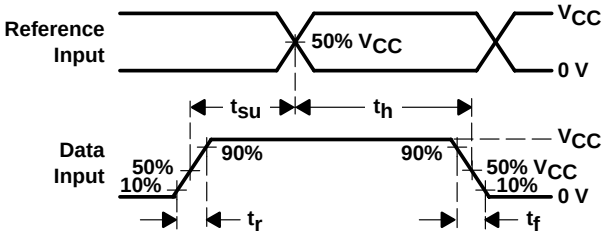
| PARAMETER | | S1 | S2 |
|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | Open | Closed |
| | $t_{PZL}$ | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | Open | Closed |
| | $t_{PLZ}$ | Closed | Open |
| $t_{pd}$ or $t_t$ | | Open | Open |



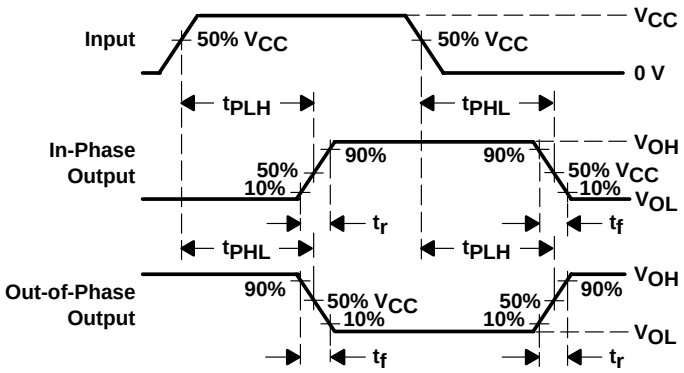

VOLTAGE WAVEFORMS
PULSE DURATION



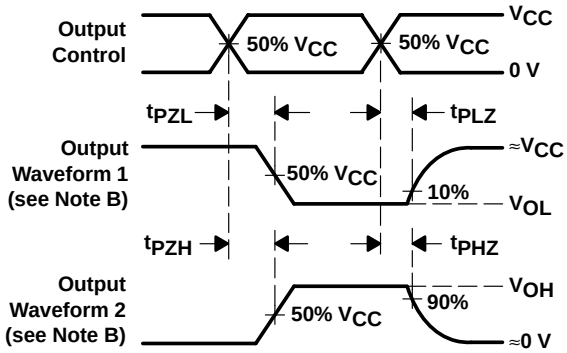

VOLTAGE WAVEFORMS
RECOVERY TIME




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES




VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
D. For clock inputs, $f_{max}$ is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
H. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
I. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD54HC373F | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD54HC373F | Samples |
| CD54HC373F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8407201RA CD54HC373F3A | Samples |
| CD74HC373E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC373E | Samples |
| CD74HC373EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC373E | Samples |
| CD74HC373M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC373M | Samples |
| CD74HC373M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC373M | Samples |
| CD74HC373ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC373M | Samples |
| CD74HC373MG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC373M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC373, CD74HC373 :**

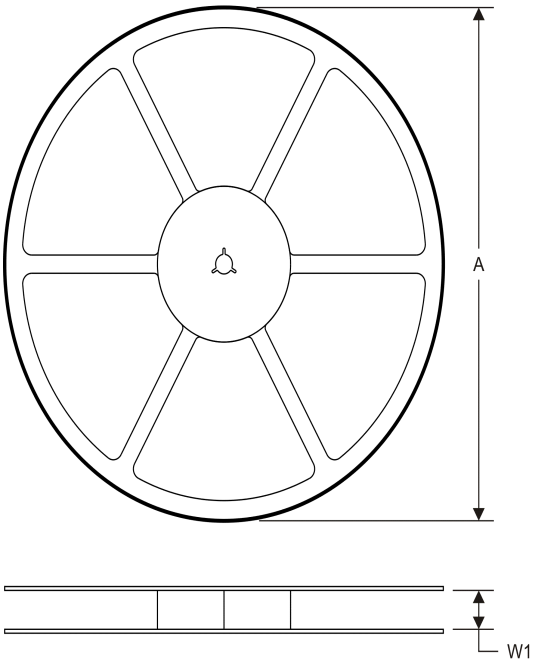
- Catalog: CD74HC373
- Military: CD54HC373

NOTE: Qualified Version Definitions:

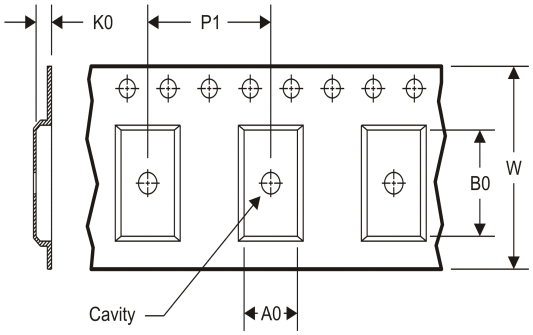
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

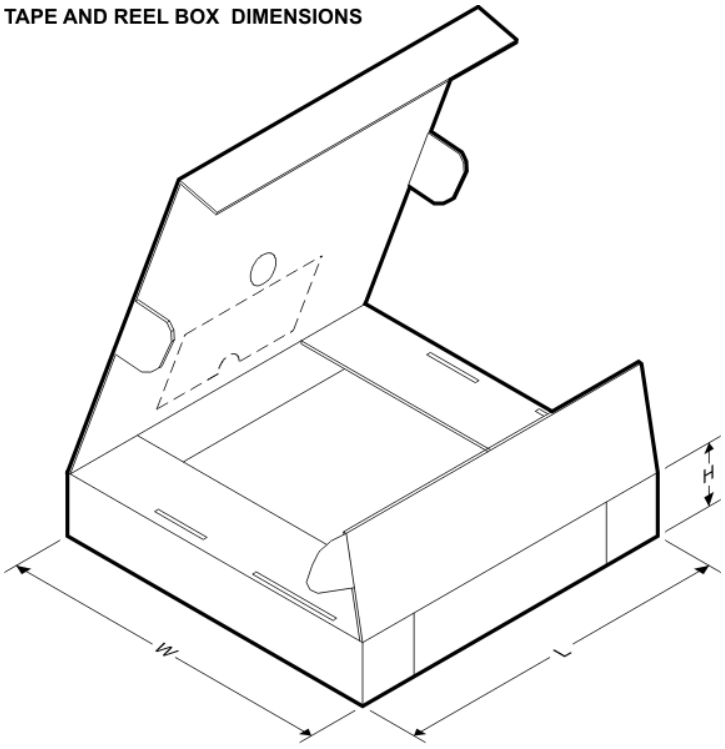
### TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC373M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**

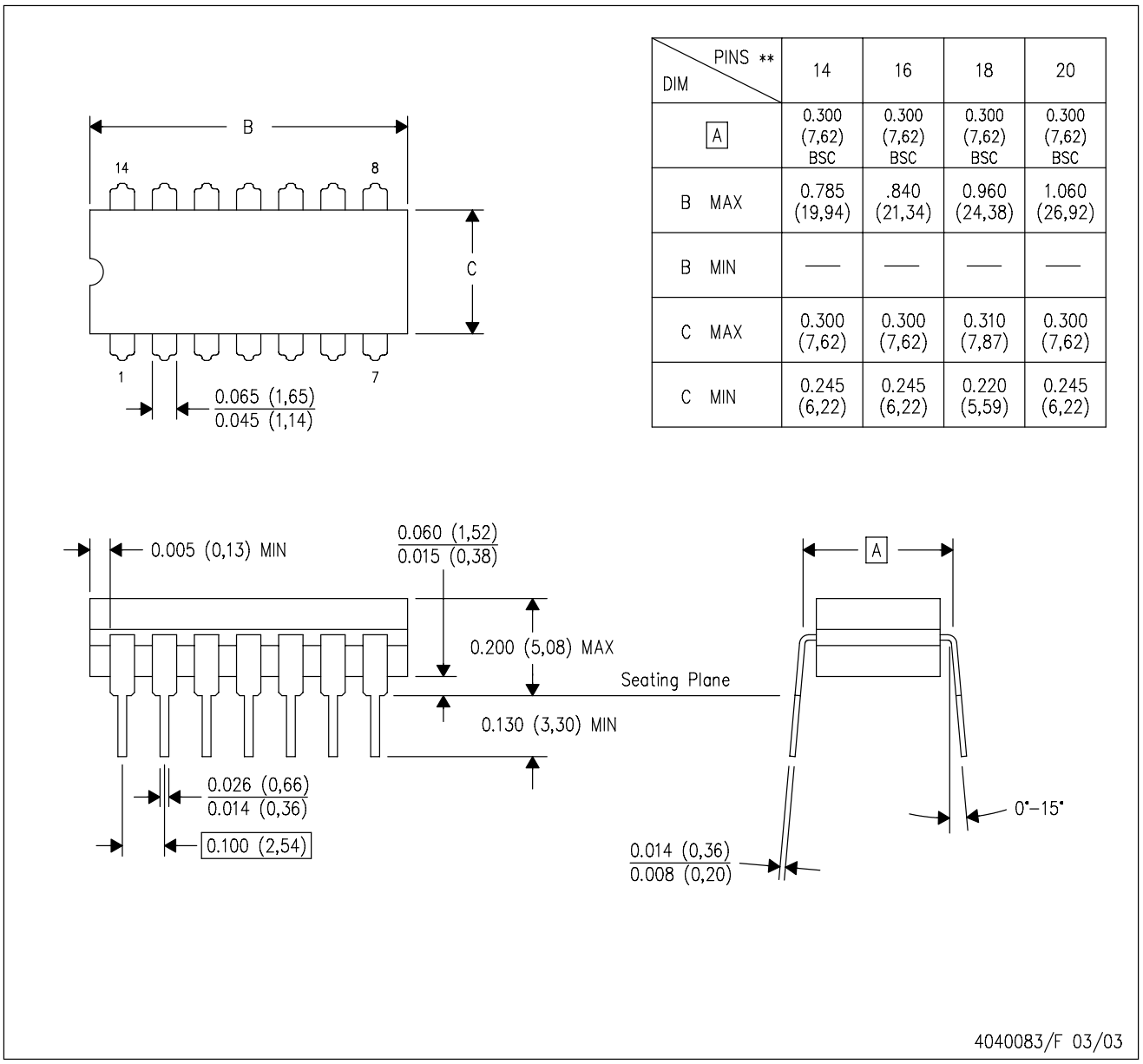



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC373M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

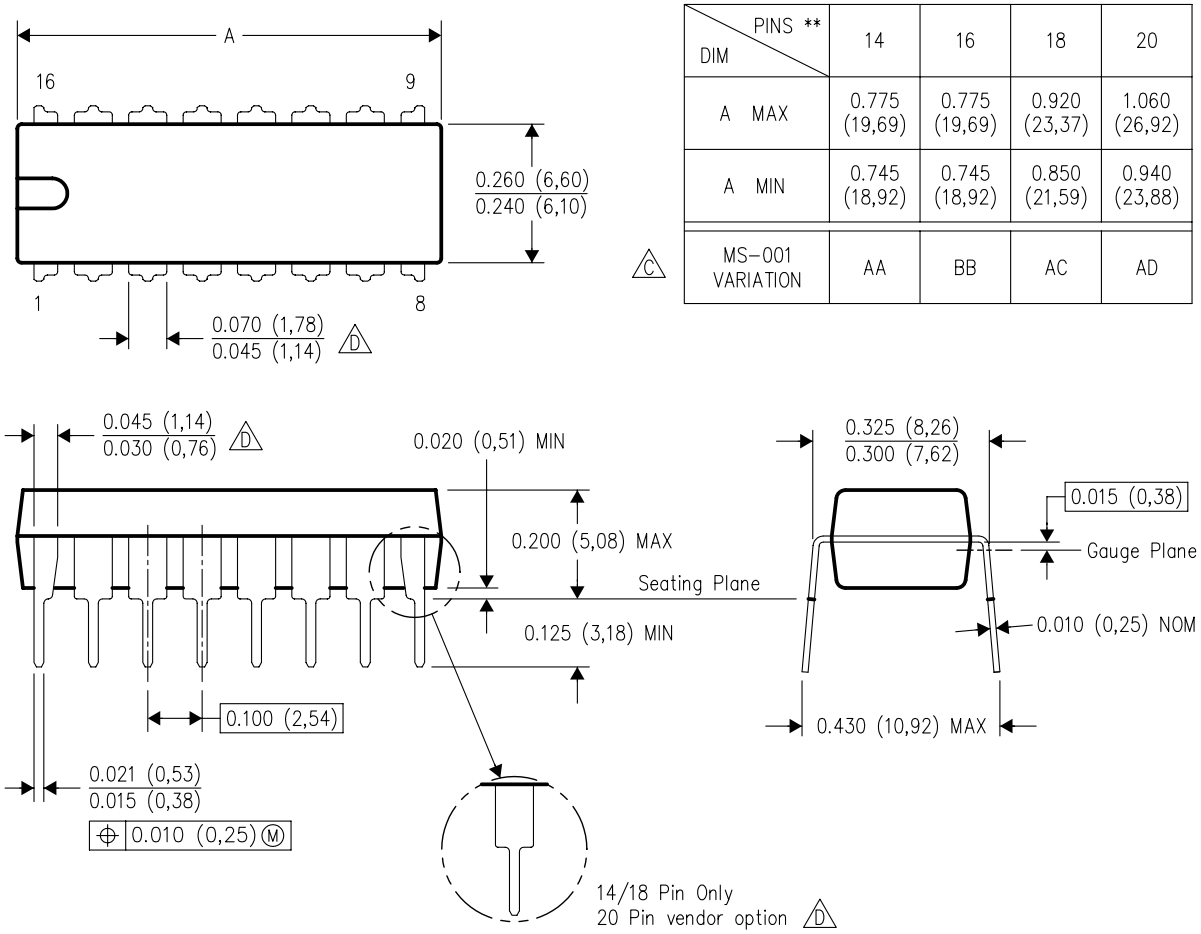
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

## MECHANICAL DATA

### N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

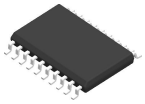
16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION | AA | BB | AC | AD |

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

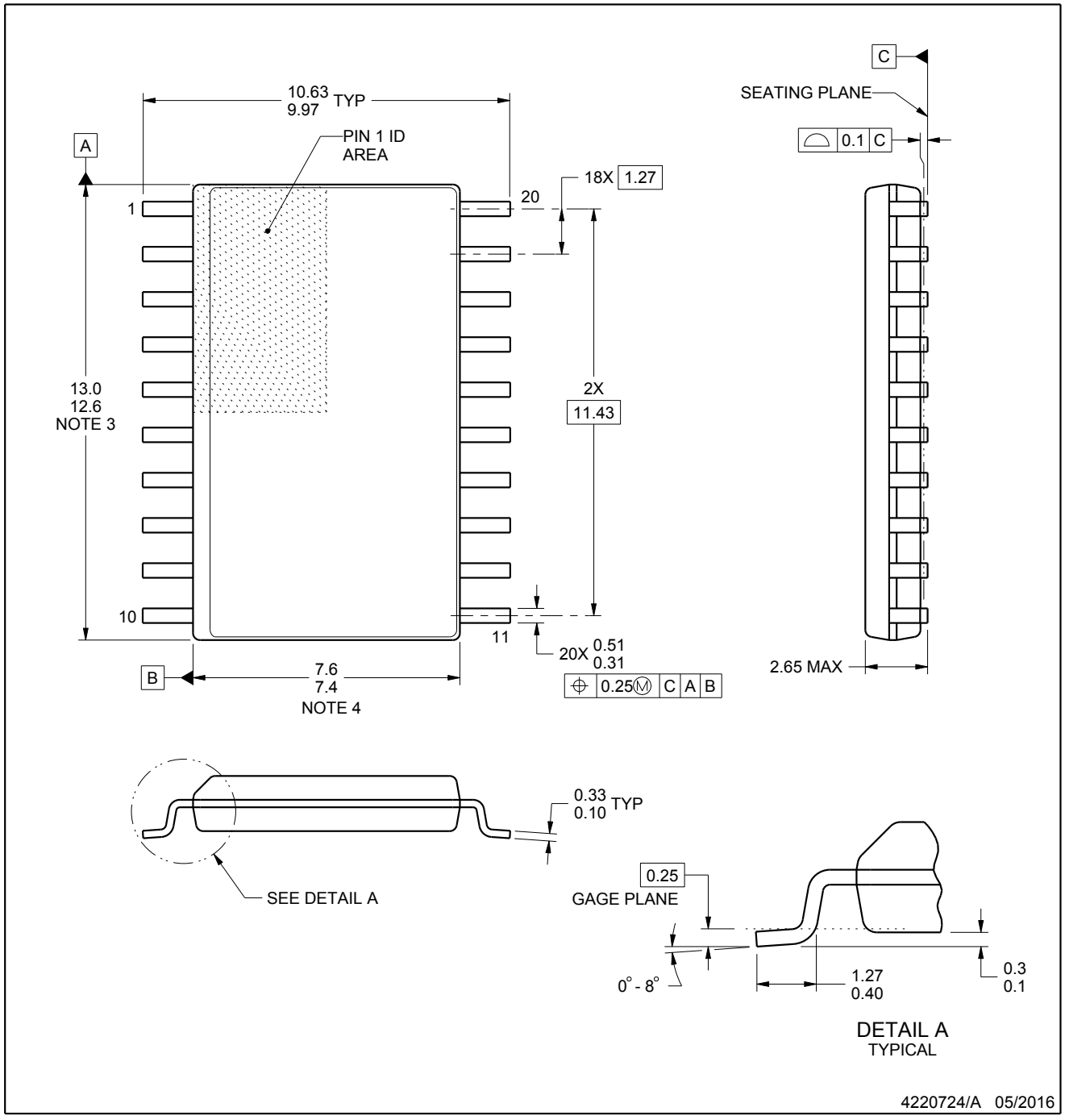


# PACKAGE OUTLINE

## DW0020A

## SOIC - 2.65 mm max height

SOIC




NOTES:

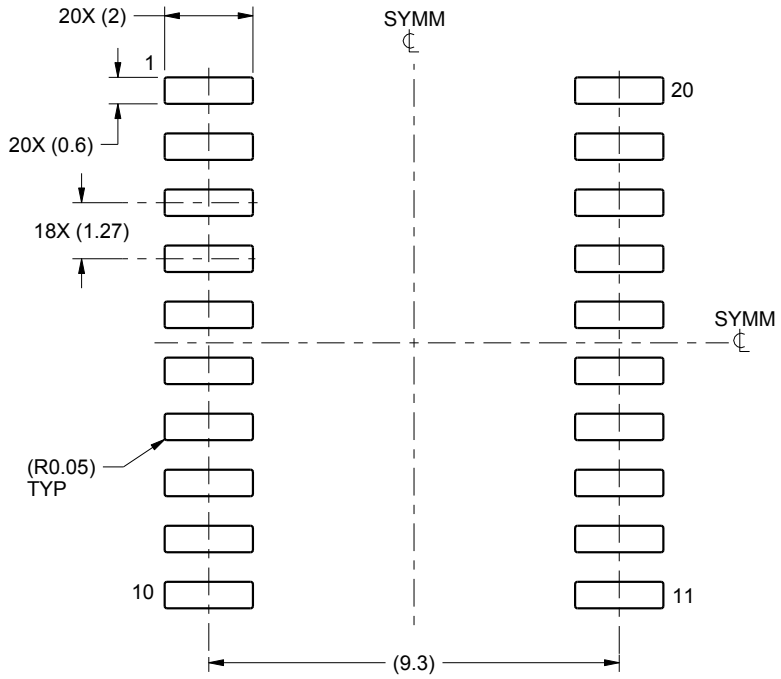
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

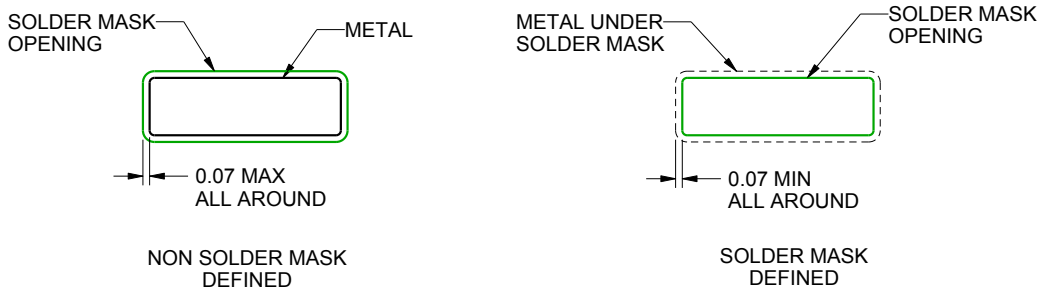
## DW0020A

### SOIC - 2.65 mm max height

SOIC




LAND PATTERN EXAMPLE
SCALE:6X




SOLDER MASK DETAILS

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NOTES: (continued)

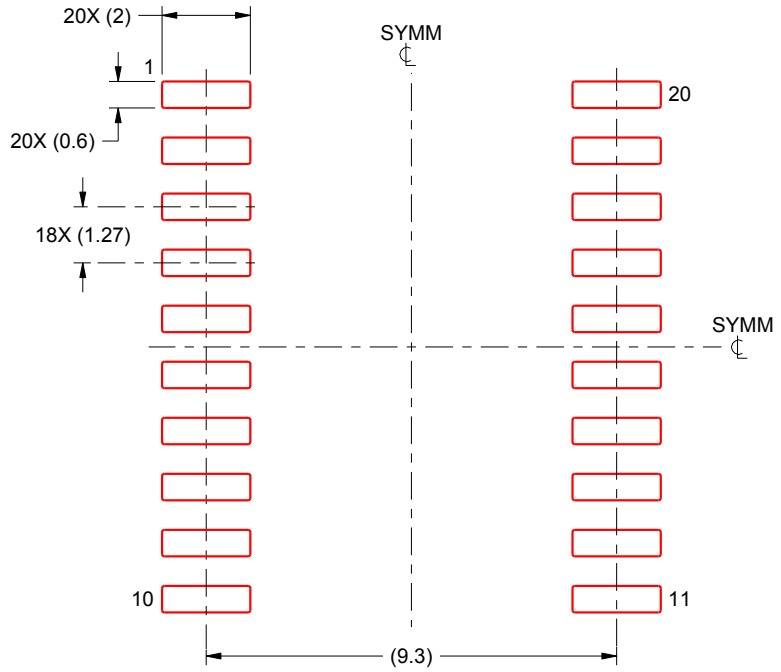
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DW0020A

## SOIC - 2.65 mm max height

SOIC




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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