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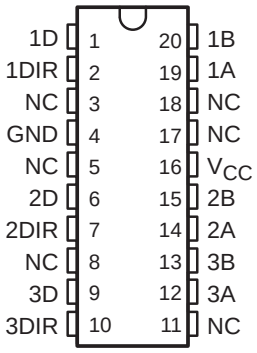
SN75ALS170, SN75ALS170A
TRIPLE DIFFERENTIAL BUS TRANSCEIVER

SLLS055D – AUGUST 1987 – REVISED SEPTEMBER 1995

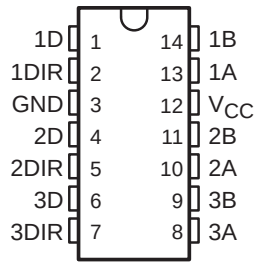
- Three Bidirectional Transceivers
- Driver Meets or Exceeds ANSI Standard EIA/TIA-422-B and RS-485 and ITU Recommendation V.11
- Two Skew Limits Available
- Designed to Operate Up to 20 Million Data Transfers per Second (FAST-20 SCSI)
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operate From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Feature Independent Direction Controls for Each Channel

DW PACKAGE
(TOP VIEW)



NC – No internal connection

J PACKAGE
(TOP VIEW)



description

The SN75ALS170 and SN75ALS170A triple differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets ANSI Standards EIA/TIA-422-B and RS-485 and both the driver and receiver meet ITU Recommendation V.11. The SN75ALS170A is designed for FAST-20 SCSI and can transmit or receive data pulses as short as 30 ns with a maximum skew of 5 ns.

The SN75ALS170 and SN75ALS170A operate from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which are internally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS170 and the SN75ALS170A are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SKEW LIMIT	PART NUMBER	
10 ns	SN75ALS170DW	SN75ALS170J
5 ns	SN75ALS170ADW	

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Function Tables

EACH DRIVER

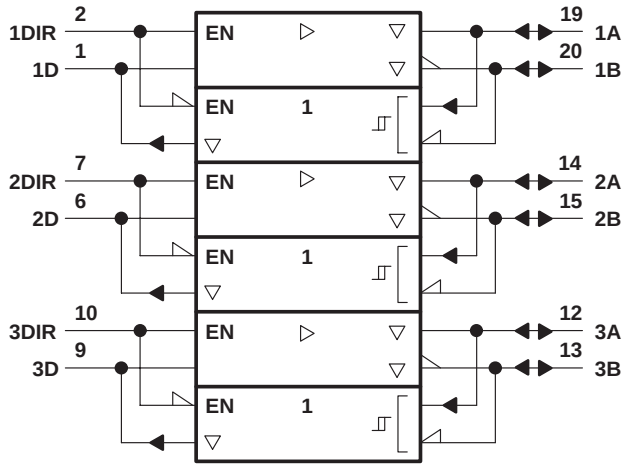
INPUT D	DIR	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	DIR	OUTPUT R
$V_{ID} \geq 0.3$ V	L	H
-0.3 V $< V_{ID} < 0.3$ V	L	?
$V_{ID} \leq -0.3$ V	L	L
X	H	Z
Open	L	H

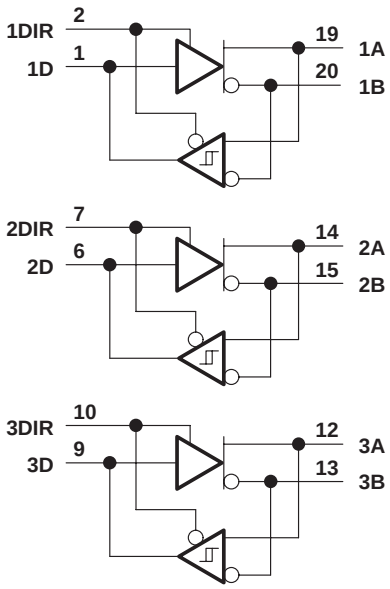
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†

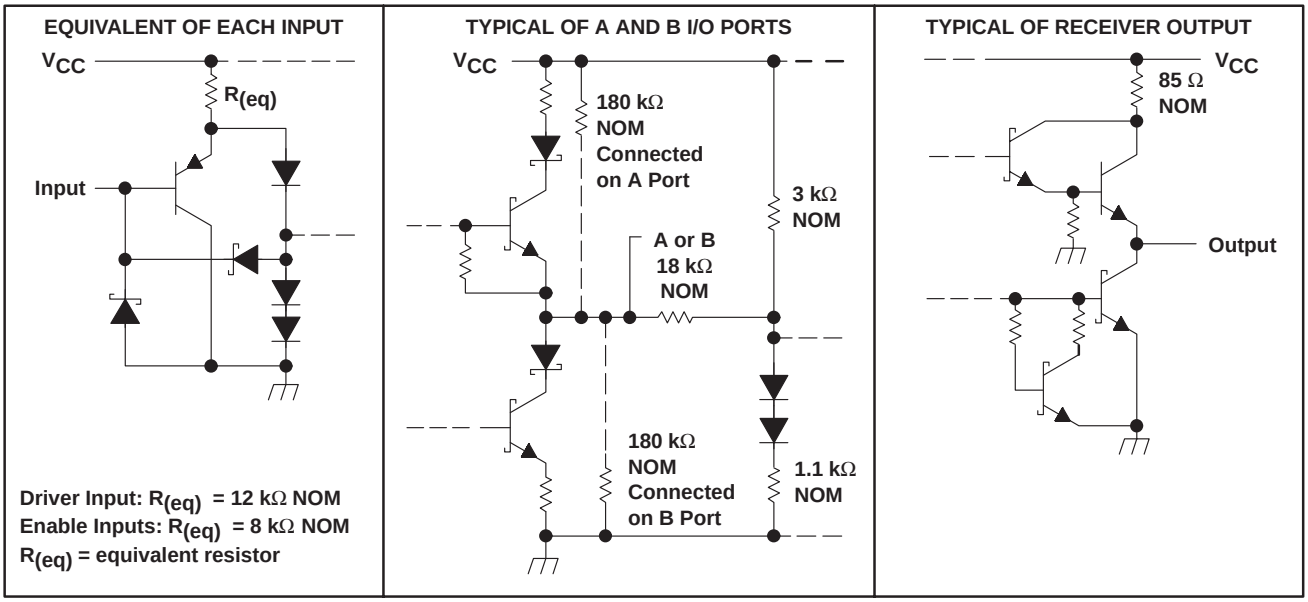


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW package.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage range at any bus terminal . . . . . –7 V to 12 V
Enable input voltage, V_I . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				–7	
High-level input voltage, V_{IH}	D, DIR	2			V
Low-level input voltage, V_{IL}	D, DIR			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			–60	mA
	Receiver			–400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –19 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = –55 mA	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 55 mA			1.7	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2§			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = –7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage¶	R_L = 540 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
						–1	
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current	V_O = –6 V				–250	mA
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
¶ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	ALS170	R_L = 54 Ω, T_A =25°C,	C_L = 50 pF, See Figure 3	3	8	13	ns
		ALS170A			5.5	8	10.5	
		ALS170	$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF, See Figure 4	R_{L2} = 75 Ω, T_A =25°C,	3	8	13	
		ALS170A			5.5	8	10.5	
$t_{sk(p)}$	Pulse skew‡		R_L = 54 Ω, See Figure 3	C_L = 50 pF,		1	5	ns
			$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 4		1	5	ns
$t_{sk(lim)}$	Skew limit§	ALS170	R_L = 54 Ω, See Figure 3	C_L = 50 pF,			10	ns
		ALS170A					5	
		ALS170	$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 4			10	
		ALS170A					5	
$t_{t(OD)}$	Differential-output transition time		R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
			$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 4	3	8	13	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Pulse skew is defined as the $|t_{d(ODH)} - t_{d(ODL)}|$ of each channel.
§ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_O	V_O
$\lvert VOD2 \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA			0.3	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	–0.3‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV, See Figure 5	I_{OH} = –400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –300 mV, See Figure 5	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 2.4 V				20	µA
		V_O = 0.4 V				–400	
I_I	Line input current	Other input = 0, See Note 4	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				–100	µA
r_I	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 300 mV,	V_O = 0	–15		–85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	ALS170	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, T_A = 25°C, See Figure 6	9		19	ns
		ALS170A		11.5		16.5	
t_{PHL}	Propagation delay time, high-to-low-level output	ALS170		9		19	ns
		ALS170A		11.5		16.5	
$t_{sk(p)}$	Pulse skew§	ALS170	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 6		2	6	ns
		ALS170A				5	
$t_{sk(lim)}$	Skew limit¶	ALS170				10	ns
		ALS170A				5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.
¶ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION

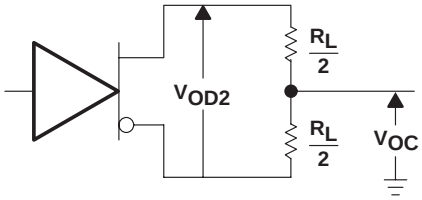


Figure 1. Driver V_{OD} and V_{OC}

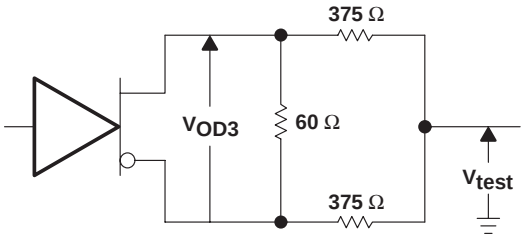
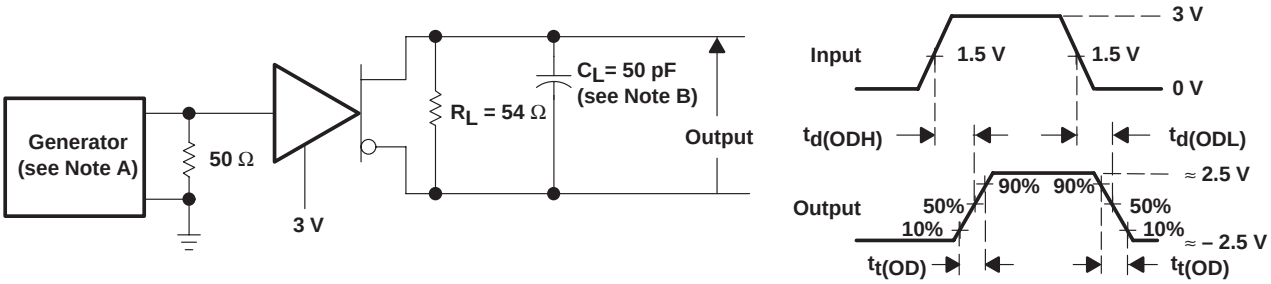


Figure 2. Driver V_{OD3}

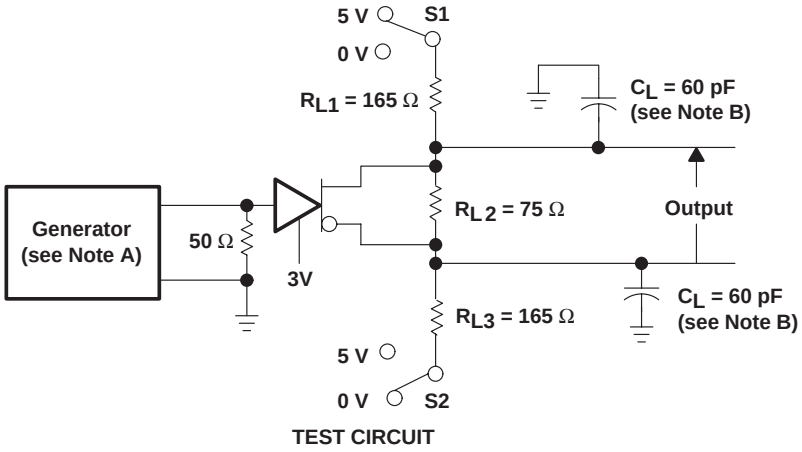


TEST CIRCUIT **VOLTAGE WAVEFORMS**

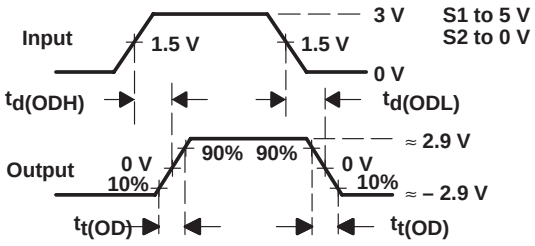
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

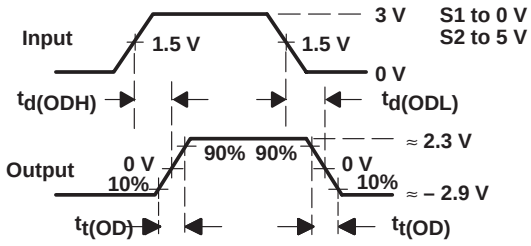
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms With Double-Differential-SCSI Termination for the Load

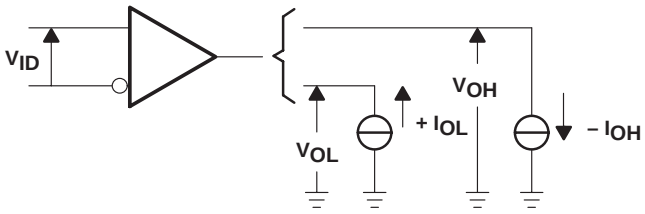
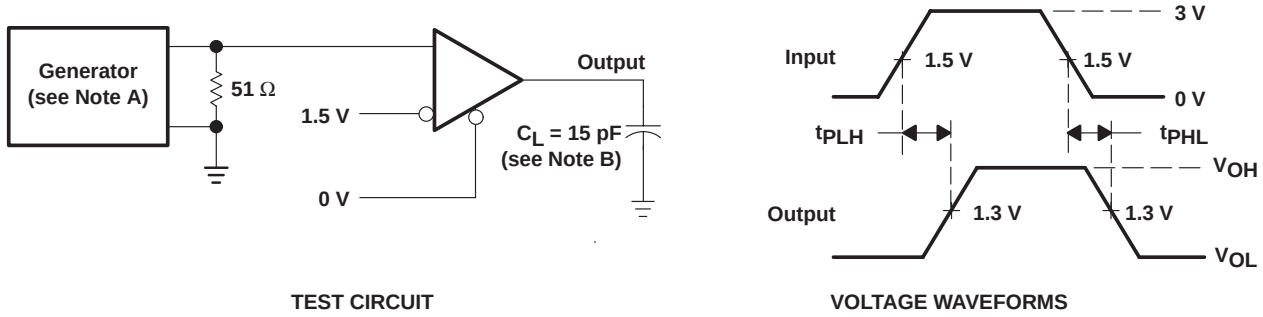


Figure 5. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

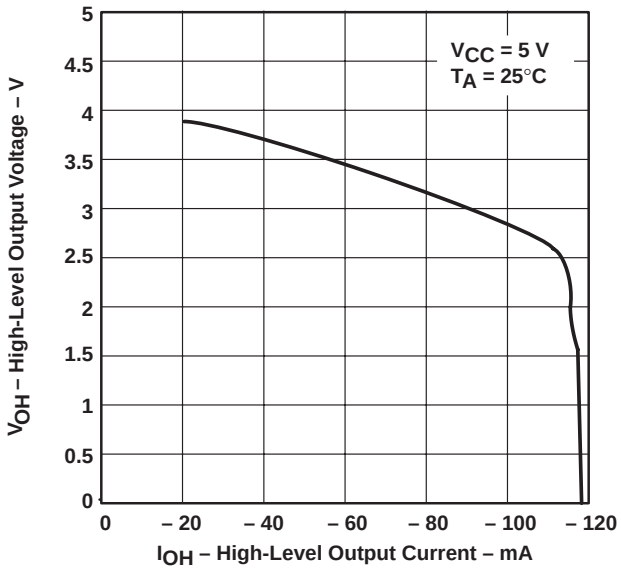


Figure 7

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

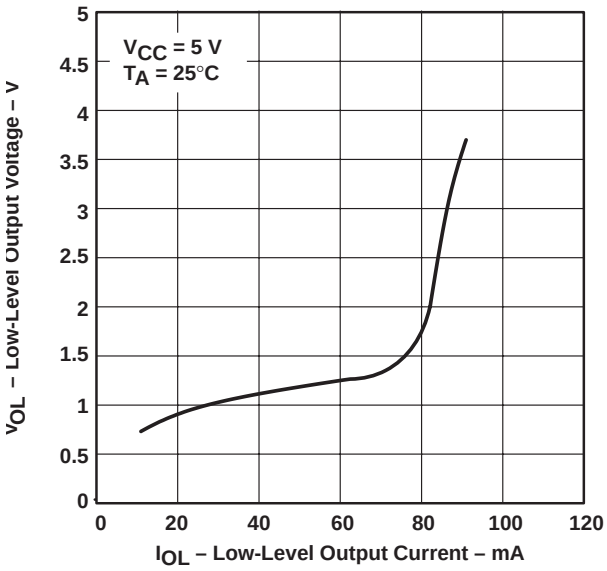


Figure 8

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

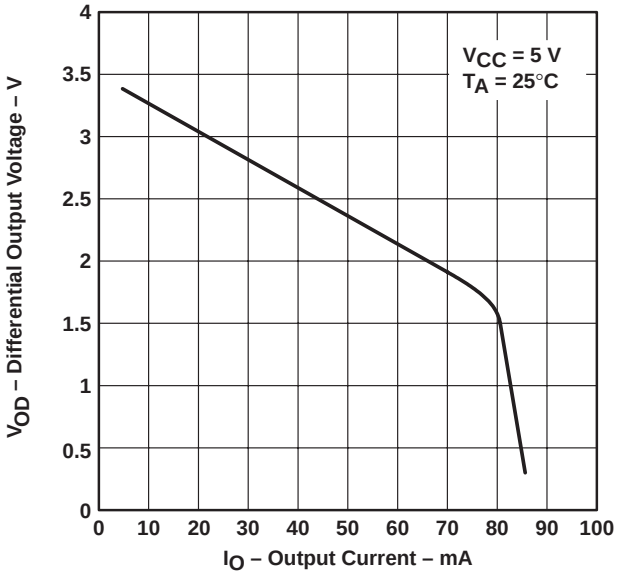


Figure 9

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

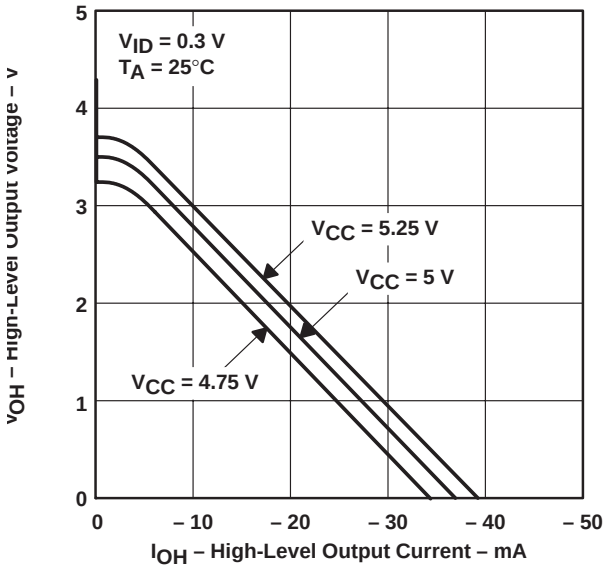


Figure 10

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

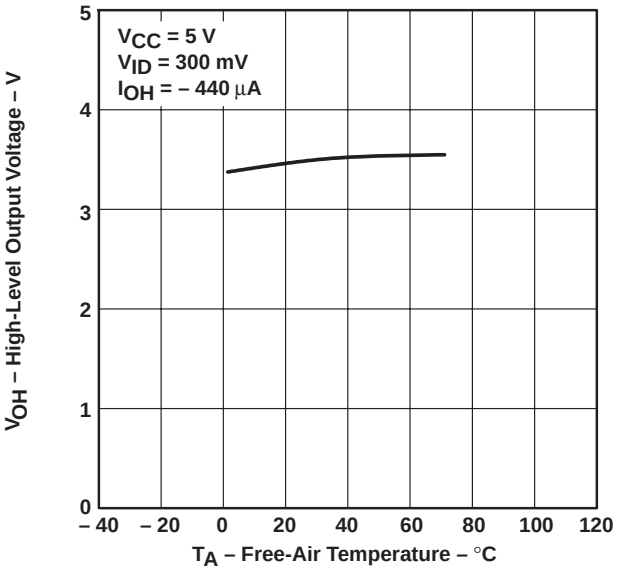


Figure 11

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

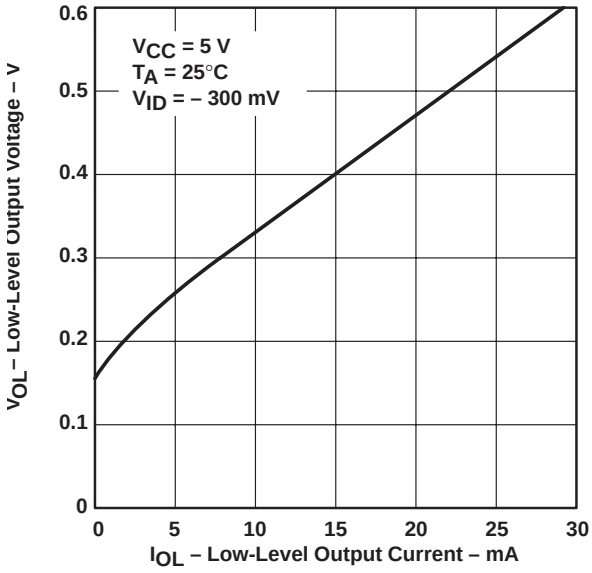


Figure 12

TYPICAL CHARACTERISTICS

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

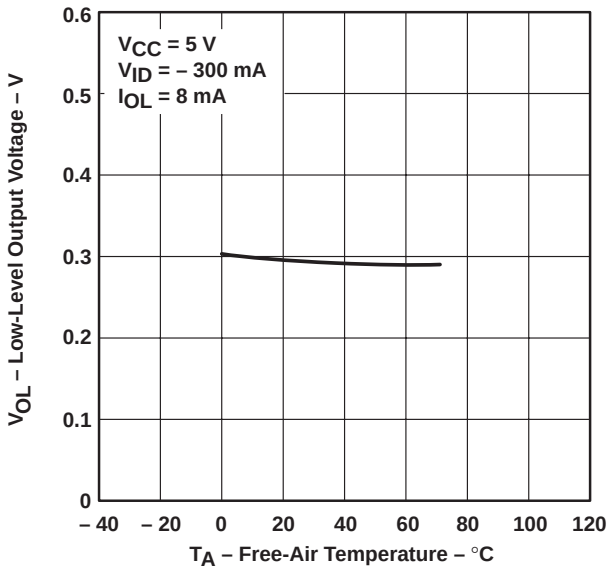


Figure 13

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

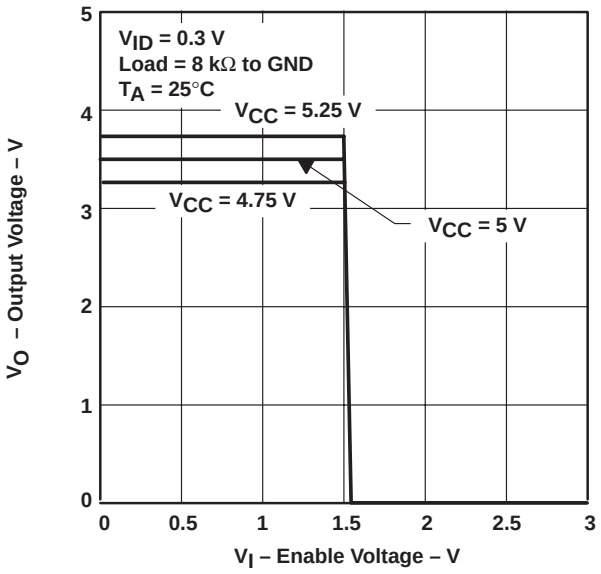


Figure 14

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

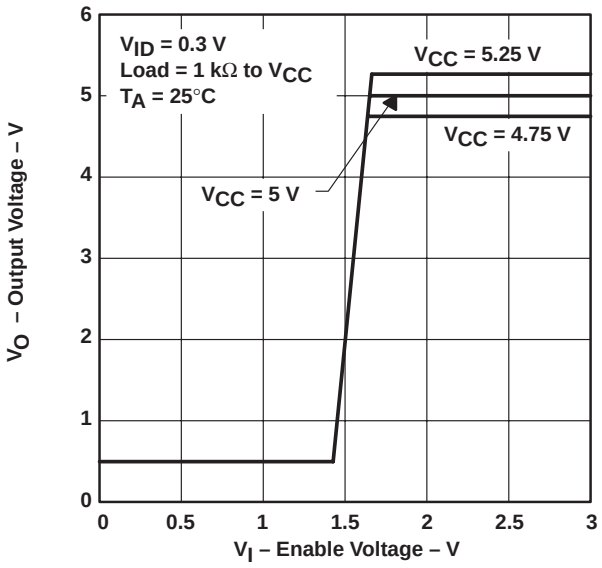
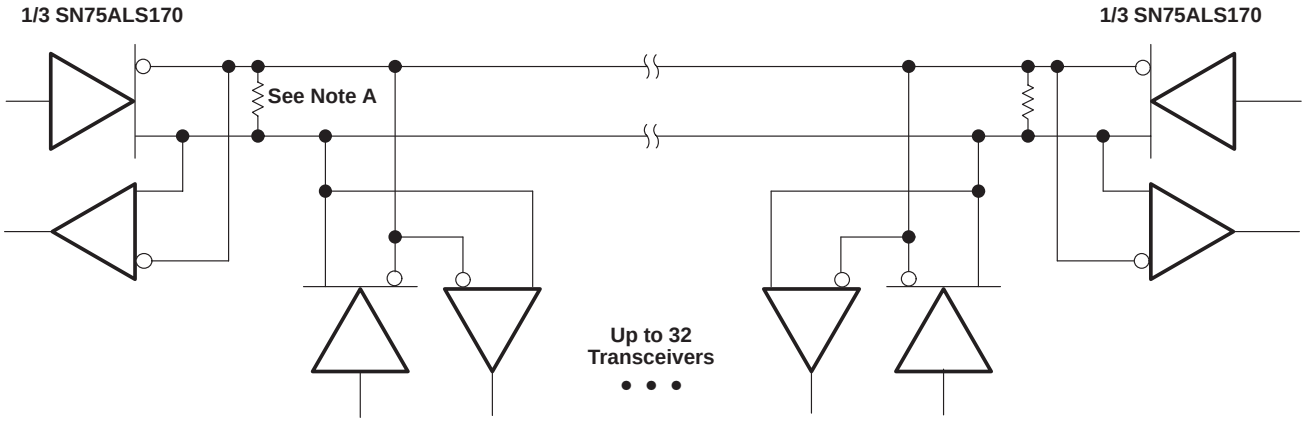


Figure 15

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 16. Typical Application Circuit

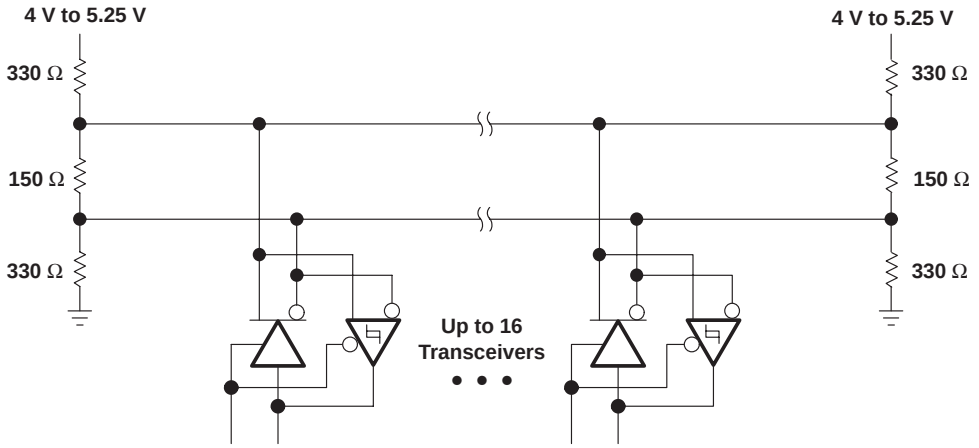


Figure 17. Typical Differential SCSI Application Circuit

APPLICATION INFORMATION

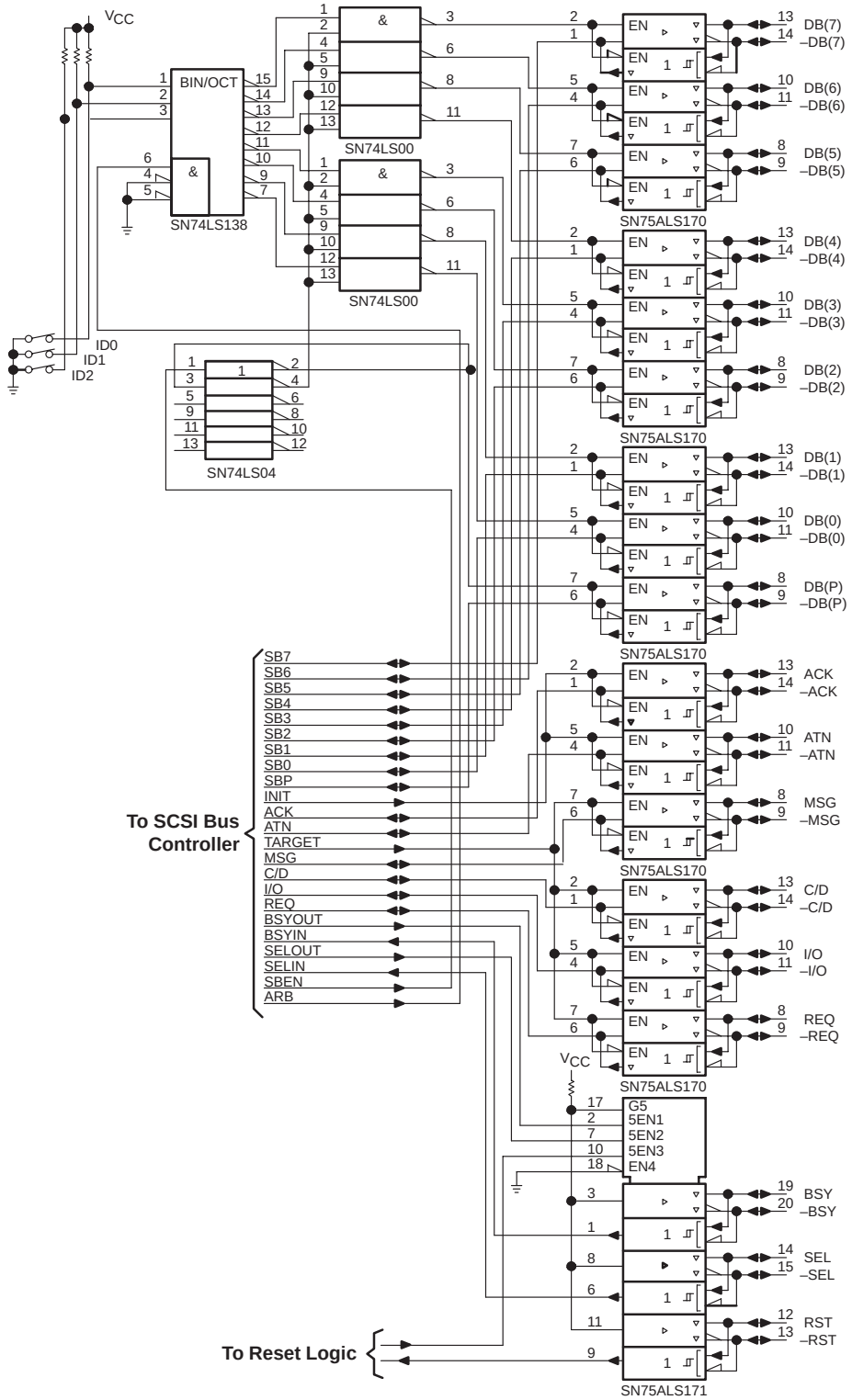


Figure 18. Typical Differential SCSI Bus Interface Implementation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS170ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170A	Samples
SN75ALS170ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170A	Samples
SN75ALS170DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170	Samples
SN75ALS170DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170	Samples
SN75ALS170DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170	Samples
SN75ALS170DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS170	Samples
SN75ALS170J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

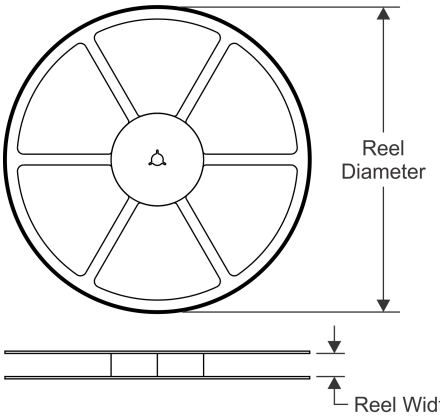
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

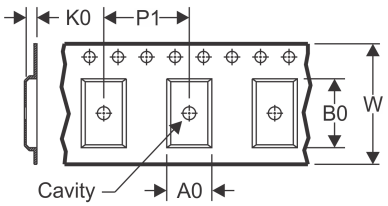
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

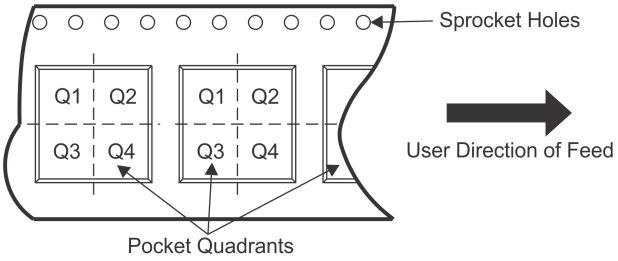


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

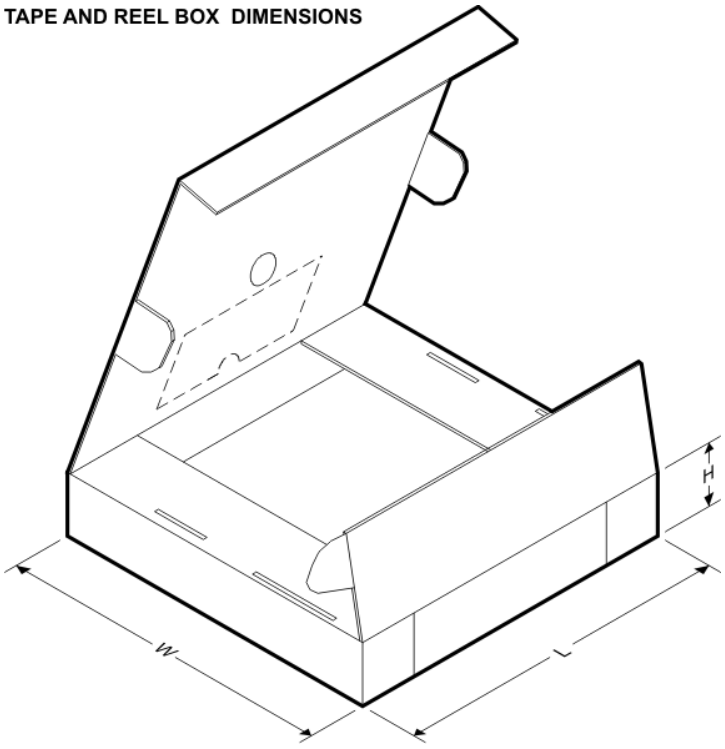


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS170ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75ALS170DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

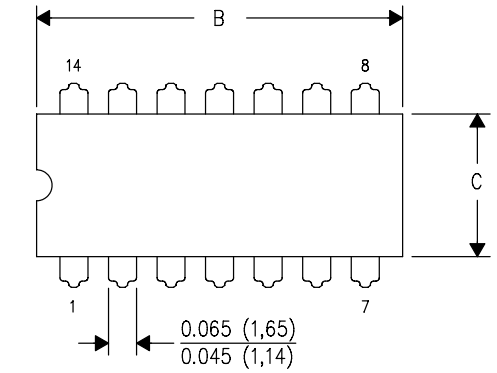


*All dimensions are nominal

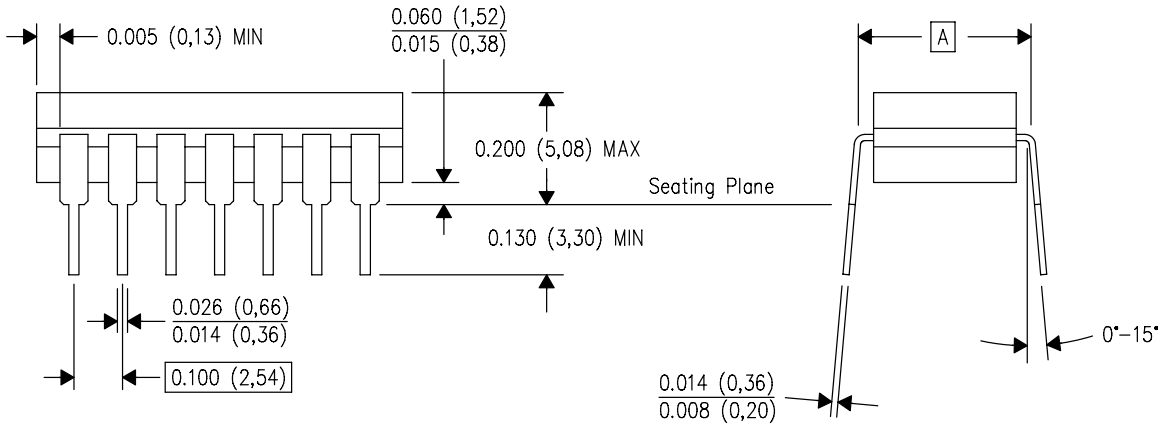
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS170ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75ALS170DWR	SOIC	DW	20	2000	367.0	367.0	45.0

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN

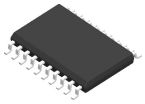


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

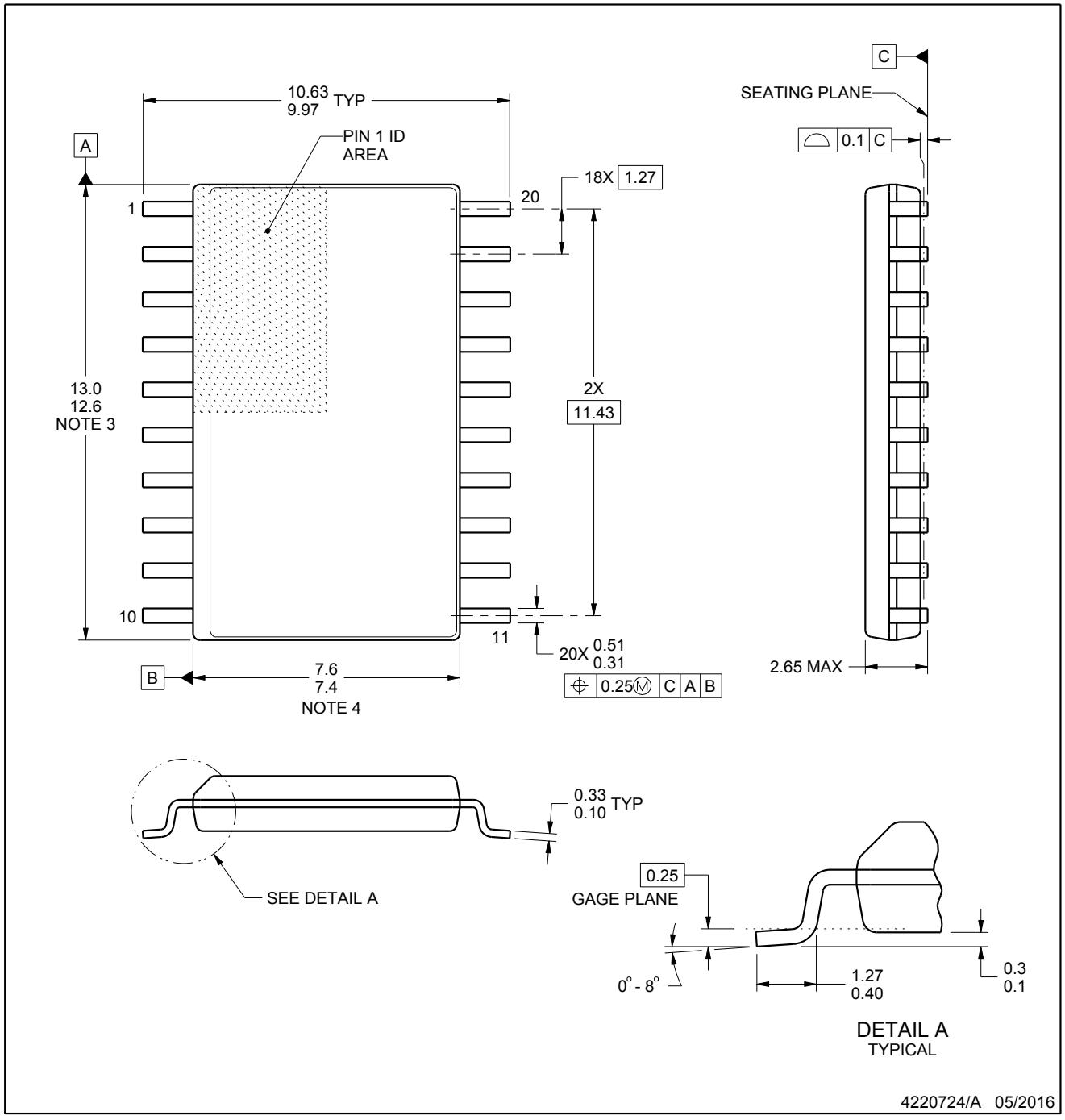


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



NOTES:

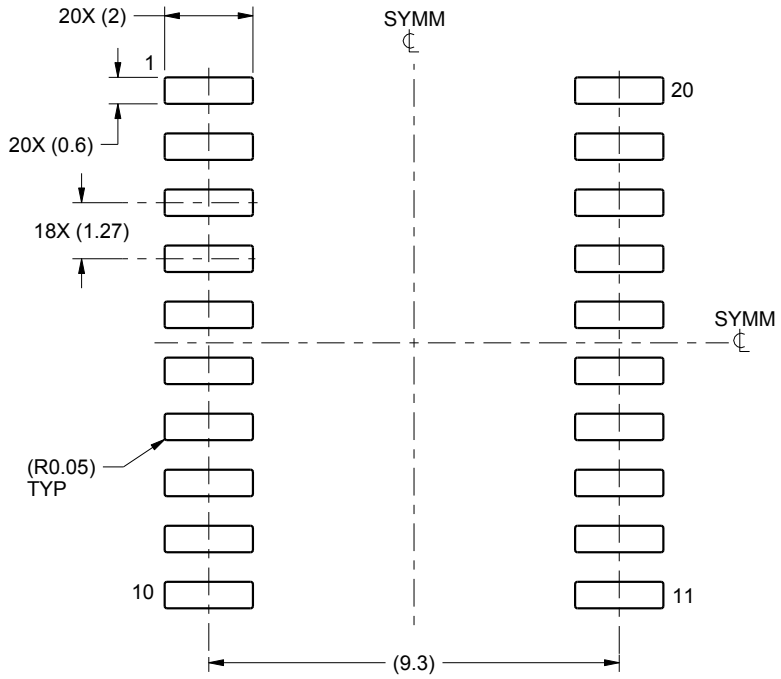
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

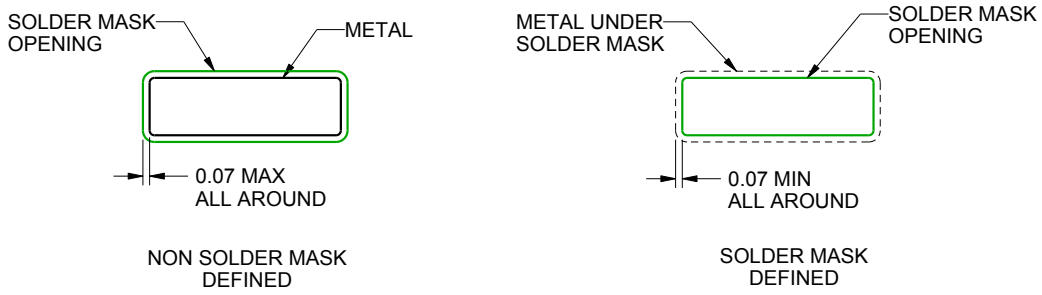
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

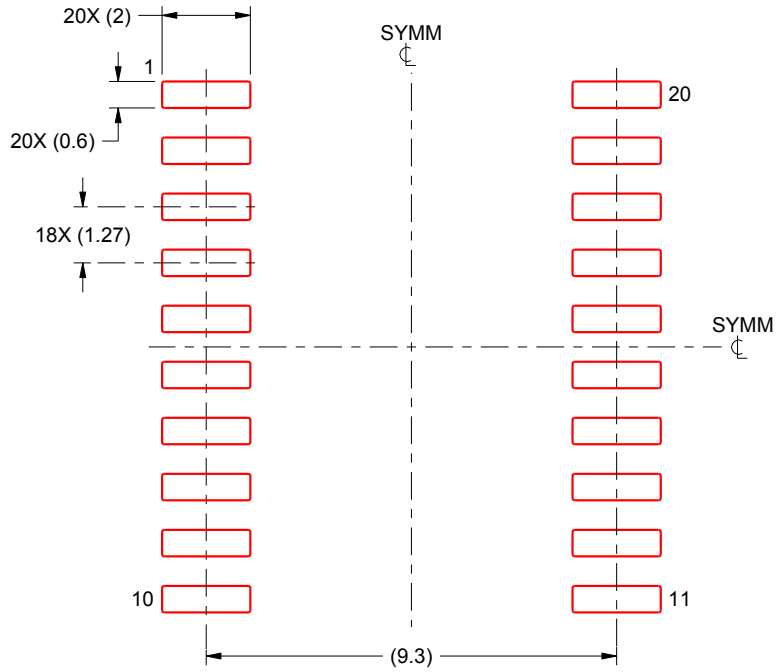
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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