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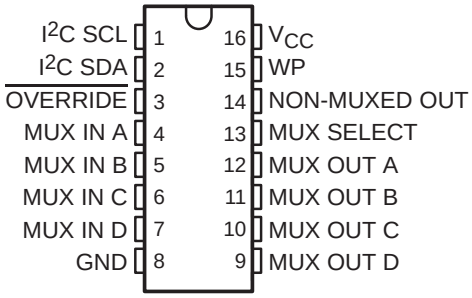
PCA8550
NONVOLATILE 5-BIT REGISTER WITH I²C INTERFACE

SCPS050A – MARCH 1999 – REVISED APRIL 1999

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Useful for Jumperless Configuration of PC Motherboard
- Inputs Accept Voltages to 5.5 V
- MUX OUT Signals are 2.5-V Outputs
- NON-MUXED OUT Signal is a 3.3-V Output
- Minimum of 1000 Write Cycles
- Minimum of 10 Years Data Retention
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 4-bit 1-of-2 multiplexer with I²C input interface is designed for 3-V to 3.6-V V_{CC} operation.

The PCA8550 is designed to multiplex four bits of data from parallel inputs or from I²C input data stored in a nonvolatile register. An additional bit of register output also is provided, which is latched to prevent changes in the output value during the write cycle. The factory default for the contents of the register is all low. These stored values can be read from, or written to, using the I²C bus. The ability to control writing to the register is provided by the write protect (WP) input. The override ($\overline{\text{OVERRIDE}}$) input forces all the register outputs to a low.

This device provides a fast-mode (400 kbit/s) or standard-mode (100 kbit/s) I²C serial interface for data input and output. The implementation is as a slave. The device address is specified in the I²C interface definition table. Both of the I²C Schmitt-trigger inputs (SCL and SDA) provide integrated pullup resistors and are 5-V tolerant.

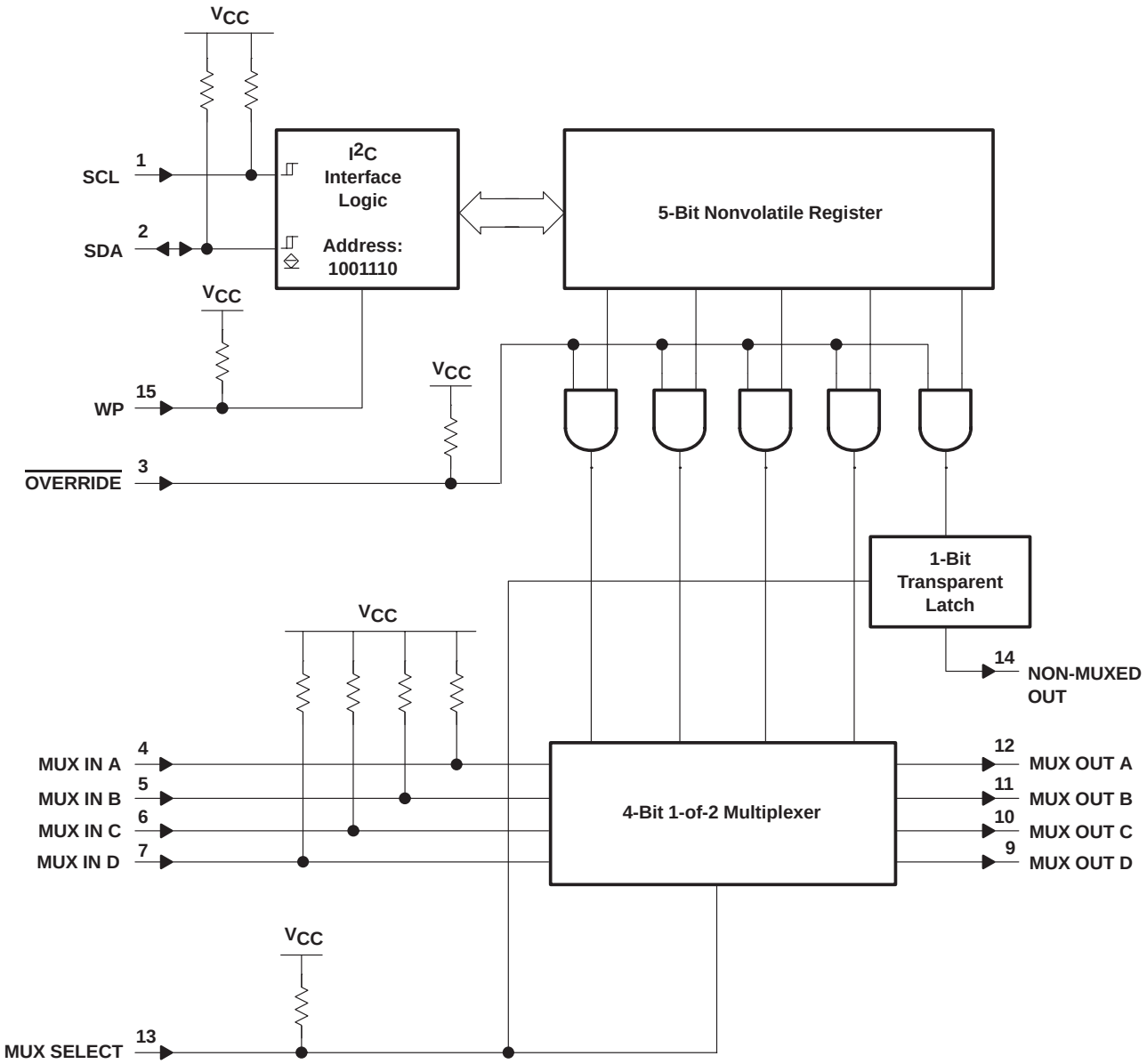
The PCA8550 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS	
MUX SELECT	$\overline{\text{OVERRIDE}}$	MUX OUT	NON-MUXED OUT
L	L	L	L
L	H	Nonvolatile register	Nonvolatile register
H	X	MUX IN	Latched NON-MUXED OUT†

† The latched NON-MUXED OUT state is the value present on the NON-MUXED OUT output at the time the MUX SELECT input transitions from the low to the high state.

logic diagram (positive logic)



I²C interface

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the serial data (SDA) input/output while the serial clock (SCL) input is high. After the start condition, the device address byte is sent, MSB first, including the data-direction bit (R/$\overline{W}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA input/output during the high of the acknowledge-related clock pulse.

The data byte follows the address acknowledge. If the R/$\overline{W}$ bit is high, the data from this device are the values read from the nonvolatile register. If the R/$\overline{W}$ bit is low, the data are from the master, to be written into the register. A valid data byte is one in which the three high-order bits are low. The first valid data byte that is received is written into the register, following the stop condition. If an invalid data byte is received, it is acknowledged, but is not written into the register. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the master following the acknowledge, they are ignored by this device.

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master. If the WP input is low during the falling edge of the first valid data byte acknowledge on the SCL input and the R/$\overline{W}$ bit is low, the stop condition causes the I²C interface logic to write the data byte value into the nonvolatile register. Data are written only if complete bytes are received and acknowledged. Writing to the register takes time (t_{wr}), during which the device does not respond to its slave address. If the WP input is high, the I²C interface logic does not write to the register.

I²C INTERFACE DEFINITION TABLE

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Address	H	L	L	H	H	H	L	R/$\overline{W}$
Data	L	L	L	NON-MUXED OUT	MUX OUT D	MUX OUT C	MUX OUT B	MUX OUT A

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 6.5 V
Output voltage range, V_O (SDA) (see Note 1) . . . . . –0.5 V to 6.5 V
Output voltage range, V_O (MUX OUT outputs) (see Note 1) . . . . . –0.5 V to 2.9 V
Output voltage range, V_O (NON-MUXED OUT output) (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2) . . . . . –50 mA, +10 mA
Input/output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) (see Note 2) . . . . . ±15 mA
Continuous current through V_{CC} or GND . . . . . ±30 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 113°C/W
DB package . . . . . 131°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	SCL, SDA	2.7	4	V
		$\overline{\text{OVERRIDE}}$, MUX IN, MUX SELECT, WP	2	4	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.9	V
		$\overline{\text{OVERRIDE}}$, MUX IN, MUX SELECT, WP	–0.5	0.8	
I_{OH}	High-level output current	MUX OUT, NON-MUXED OUT		–2	mA
I_{OL}	Low-level output current	SDA		6	mA
		MUX OUT, NON-MUXED OUT		2	
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{\text{OVERRIDE}}$, MUX IN, MUX SELECT, WP		10	ns/V
T_A	Operating free-air temperature		0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA			–1.5		V
V_{hys}†	SCL, SDA				0.19		V
V_{OH}	MUX OUT	I_{OH} = –100 µA			2	2.625	V
		I_{OH} = –1 mA			1.7	2.625	
	NON-MUXED OUT	I_{OH} = –100 µA			2.4	3.6	
		I_{OH} = –2 mA			2	3.6	
V_{OL}	MUX OUT	I_{OL} = 100 µA			–0.3	0.4	V
		I_{OL} = 2 mA			–0.3	0.7	
	NON-MUXED OUT	I_{OL} = 100 µA			–0.5	0.4	
		I_{OL} = 2 mA			–0.5	0.7	
	SDA	I_{OL} = 3 mA				0.4	
		I_{OL} = 6 mA				0.6	
I_{IH}	SCL, SDA	V_{IH} = 2.4 V			–1.5	–12	µA
	$\overline{\text{OVERRIDE}}$, MUX SELECT, WP				–20	–100	
	MUX IN				–0.166	–0.75	mA
I_{IL}	SCL, SDA	V_{IL} = 0.4 V			–7	–32	µA
	$\overline{\text{OVERRIDE}}$, MUX SELECT, WP				–86	–267	
	MUX IN				–0.72	–2	mA
I_{CC}	During read or write cycle	V_I = 0 to V_{CC},	I_O = 0,	V_{CC} = 3.3 V		10	mA
	Not during read or write cycle	V_I = V_{CC},	I_O = 0			500	µA
C_i		V_I = V_{CC} or GND				10	pF

† V_{hys} is the hysteresis of Schmitt-trigger inputs.

nonvolatile storage specifications

PARAMETER	SPECIFICATIONS
Write time (t_{wr})	10 ms, typical
Memory-cell data retention	10 years, minimum
Maximum number of memory-cell write cycles	1000 cycles, minimum

I²C interface timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

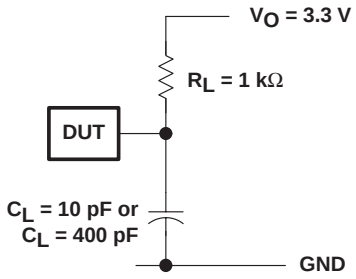
		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	
f_{scl}	I²C clock frequency	10	400	kHz
T_{sch}	I²C clock high time	600		ns
T_{scl}	I²C clock low time	1.3		µs
T_{sp}	I²C spike time	0	50	ns
T_{sds}	I²C serial data setup time	100		ns
T_{sdh}	I²C serial data hold time	0	900	ns
T_{icr}	I²C input rise time	20	300	ns
T_{icf}	I²C input fall time	20	300	ns
T_{ocf}	I²C output fall time (10-pF to 400-pF bus)	20 + 0.1 C_b†	250	ns
T_{buf}	I²C bus free time between stop and start	1.3		µs
T_{sts}	I²C start or repeated start condition setup	600		ns
T_{sth}	I²C start or repeated start condition hold	600		ns
T_{sps}	I²C stop condition setup	600		ns
C_b†	I²C bus capacitive load		400	pF

† C_b = capacitance of one bus line in pF.

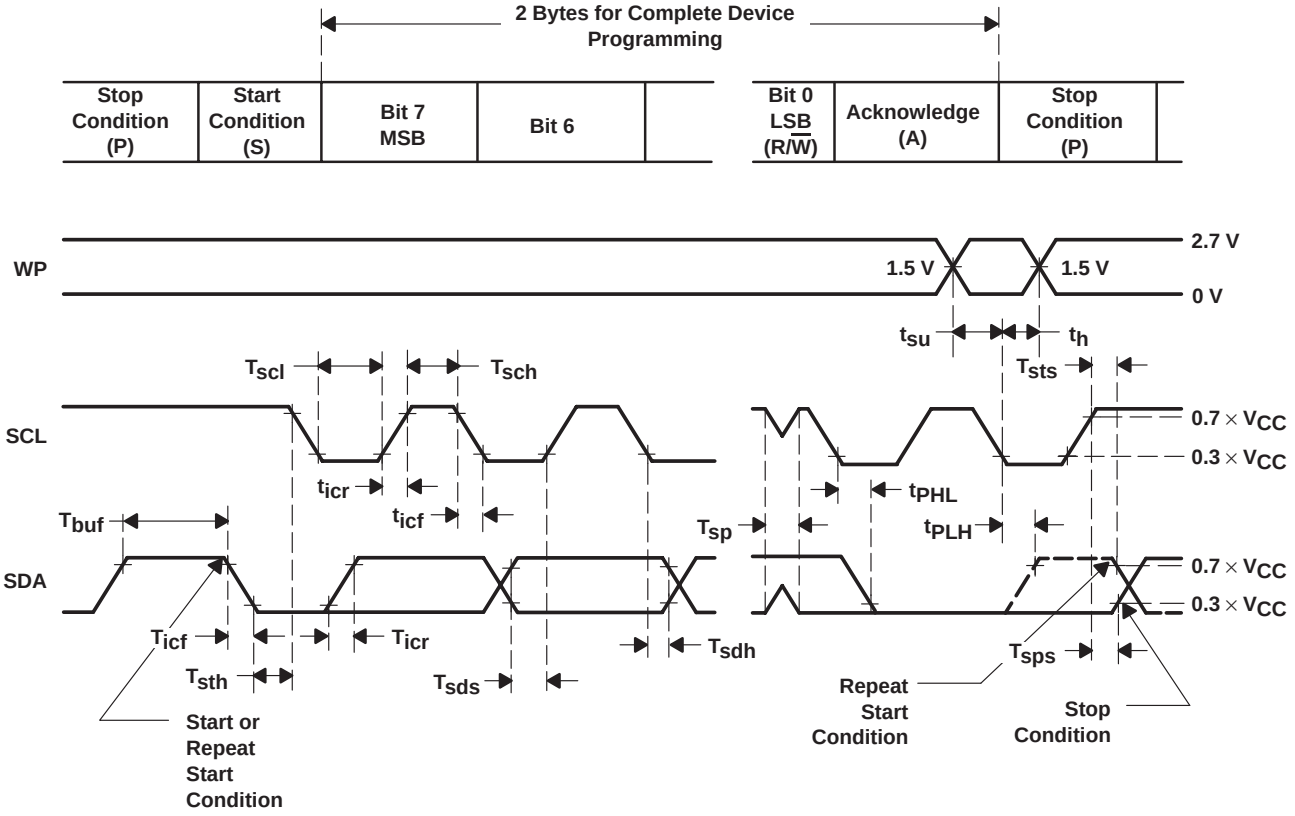
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	
t_{mpd}	Mux input to output propagation delay	MUX IN	MUX OUT		20	ns
t_{sov}	MUX SELECT to output valid	MUX SELECT	Output valid		22	ns
t_{ovn}	$\overline{\text{OVERRIDE}}$ to NON-MUXED OUT output delay	$\overline{\text{OVERRIDE}}$	NON-MUXED OUT		15	ns
t_{ovm}	$\overline{\text{OVERRIDE}}$ to MUX OUT output delay	$\overline{\text{OVERRIDE}}$	MUX OUT		25	ns
t_{su}	Setup time	WP	Falling edge of first valid data byte acknowledge on the SCL input	30		ns
t_h	Hold time	WP	Falling edge of first valid data byte acknowledge on the SCL input	120		ns
t_r	Output rise time			1	3	ns/V
t_f	Output fall time			1	3	ns/V

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

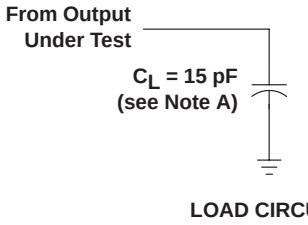


VOLTAGE WAVEFORMS

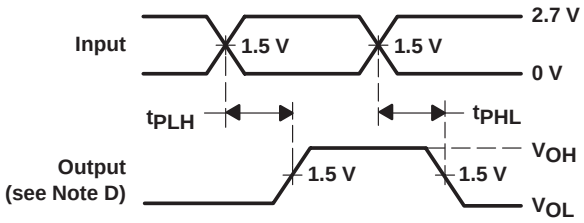
BYTE	DESCRIPTION
1	I²C address
2	Nonvolatile register data

Figure 1. I²C Interface Load Circuit and Voltage Waveforms

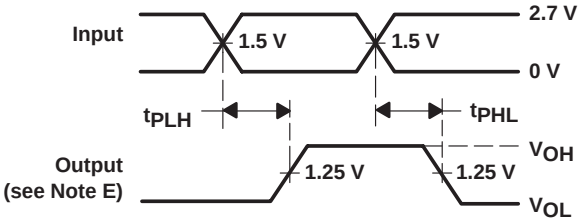
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
FOR NON-MUXED OUT OUTPUT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
FOR MUXED OUT OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{sov} and t_{ovn}.
E. t_{PLH} and t_{PHL} are the same as t_{mpd}, t_{sov}, and t_{ovm}.

Figure 2. Load Circuit and Voltage Waveforms

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