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STL40N75LF3

N-channel 75 V, 16 mΩ typ., 10 A STripFET™ III Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

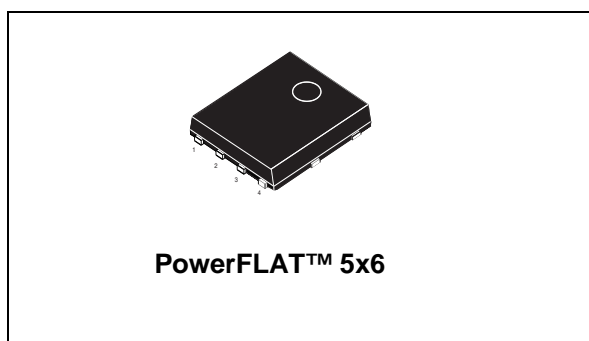
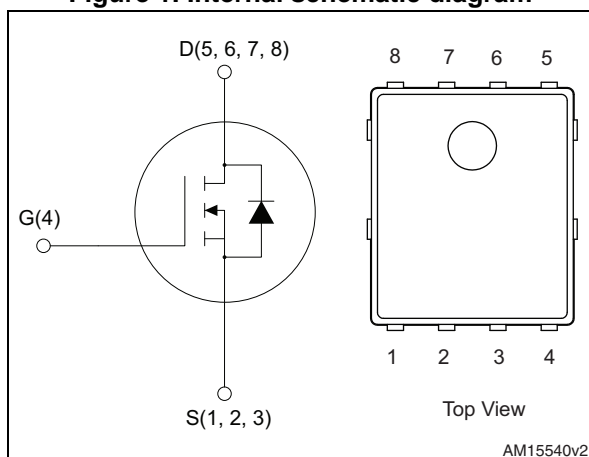


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D
STL40N75LF3	75 V	19 mΩ	10 A

- N-channel enhancement mode
- Low gate charge
- Low threshold voltage device

Applications

- Switching applications

Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL40N75LF3	40N75LF3	PowerFLAT™ 5x6	Tape and reel

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Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	75	V
V_{GS}	Gate-source voltage	+20\16	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	40	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	26	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	160	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	10	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$	6	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	75	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. The value is rated according to $R_{thj-case}$
2. Pulse width limited by safe operating area
3. The value is rated according to $R_{thj-pcb}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	31.3	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch², 2oz Cu., t < 10 sec.

Electrical characteristics

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2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 250 μA	75			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 75 V, V _{DS} = 75 V, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = +20 / -16 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1			V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 20 A V _{GS} = 5 V, I _D = 20 A		16 18.7	19 22	mΩ mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	1300 228 15	-	pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 37.5 V, I _D = 40 A V _{GS} = 5 V (see Figure 14)	-	12 5 5.3	-	nC nC nC
R _G	Gate input resistance	f = 1 MHz gate DC bias = 0 Test signal level = 20 mV open drain	-	3.5	-	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	V _{DD} = 37.5 V, I _D = 20 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13)	-	12 25 25 3	-	ns ns ns ns

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Electrical characteristics

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		40	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				160	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40\text{ A}, V_{GS}=0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 40\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD}=60\text{ V}$	-	35		ns
Q_{rr}	Reverse recovery charge			44		nC
I_{RRM}	Reverse recovery current			27		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μ s, duty cycle 1.5%

Electrical characteristics

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

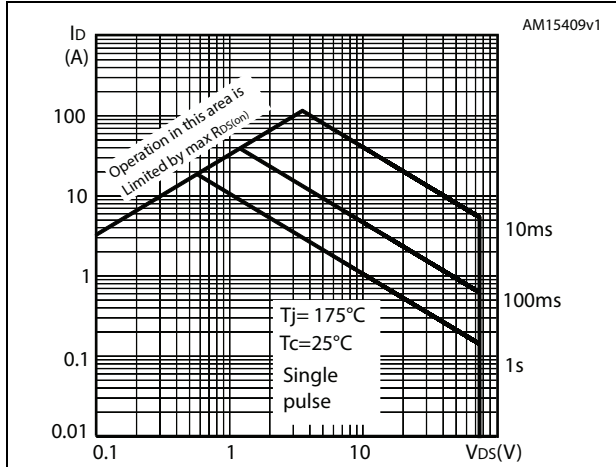


Figure 3. Thermal impedance

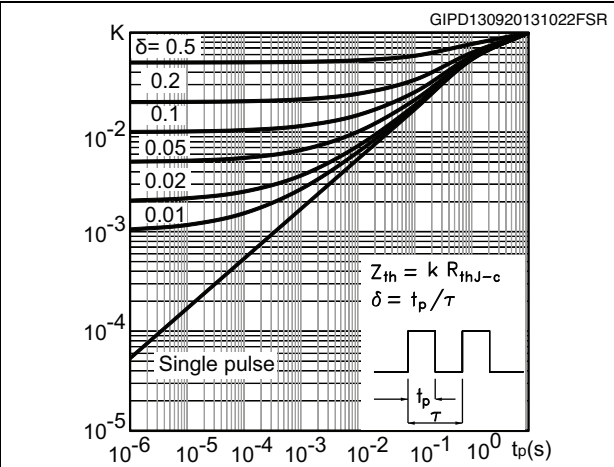


Figure 4. Output characteristics

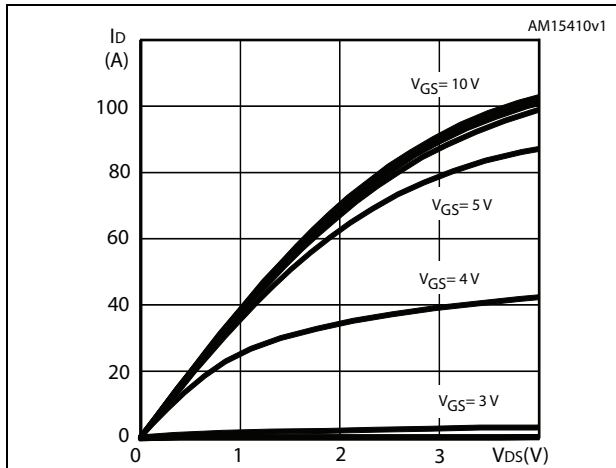


Figure 5. Transfer characteristics

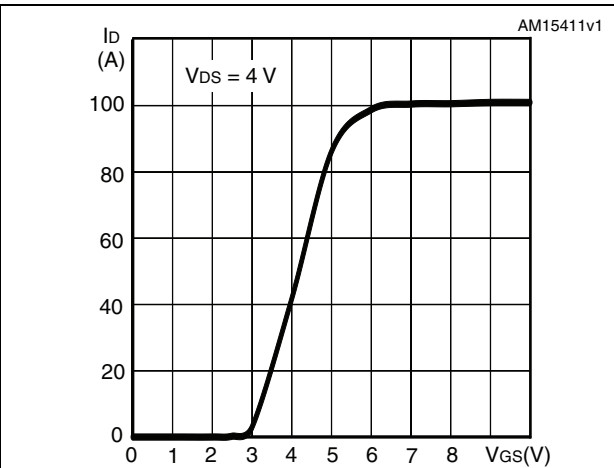


Figure 6. Gate charge vs gate-source voltage

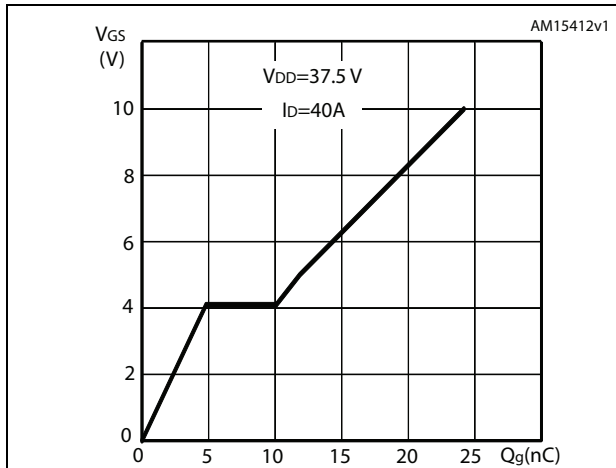
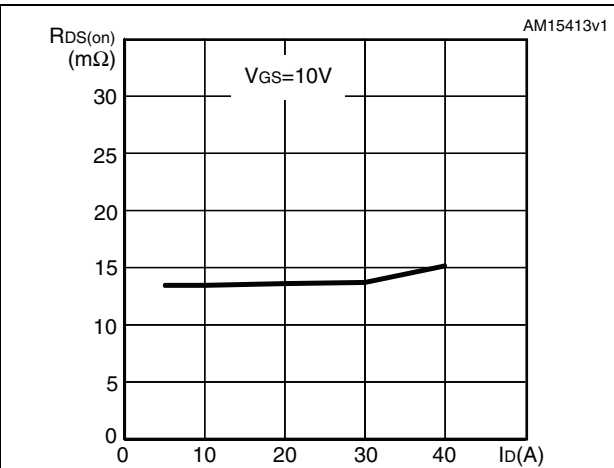


Figure 7. Static drain-source on-resistance



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Electrical characteristics

Figure 8. Capacitance variations

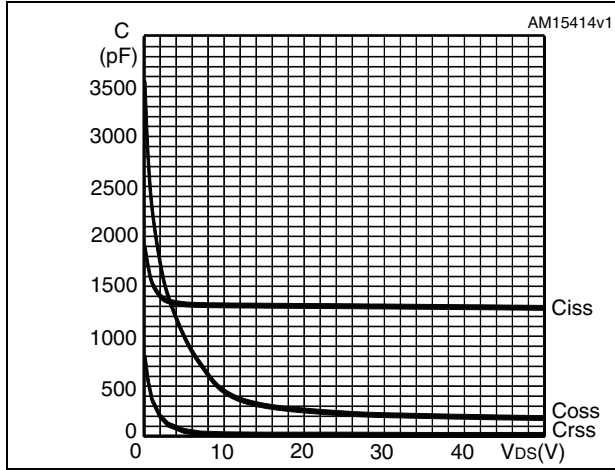


Figure 9. Normalized $V(BR)_{DSS}$ vs temperature

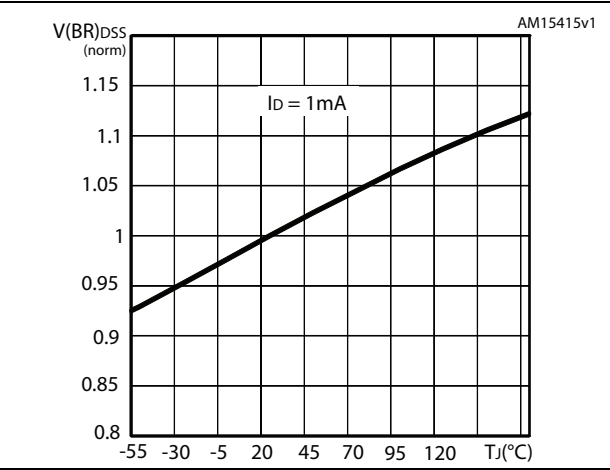


Figure 10. Normalized gate threshold voltage vs temperature

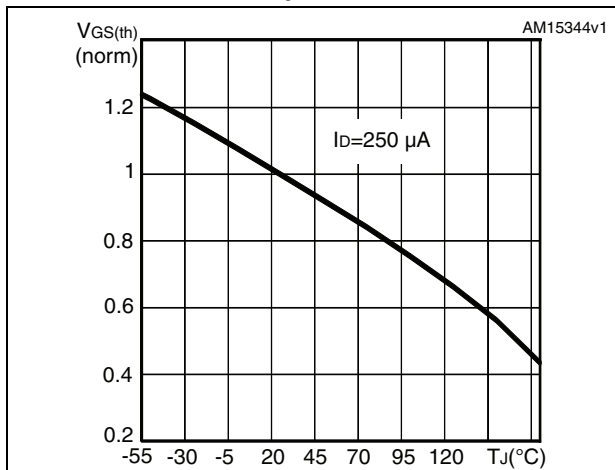


Figure 11. Normalized on-resistance vs temperature

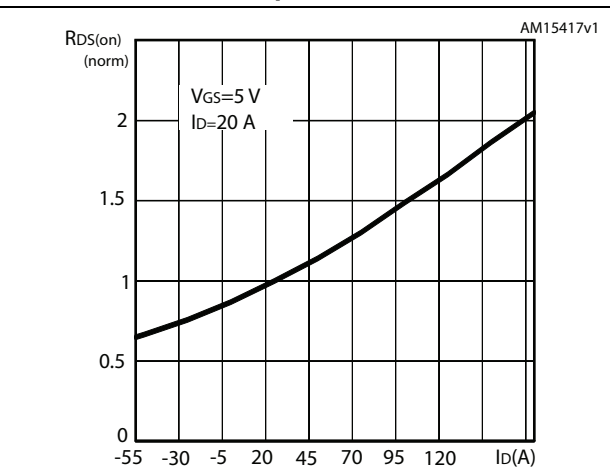
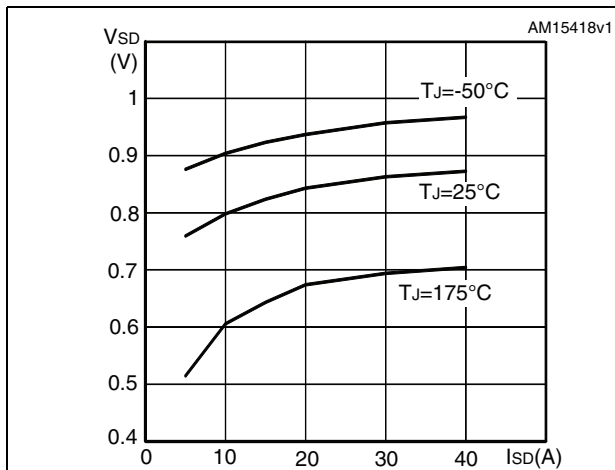


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

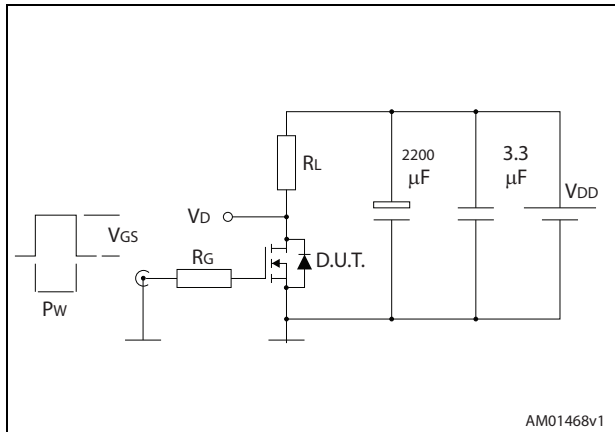


Figure 14. Gate charge test circuit

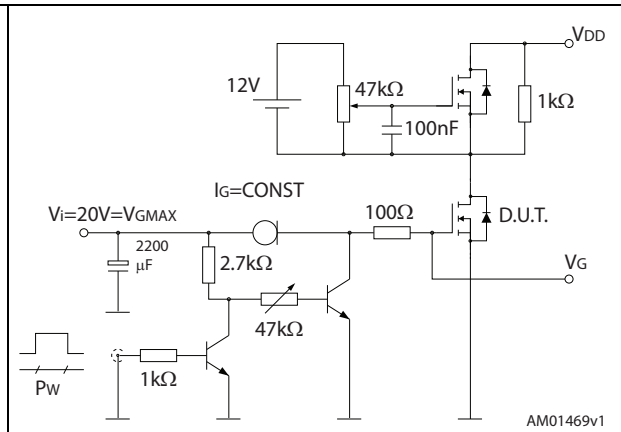


Figure 15. Test circuit for inductive load switching and diode recovery times

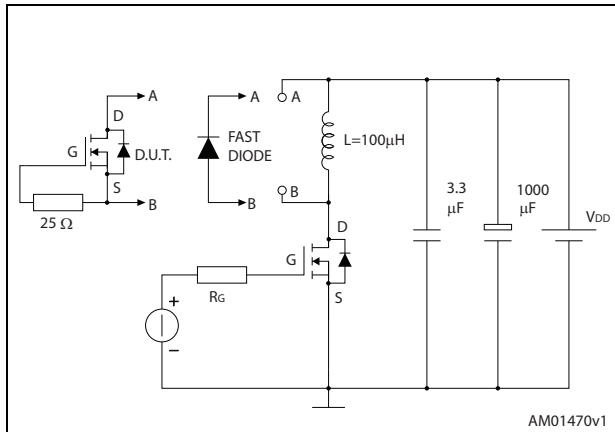


Figure 16. Unclamped inductive load test circuit

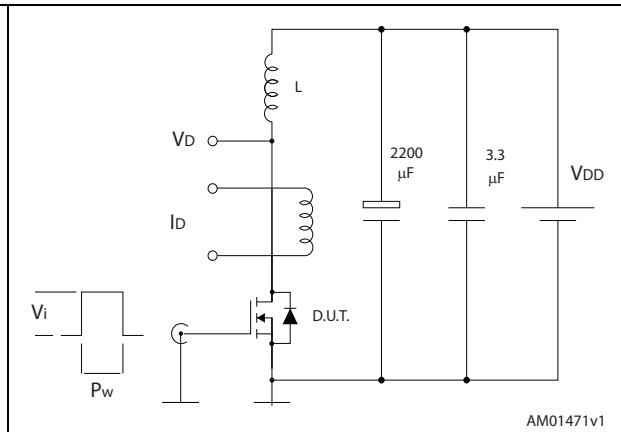


Figure 17. Unclamped inductive waveform

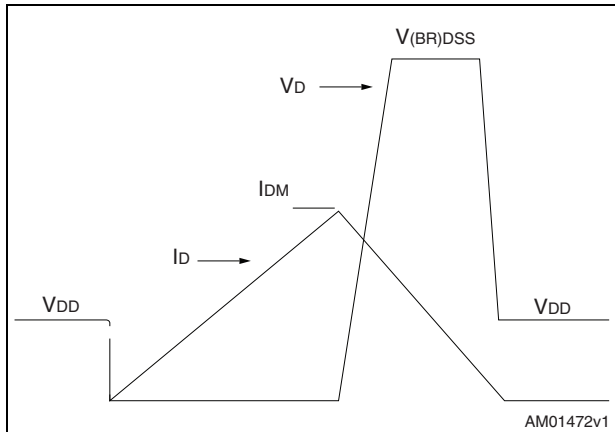
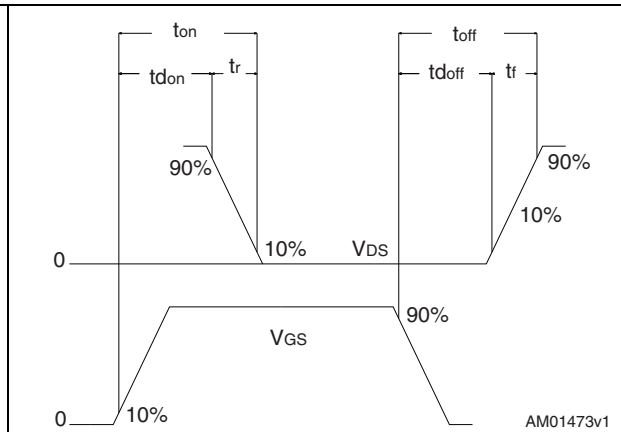


Figure 18. Switching time waveform



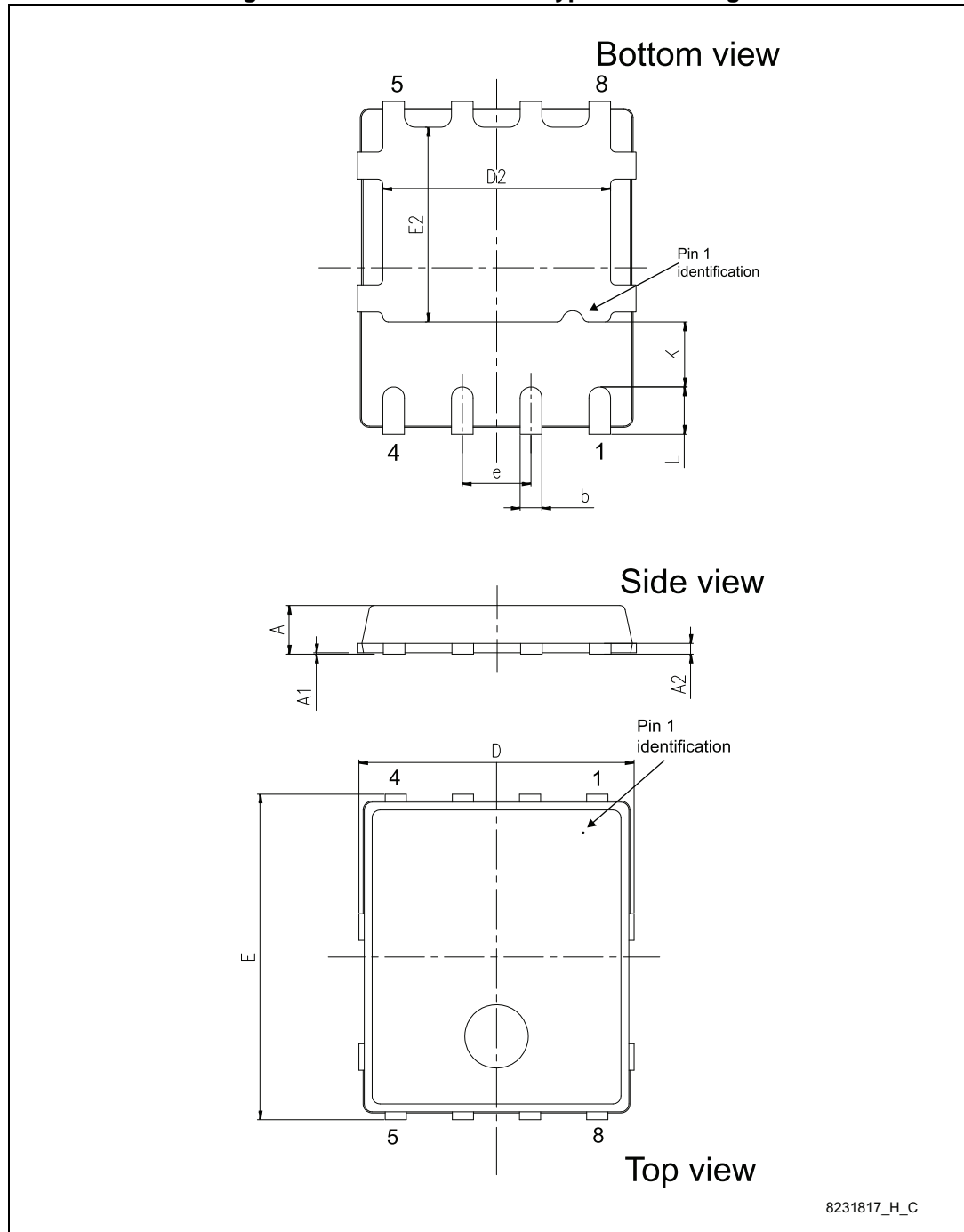
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Package mechanical data

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-C drawings



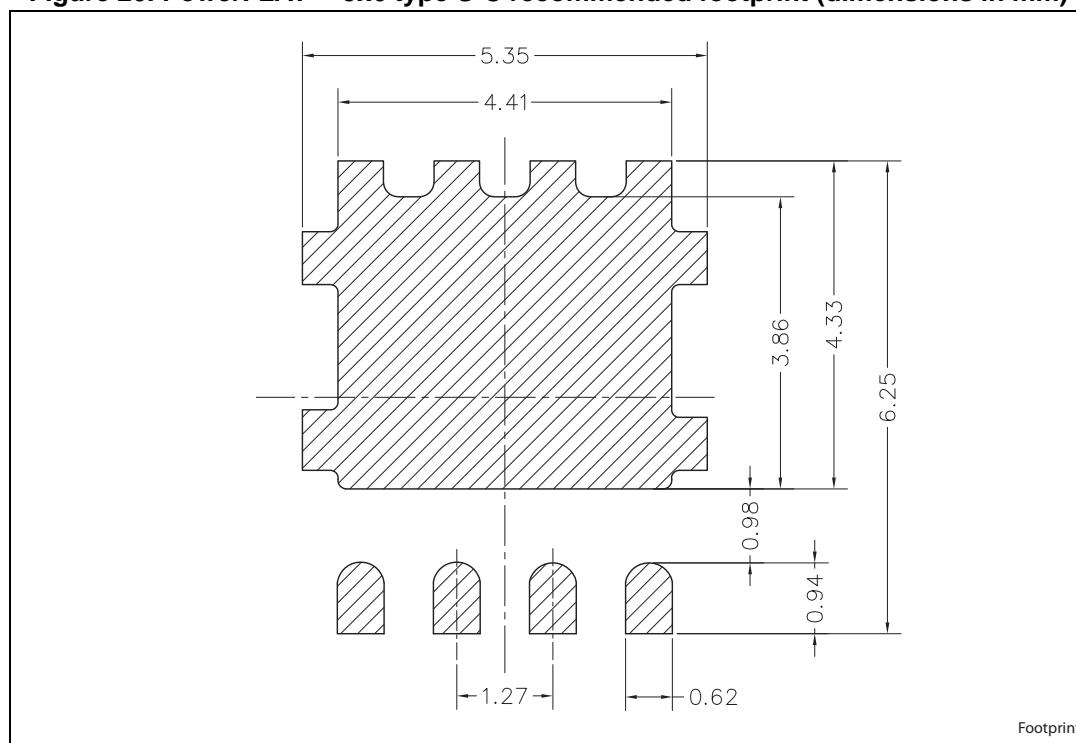
Package mechanical data

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Table 8. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Figure 20. PowerFLAT™ 5x6 type S-C recommended footprint (dimensions in mm)



5 Packaging information

Figure 21. PowerFLAT™ 5x6 type S-C tape

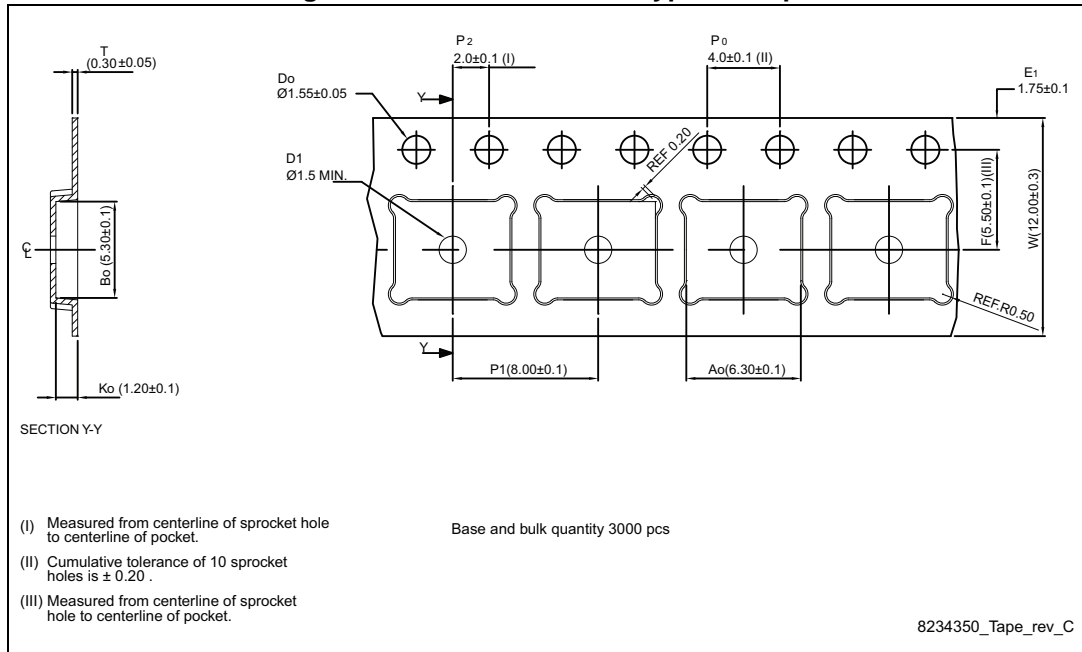
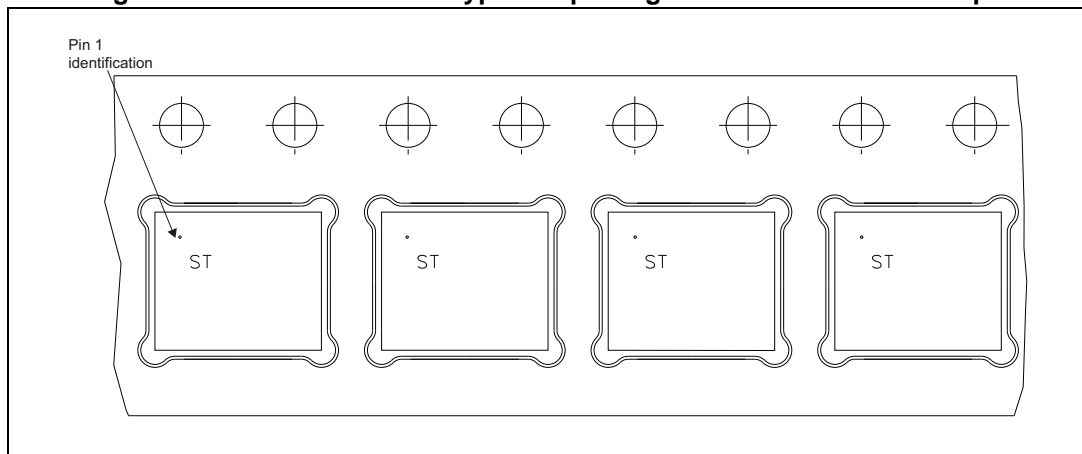


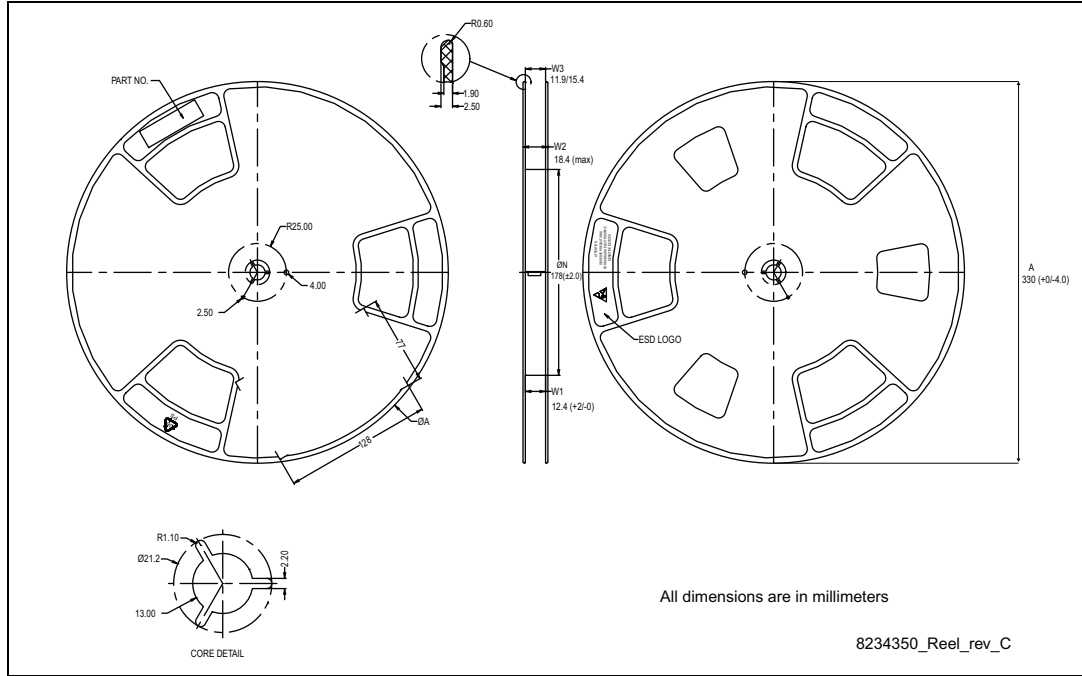
Figure 22. PowerFLAT™ 5x6 type S-C package orientation in carrier tape



Packaging information

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Figure 23. PowerFLAT™ 5x6 type S-C reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Oct-2012	1	First release.
24-Feb-2014	2	Deleted note in the table of <i>Features</i> . Updated <i>Figure 1</i> . Updated values of P_{TOT} , T_J and T_{stg} in <i>Table 2</i> . Updated notes in <i>Table 2</i> . Updated V_{GS} test condition in <i>Table 5</i> . Updated V_{DD} test condition in <i>Table 6</i> . Removed T_j test condition from <i>Table 7</i> . Updated <i>Figure 2</i> , <i>Figure 4</i> , <i>Figure 6</i> , <i>Figure 9</i> and <i>Figure 11</i> . Updated mechanical data.

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