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STMicroelectronics
EMIF08-1005T16

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EMIF08-1005T16

8 lines IPAD™ low capacitance EMI filter and ESD protection in thin micro QFN

Datasheet – production data

Features

- High efficiency in EMI filtering
- ESD performances: up to 15 kV
- Micro QFN 400 µm pitch
- Low PCB space consuming with narrow package (1.35 mm width)
- Thin package: 0.5 mm max.
- ECOPACK®2 compliant component

Benefits

- High reduction of parasitic elements through integration
- Improved application robustness against ESD
- High reliability offered by monolithic integration
- Low profile and small packaging save space on the PCB

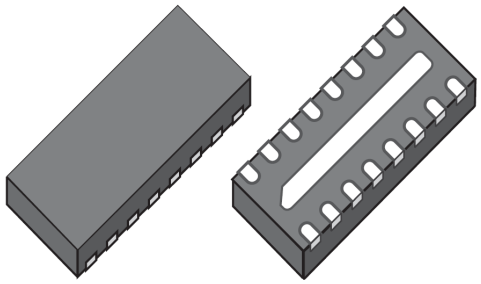
Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

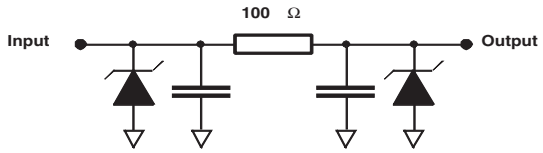
Where EMI filtering in ESD sensitive equipment is required:

- Mobile phone
- Netbook, laptop PC
- Portable devices



Micro QFN 16L 1.35 x 3.3 x 0.5 mm

Figure 1. Basic cell configuration



Typical line capacitance = 45 pF at 0 V

Description

The EMIF08-1005T16 is an 8 lines highly integrated device designed to suppress EMI / RFI noise in all systems exposed to electromagnetic interference.

This filter includes an ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV on the input or output pins.

TM: IPAD is a trademark of STMicroelectronics.

1 Characteristics

Figure 2. Pin numbering

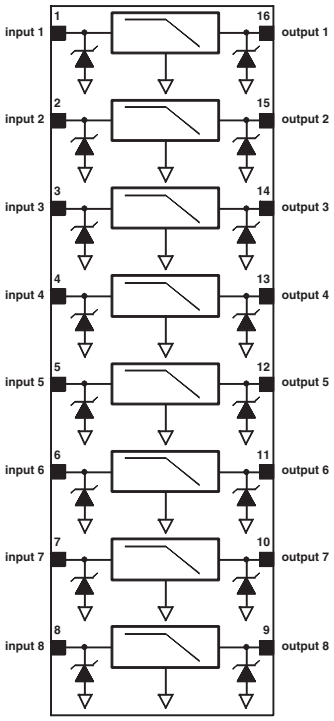


Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, all pins to GND: Contact discharge Air discharge	 ±15 ±30	kV
I_{RMS}	Maximum rms current	50	mA
T_{OP}	Operating temperature	-40 to 85	°C
T_j	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Figure 3. Electrical characteristics (definitions)

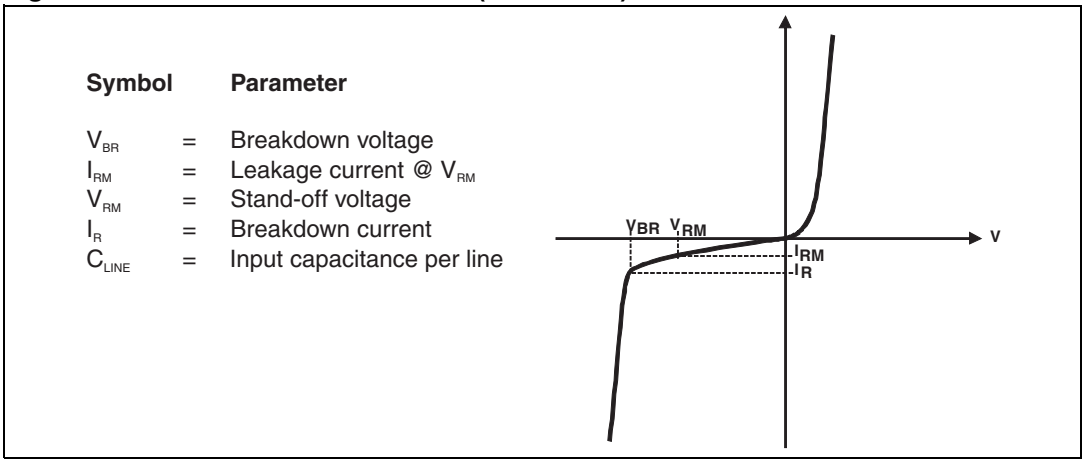


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3 V per line			100	nA
$R_{i/o}$	Tolerance 10%	90	100	110	Ω
C_{LINE}	V_{LINE} = 0 V DC, F = 1 MHz, V_{osc} = 30 mV		45	50	pF
	V_{LINE} = 2.5 V DC, F = 1 MHz, V_{osc} = 30 mV		9		

Figure 4. S21 attenuation measurements

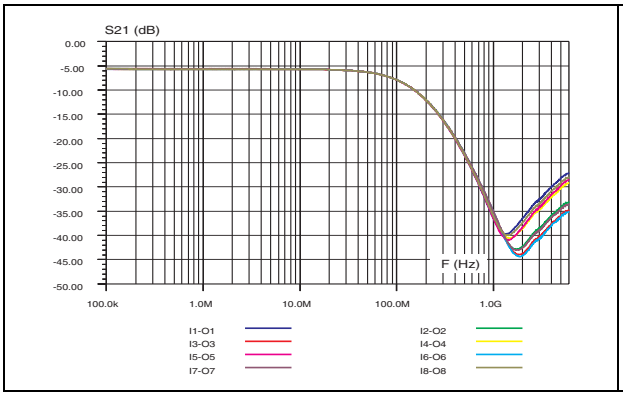


Figure 5. Analog crosstalk measurements

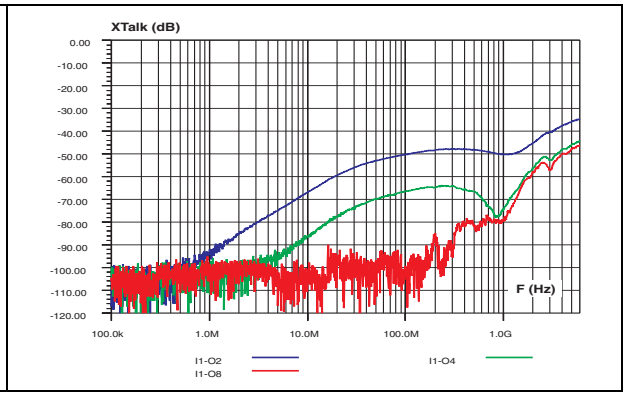


Figure 6. ESD response to IEC 61000-4-2 (+15 kV contact discharge)

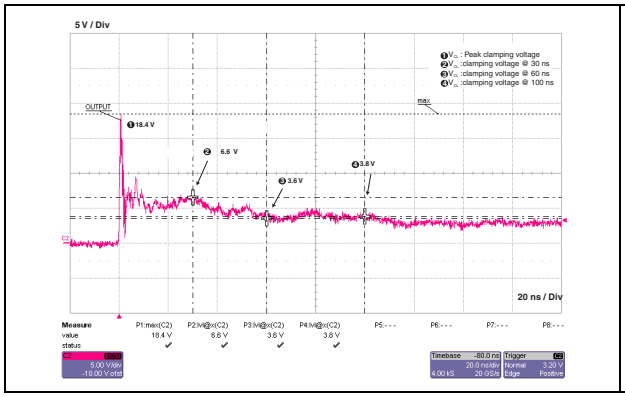


Figure 7. ESD response to IEC 61000-4-2 (-15 kV contact discharge)

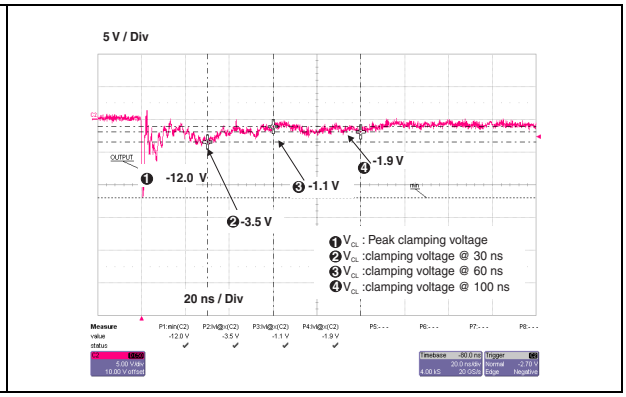


Figure 8. Line capacitance versus applied voltage

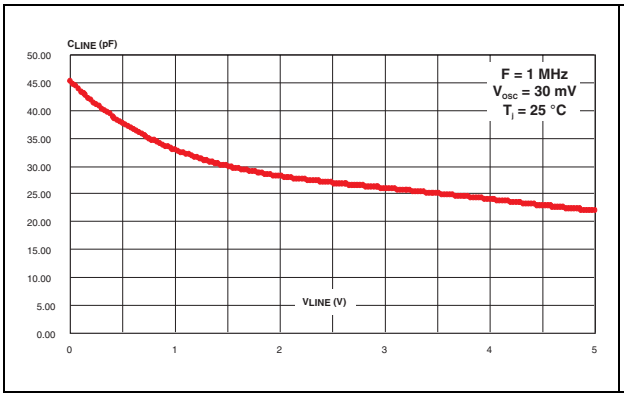
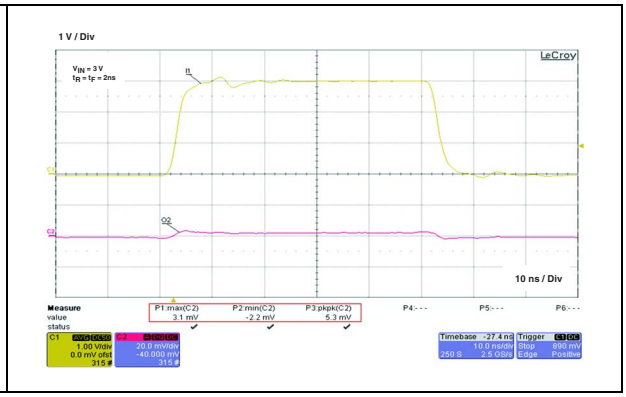
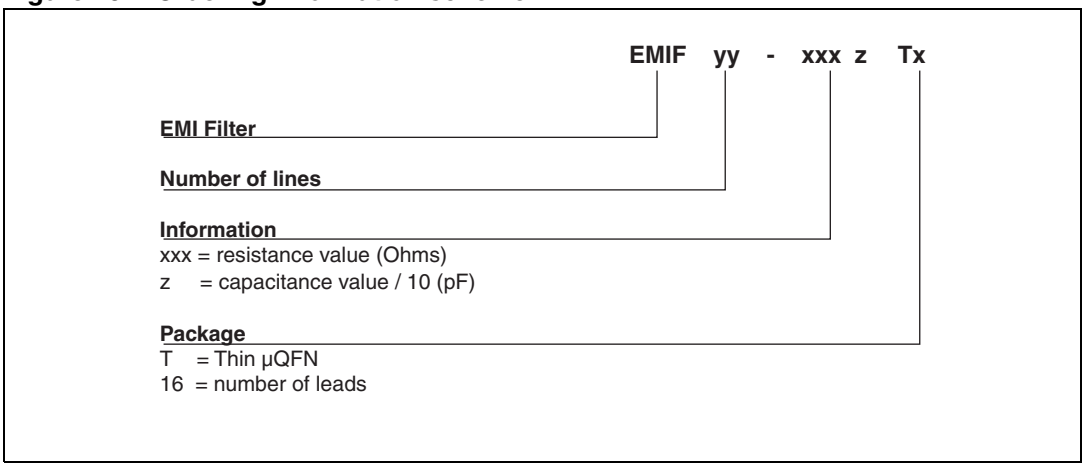


Figure 9. Typical digital crosstalk



2 Ordering information scheme

Figure 10. Ordering information scheme

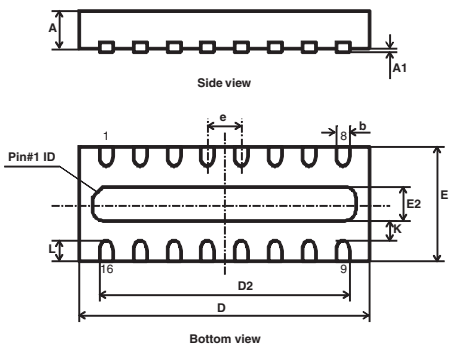


3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 3. Thin µQFN 3.3x1.35 16L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.41	0.45	0.50	0.016	0.018	0.020
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.25	3.30	3.35	0.128	0.130	0.132
D2	2.85	3.00	3.10	0.112	0.118	0.122
E	1.30	1.35	1.40	0.051	0.053	0.055
E2	0.25	0.40	0.50	0.010	0.016	0.020
e	-	0.40	-	-	0.016	-
k	0.20	-	-	0.008	-	-
L	0.20	0.25	0.30	0.008	0.010	0.012

Figure 11. Footprint

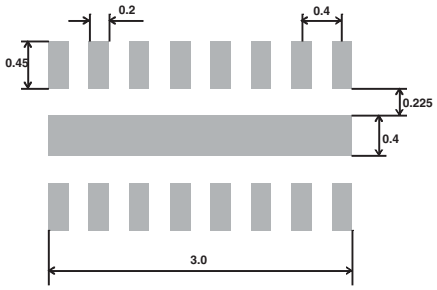
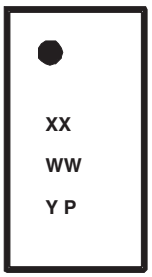
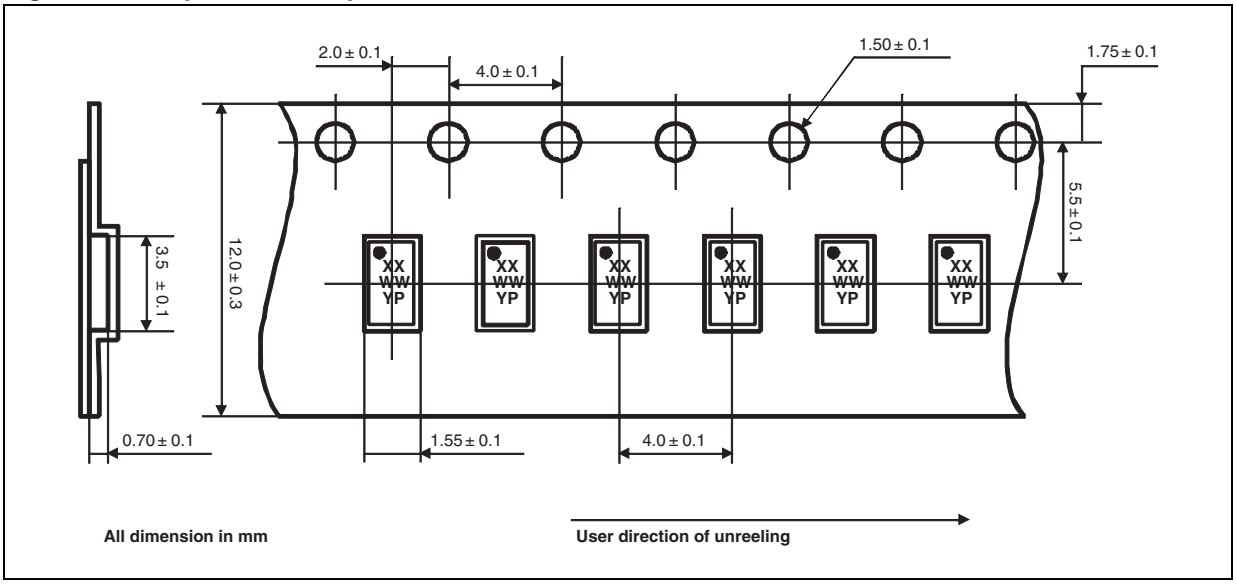


Figure 12. Marking



Dot : Pin 1
XX : Marking
WW : Assembly Week
Y : Assembly Year
P : Assembly Plant

Figure 13. Tape and reel specification



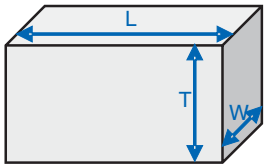
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

4 Recommendations on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 14. Stencil opening dimensions



   b) General design rule

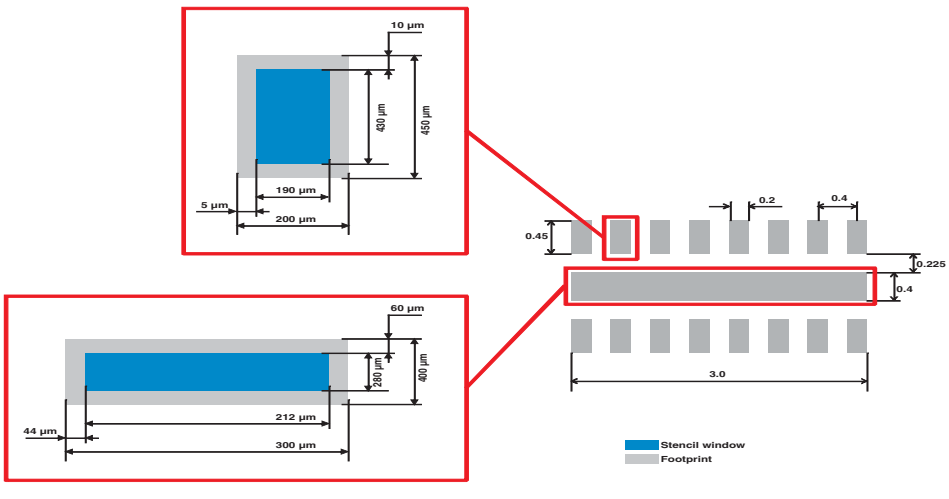
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 15. Recommended stencil window position



4.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

4.3 Placement

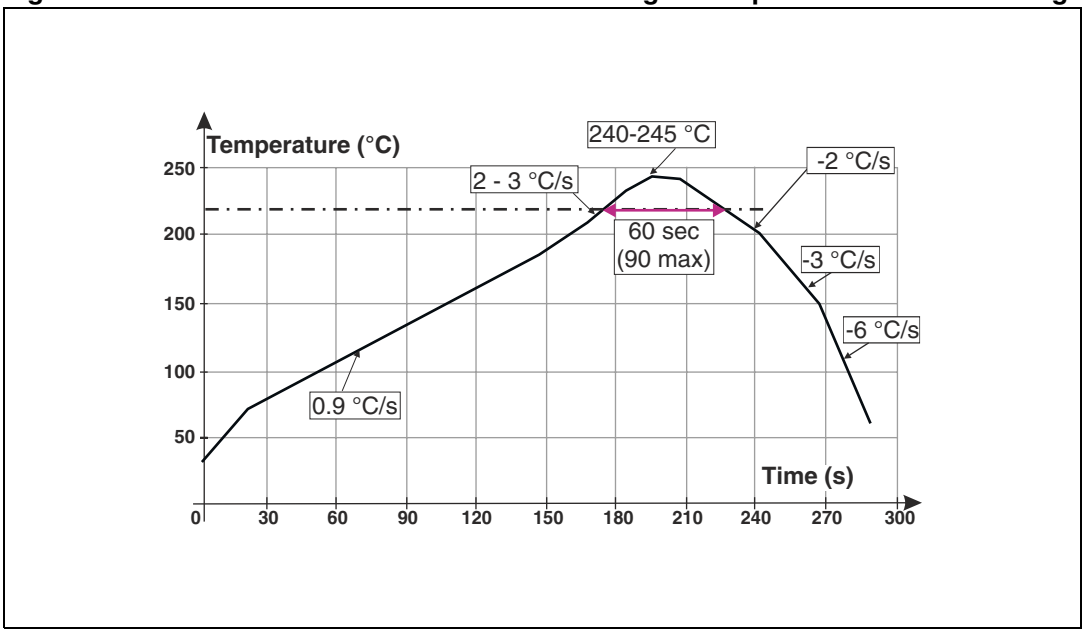
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 16. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF08-1005T16	LA(1)	µQFN	6.29 mg	3000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
31-Oct-2012	1	Initial release.

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