

## **Excellent Integrated System Limited**

Stocking Distributor

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[Vishay/Siliconix](#)  
[SI1062X-T1-GE3](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)



## N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) Max.	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
20	0.420 at V <sub>GS</sub> = 4.5 V	0.5	1 nC
	0.492 at V <sub>GS</sub> = 2.5 V	0.2	
	0.597 at V <sub>GS</sub> = 1.8 V	0.2	
	0.762 at V <sub>GS</sub> = 1.5 V	0.05	

### FEATURES

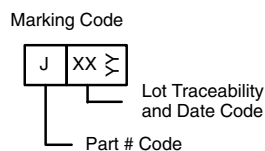
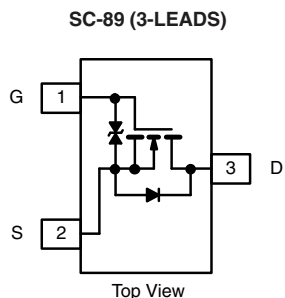
- TrenchFET<sup>®</sup> Power MOSFET
- Gate-Source ESD Protected: 1000 V
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS  
 COMPLIANT  
 HALOGEN  
 FREE

### APPLICATIONS

- Load/Power Switching for Portable Devices
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits



Ordering Information: Si1062X-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	± 8	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	0.53 <sup>a, b</sup>	A
	T <sub>A</sub> = 70 °C	0.43 <sup>a, b</sup>	
Pulsed Drain Current (t = 300 μs)	I <sub>DM</sub>	2	
Continuous Source-Drain Diode Current	I <sub>S</sub>	0.18 <sup>a, b</sup>	A
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C	0.22 <sup>a, b</sup>	W
	T <sub>A</sub> = 70 °C	0.14 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient <sup>b</sup>	t ≤ 5 s	R <sub>thJA</sub>	440	530	°C/W
	Steady State		540	650	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.

**New Product**
**Si1062X**

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<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		11		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-1.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.4		1	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 30$	$\mu\text{A}$
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			$\pm 1$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	2			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$		0.350	0.420	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 0.2\text{ A}$		0.410	0.492	
		$V_{GS} = 1.8\text{ V}, I_D = 0.2\text{ A}$		0.459	0.597	
		$V_{GS} = 1.5\text{ V}, I_D = 0.05\text{ A}$		0.510	0.762	
Forward Transconductance	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 0.5\text{ A}$		7.5		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		43		pF
Output Capacitance	$C_{oss}$			14		
Reverse Transfer Capacitance	$C_{rss}$			8		
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 8\text{ V}, I_D = 0.5\text{ A}$		1.8	2.7	nC
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$		1	2	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$		0.16		nC
Gate-Drain Charge	$Q_{gd}$			0.13		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		12.2		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 20\text{ }\Omega$ $I_D \cong 0.4\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		2	4	ns
Rise Time	$t_r$			14	24	
Turn-Off Delay Time	$t_{d(off)}$			16	30	
Fall Time	$t_f$			11	20	
<b>Drain-Source Body Diode Characteristics</b>						
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				2	A
Body Diode Voltage	$V_{SD}$	$I_S = 0.4\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 0.4\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		10	15	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			2	4	nC
Reverse Recovery Fall Time	$t_a$			5		ns
Reverse Recovery Rise Time	$t_b$			5		

Notes:

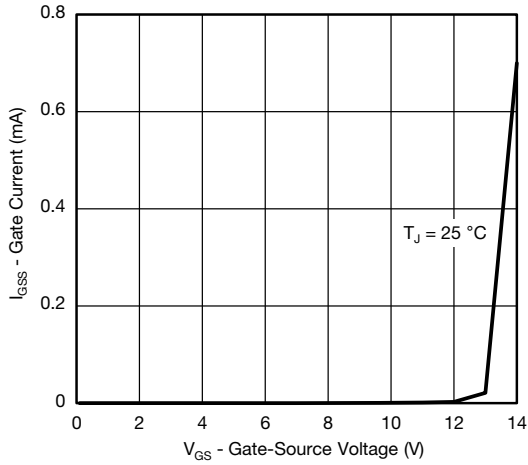
 a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

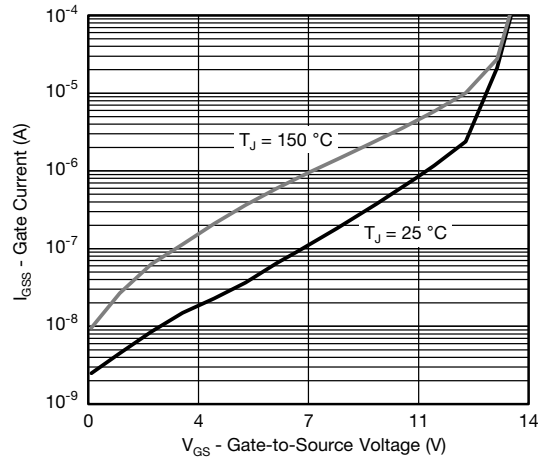
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



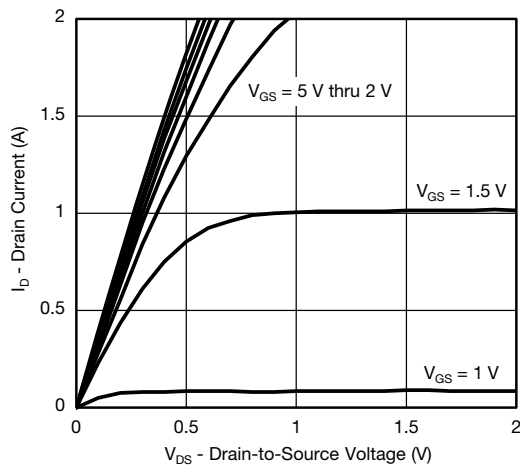
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



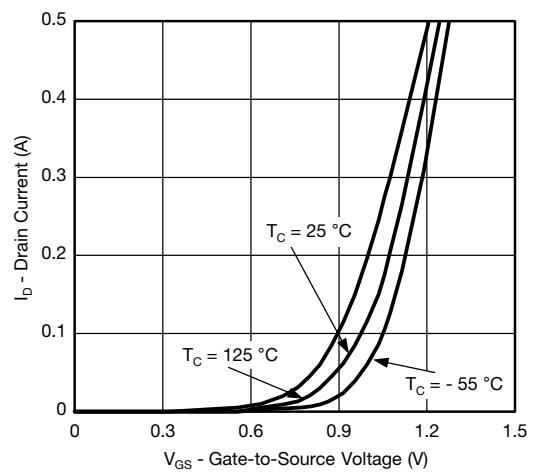
**Gate Current vs. Gate-Source Voltage**



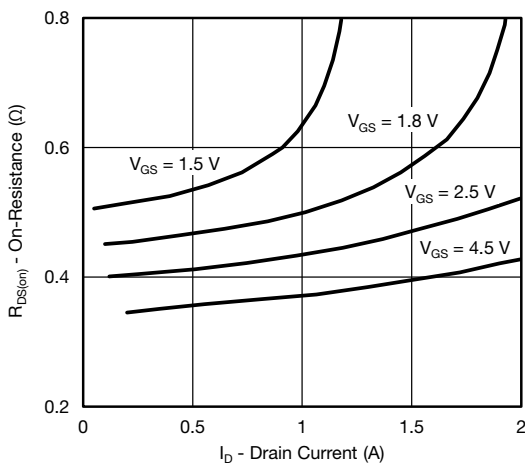
**Gate Current vs. Gate-Source Voltage**



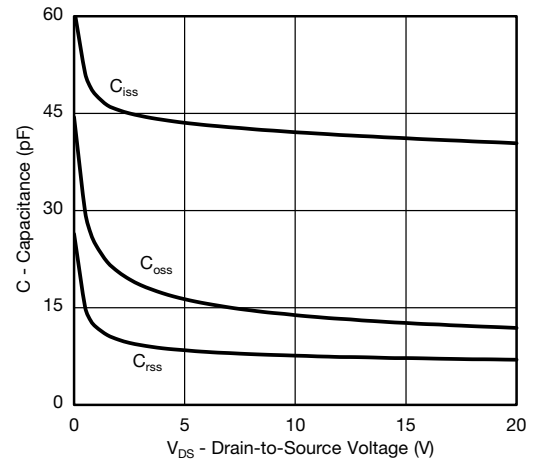
**Output Characteristics**



**Transfer Characteristics**



**On-Resistance vs. Drain Current**



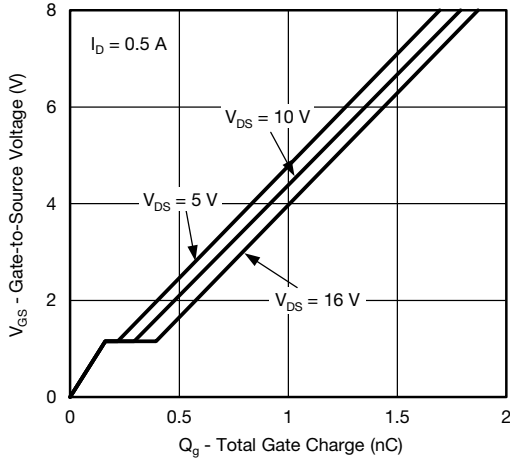
**Capacitance**



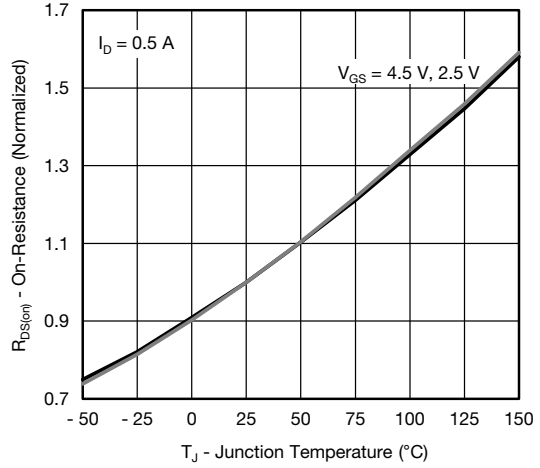
**Si1062X**

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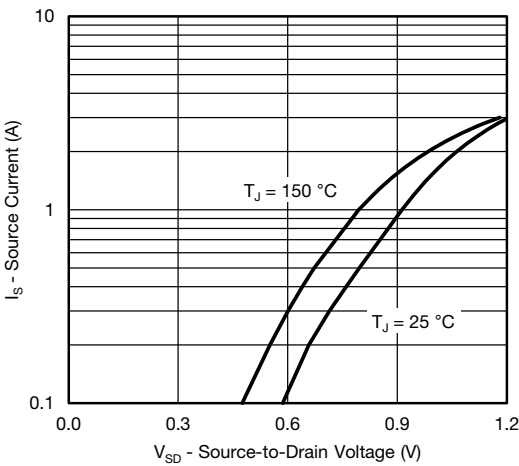
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



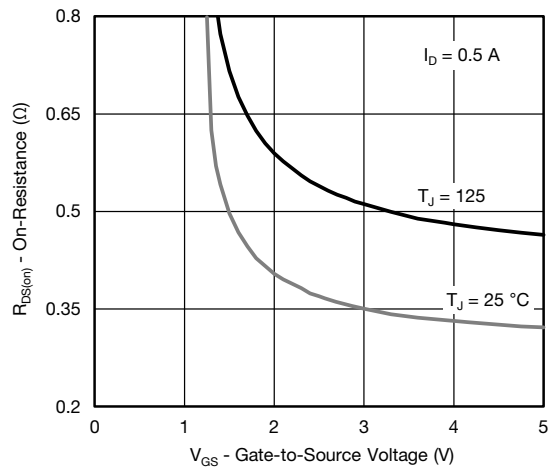
**Gate Charge**



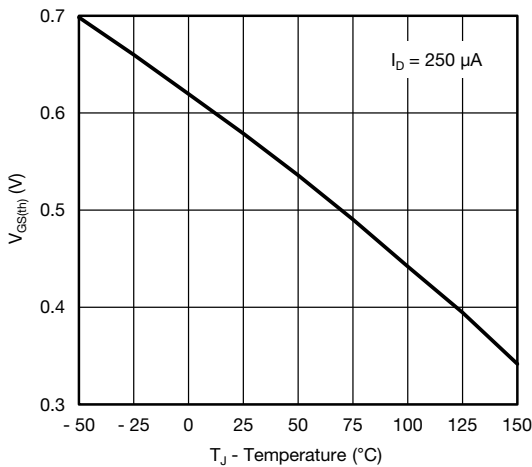
**On-Resistance vs. Junction Temperature**



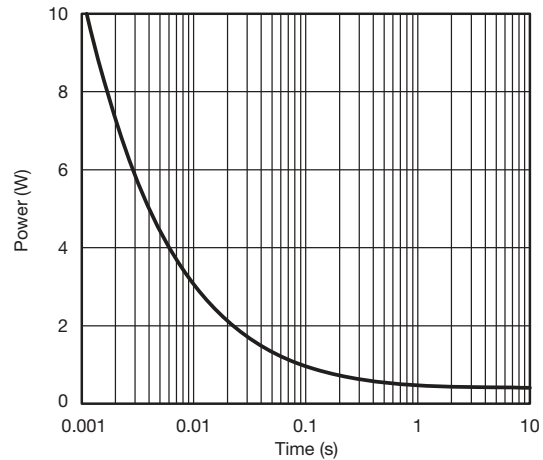
**Source-Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



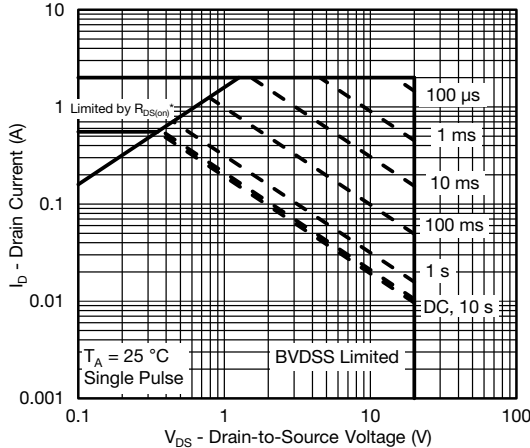
**Single Pulse Power, Junction-to-Ambient**

**New Product**

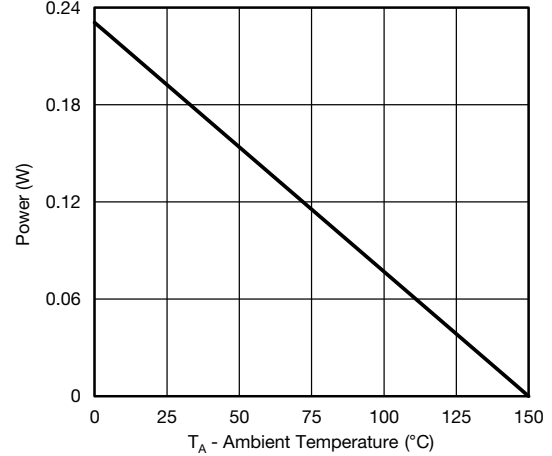


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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

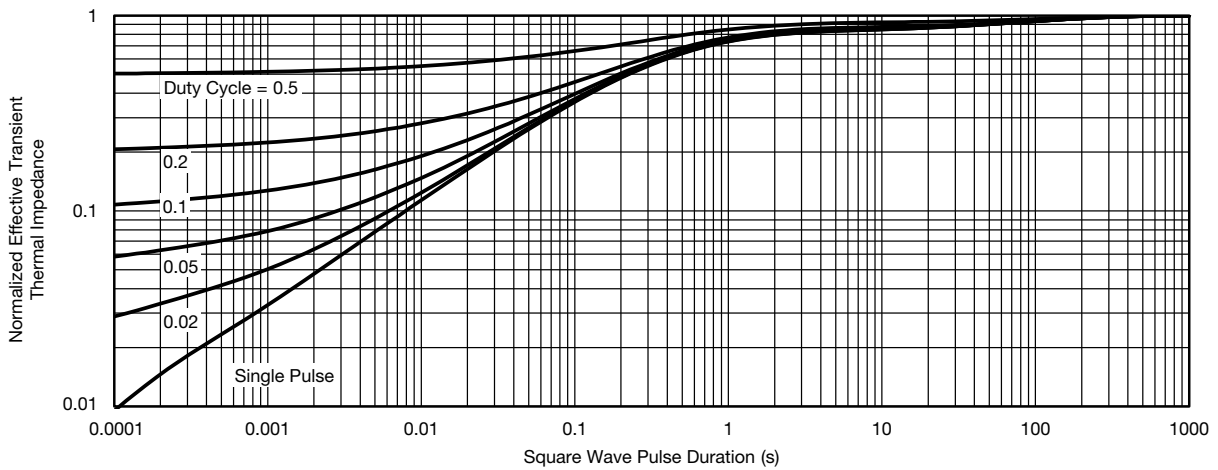


**Safe Operating Area, Junction-to-Ambient**



**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

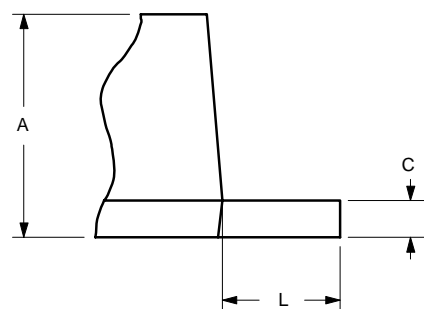
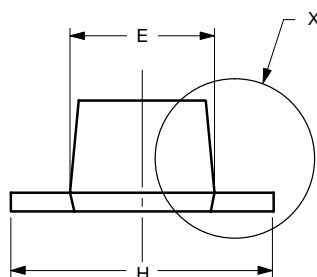
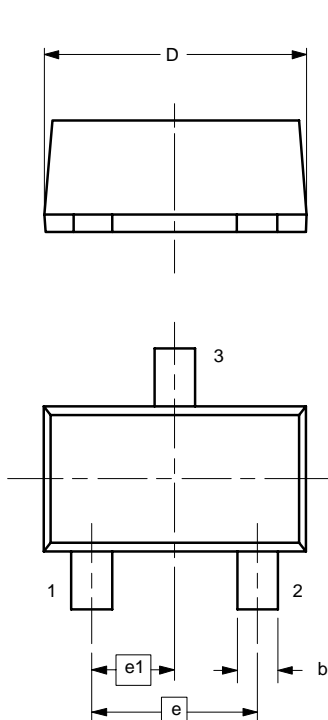
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## Package Information

### Vishay Siliconix

#### SC89-3



DETAIL X

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	0.60	0.80	0.024	0.031
<b>b</b>	0.23	0.33	0.009	0.013
<b>C</b>	0.10	0.20	0.004	0.008
<b>D</b>	1.50	1.70	0.059	0.067
<b>E</b>	0.75	0.95	0.030	0.037
<b>e</b>	1.00 BSC		0.040 BSC	
<b>e<sub>1</sub></b>	0.50 BSC		0.020 BSC	
<b>H</b>	1.50	1.70	0.059	0.067
<b>L</b>	0.30	0.50	0.012	0.020

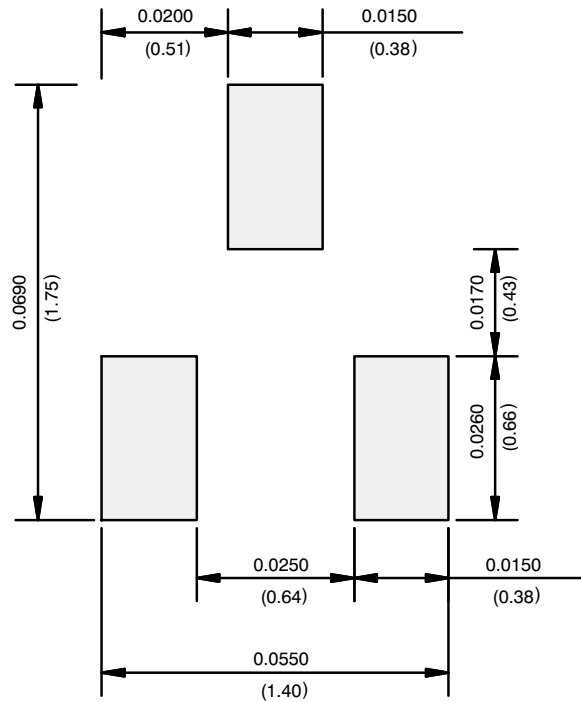
ECN: S-03946—Rev. B, 09-Jul-01  
DWG: 5869

# Application Note 826

Vishay Siliconix



## RECOMMENDED MINIMUM PADS FOR SC-89: 3-Lead



Recommended Minimum Pads  
 Dimensions in Inches/(mm)

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