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[Vishay/Siliconix](#)
[SIB417AEDK-T1-GE3](#)

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sales@integrated-circuit.com

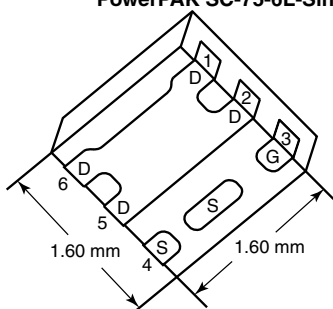


SiB417AEDK
 Vishay Siliconix

P-Channel 1.2 V (G-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A) ^g	Q _g (Typ.)
- 8	0.032 at V _{GS} = - 4.5 V	- 9 ^a	11.3 nC
	0.045 at V _{GS} = - 2.5 V	- 9 ^a	
	0.063 at V _{GS} = - 1.8 V	- 9 ^a	
	0.120 at V _{GS} = - 1.5 V	- 8.8	
	0.230 at V _{GS} = - 1.2 V	- 6.4	

PowerPAK SC-75-6L-Single



Ordering Information:
 SiB417AEDK-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

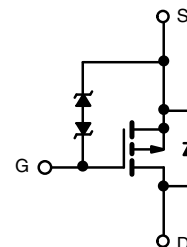
- TrenchFET[®] Power MOSFET
- Thermally Enhanced PowerPAK[®] SC-75 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g Tested
- Typical ESD Protection 2500 V
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
 COMPLIANT
 HALOGEN
FREE

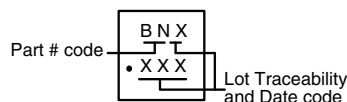
APPLICATIONS

- Load Switch for Portable Devices, Smart Phones, and Tablet PCs
 - Low Voltage Drop
 - Space Savings



P-Channel MOSFET

Marking Code



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 8	V
Gate-Source Voltage	V _{GS}	± 5	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 9 ^a
		T _C = 70 °C	- 9 ^a
		T _A = 25 °C	- 7.2 ^{b, c}
		T _A = 70 °C	- 5.7 ^{b, c}
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 15	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	- 9 ^a
		T _A = 25 °C	- 2 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	13
		T _C = 70 °C	8.4
		T _A = 25 °C	2.4 ^{b, c}
		T _A = 70 °C	1.6 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	41	51	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	7.5	9.5	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 105 °C/W.
- Based on T_C = 25 °C.

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 8			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 6.1		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			2.1		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.35		- 1	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 5 V			± 20	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 8 V, V _{GS} = 0 V V _{DS} = - 8 V, V _{GS} = 0 V, T _J = 55 °C			- 1 - 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 15			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 3 A		0.0265	0.0320	Ω
		V _{GS} = - 2.5 V, I _D = - 3 A		0.0360	0.0450	
		V _{GS} = - 1.8 V, I _D = - 1 A		0.0500	0.0630	
		V _{GS} = - 1.5 V, I _D = - 0.5 A		0.0600	0.1200	
		V _{GS} = - 1.2 V, I _D = - 0.5 A		0.1000	0.2300	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 4 V, I _D = - 7.4 A		18		S
Dynamic^b						
Input Capacitance	C _{iSS}	V _{DS} = - 4 V, V _{GS} = 0 V, f = 1 MHz		878		pF
Output Capacitance	C _{oSS}			415		
Reverse Transfer Capacitance	C _{rSS}			735		
Total Gate Charge	Q _g	V _{DS} = - 4 V, V _{GS} = - 5 V, I _D = - 7.4 A		12.3	18.5	nC
		V _{DS} = - 4 V, V _{GS} = - 4.5 V, I _D = - 7.4 A		11.3	17	
Gate-Source Charge	Q _{gs}			1.35		
Gate-Drain Charge	Q _{gd}			3.42		
Gate Resistance	R _g	f = 1 MHz	1.3	6.5	13	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 4 V, R _L = 0.68 Ω I _D ≅ - 5.9 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		19	29	ns
Rise Time	t _r			18	27	
Turn-Off Delay Time	t _{d(off)}			32	48	
Fall Time	t _f			19	29	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 9	A
Pulse Diode Forward Current	I _{SM}				- 15	
Body Diode Voltage	V _{SD}	I _S = - 5.9 A, V _{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 5.9 A, dI/dt = 100 A/μs, T _J = 25 °C		32	48	ns
Body Diode Reverse Recovery Charge	Q _{rr}			13	20	nC
Reverse Recovery Fall Time	t _a			14		ns
Reverse Recovery Rise Time	t _b			18		

Notes:

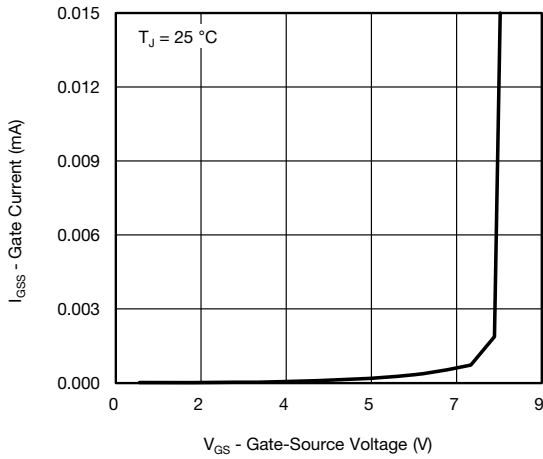
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

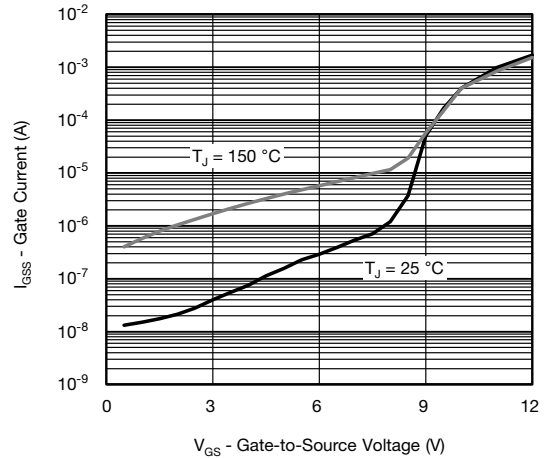


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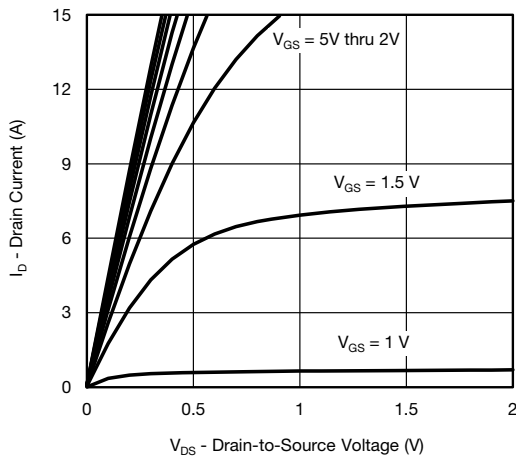
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



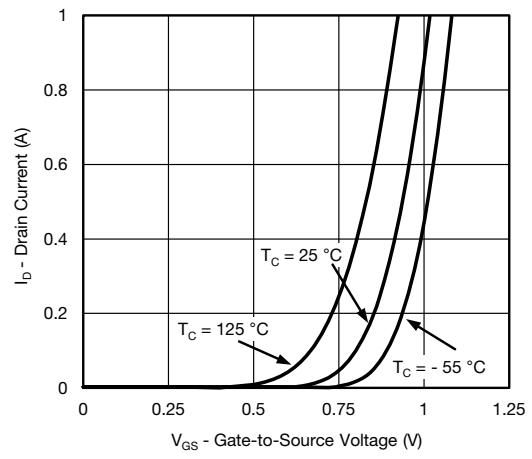
Gate Source Voltage vs. Gate Current



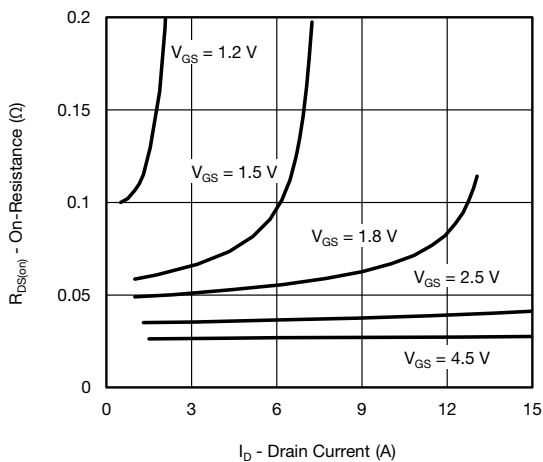
Gate Source Voltage vs. Gate Current



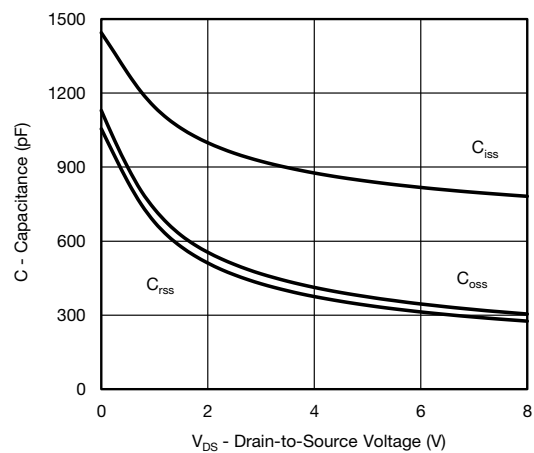
Output Characteristics



Transfer Characteristics



On-Resistance vs. Drain Current and Gate Voltage

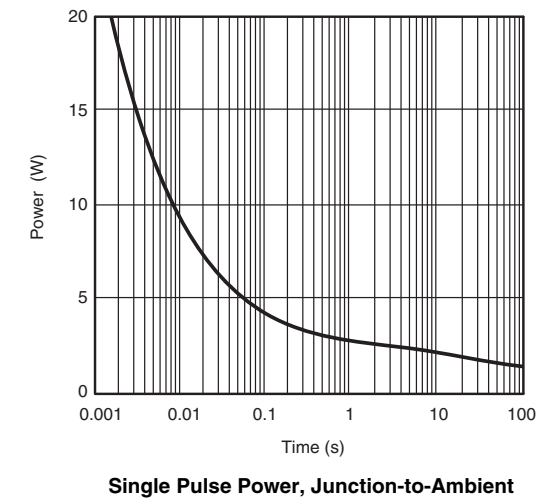
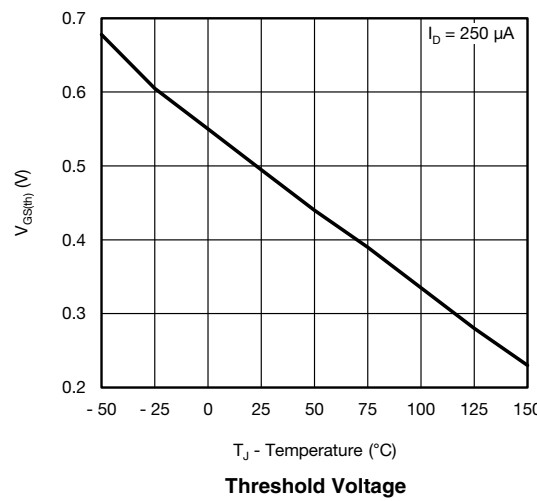
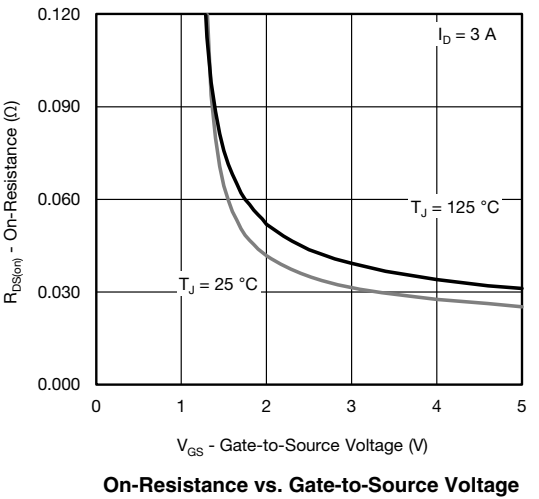
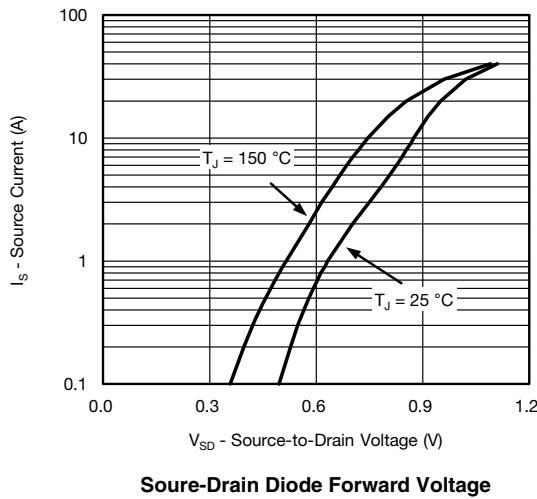
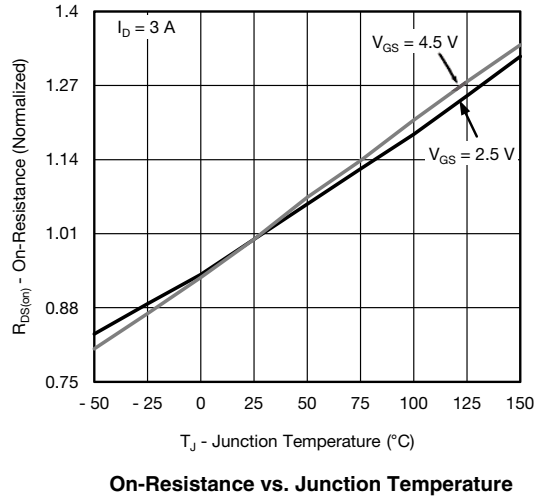
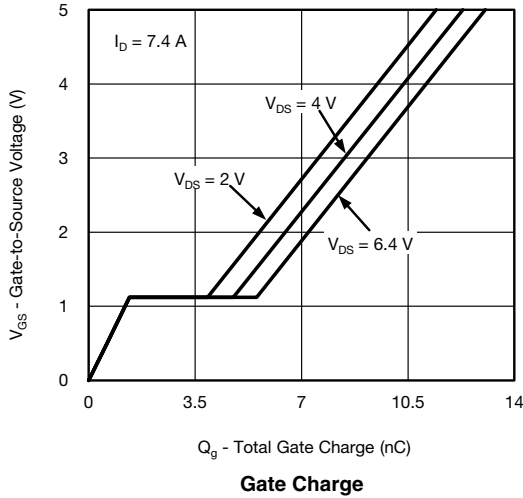


Capacitance

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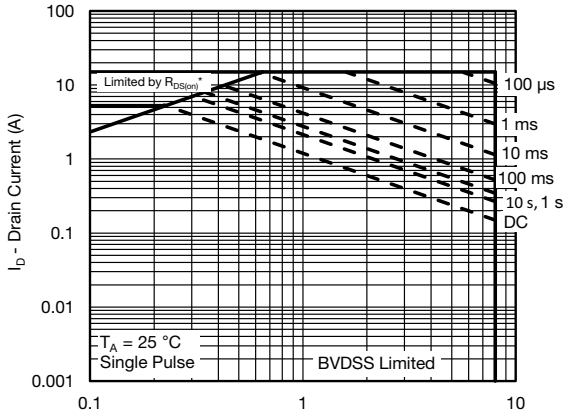
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





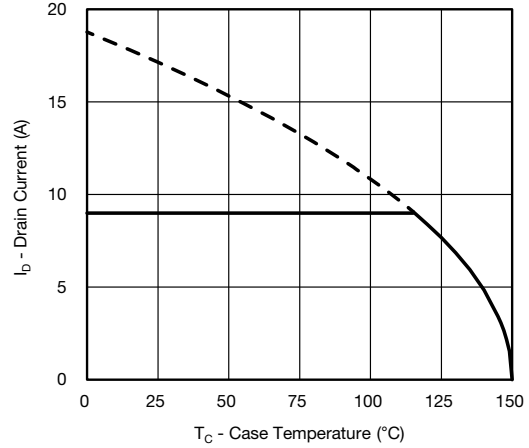
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

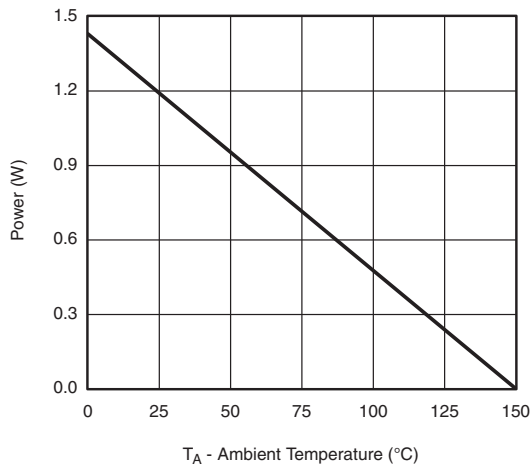


V_{DS} - Drain-to-Source Voltage (V)
 * V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

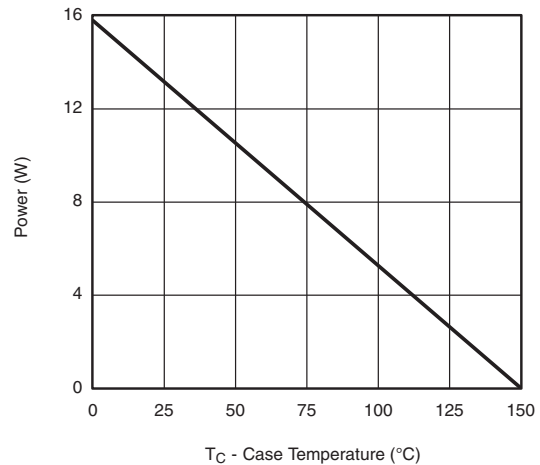
Safe Operating Area, Junction-to-Case



Current Derating**



Power Junction-to-Ambient



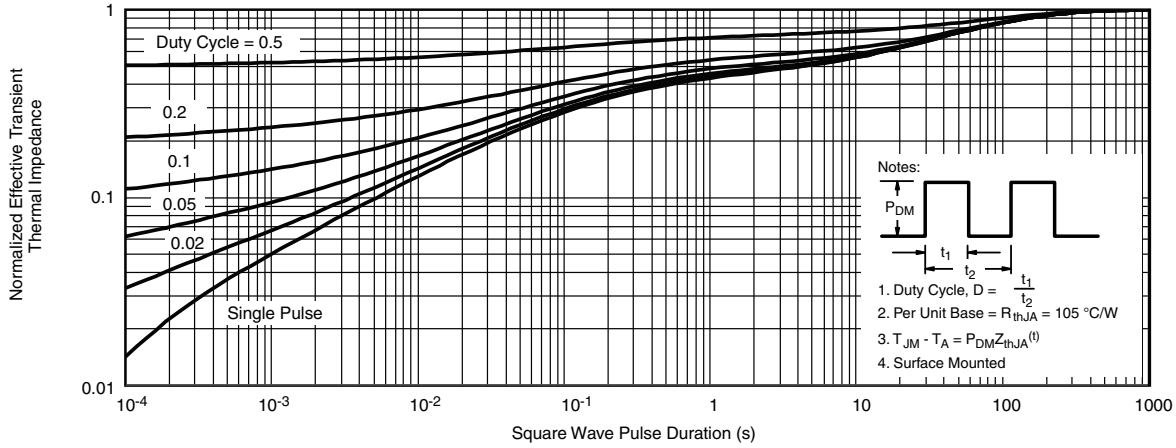
Power Junction-to-Case

** The power dissipation P_D is based on $T_{J(max.)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

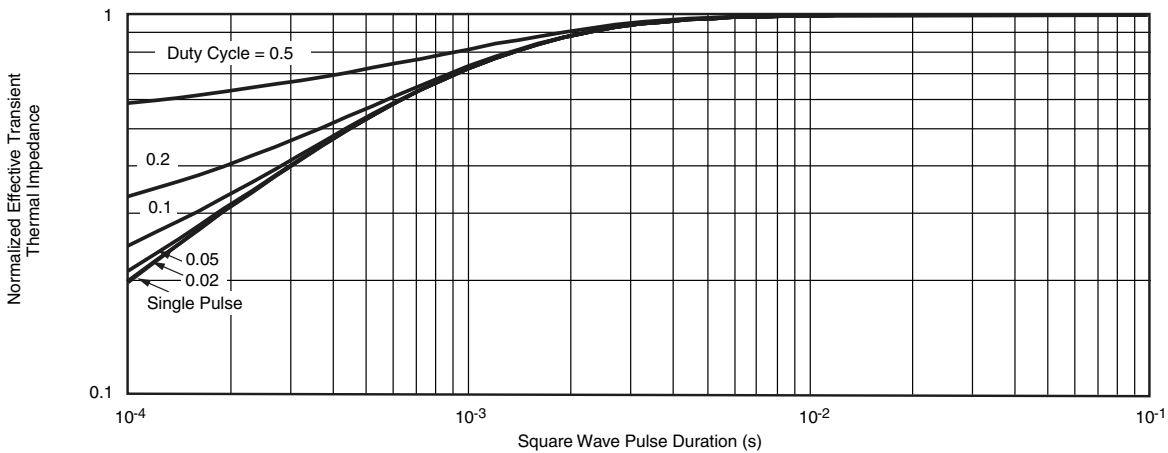
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

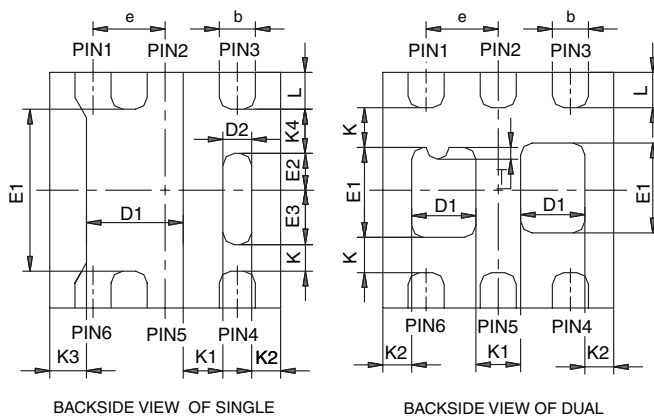
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg263899.



Package Information

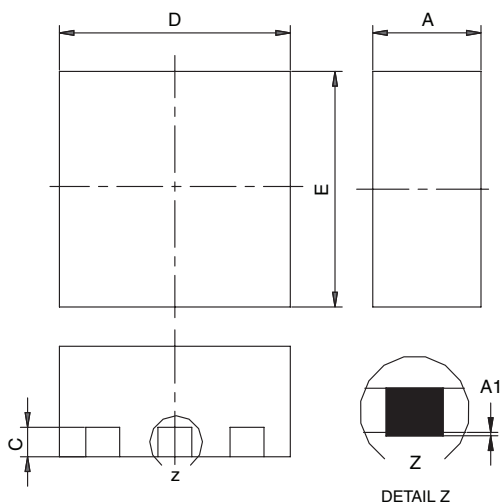
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PowerPAK[®] SC75-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- Notes:
 1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

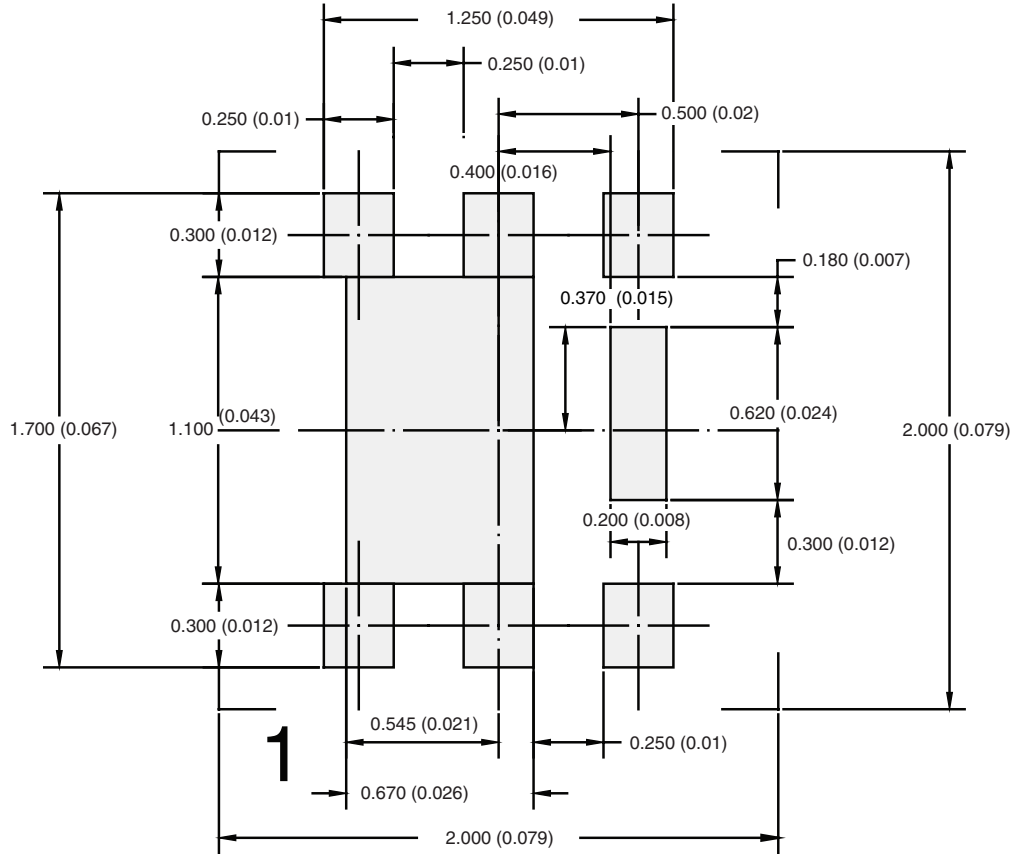
ECN: C-07431 – Rev. C, 06-Aug-07
 DWG: 5935



Application Note 826

Vishay Siliconix

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Single



Dimensions in mm/(Inches)

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APPLICATION NOTE



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