Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

Texas Instruments
TMDXHVMTRKIT5X

For any questions, you can email us directly:
sales@integrated-circuit.com

TMS320F2805x Piccolo™ Microcontrollers

1 Device Overview

1.1 Features

- High-Efficiency 32-Bit CPU (TMS320C28x)
  - 60 MHz (16.67-ns Cycle Time)
  - 16 x 16 and 32 x 32 MAC Operations
  - 16 x 16 Dual MAC
  - Harvard Bus Architecture
  - Atomic Operations
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - Code-Efficient (in C/C++ and Assembly)
- Programmable Control Law Accelerator (CLA)
  - 32-Bit Floating-Point Math Accelerator
  - Executes Code Independently of the Main CPU
- Dual-Zone Security Module
- Endianness: Little Endian
- Low Device and System Cost:
  - Single 3.3-V Supply
  - No Power Sequencing Requirement
  - Integrated Power-on Reset and Brown-out Reset
  - Low Power
  - No Analog Support Pins
- Clocking:
  - Two Internal Zero-Pin Oscillators
  - On-Chip Crystal Oscillator and External Clock Input
  - Watchdog Timer Module
  - Missing Clock Detection Circuitry
- Up to 42 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins With Input Filtering
- JTAG Boundary Scan Support
  - IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture
- Peripheral Interrupt Expansion (PIE) Block That Supports All Peripheral Interrupts
- Three 32-Bit CPU Timers
- Independent 16-Bit Timer in Each ePWM Module
- On-Chip Memory
  - Flash, SARAM, Message RAM, OTP, CLA Data ROM, Boot ROM, Secure ROM Available
- 128-Bit Security Key and Lock
  - Protects Secure Memory Blocks
  - Prevents Firmware Reverse Engineering
- Serial Port Peripherals
  - Three Serial Communications Interface (SCI) (Universal Asynchronous Receiver/Transmitter [UART]) Modules
  - One Serial Peripheral Inteface (SPI) Module
  - One Inter-Integrated-Circuit (I^2C) Bus
  - One Enhanced Controller Area Network (eCAN) Bus
- Enhanced Control Peripherals
  - Enhanced Pulse Width Modulator (ePWM)
  - Enhanced Capture (eCAP) Module
  - Enhanced Quadrature Encoder Pulse (eQEP) Module
- Analog Peripherals
  - One 12-Bit Analog-to-Digital Converter (ADC)
  - One On-Chip Temperature Sensor for Oscillator Compensation
  - Up to Seven Comparators With up to Three Integrated Digital-to-Analog Converters (DACs)
  - One Buffered Reference DAC
  - Up to Four Programmable Gain Amplifiers (PGAs)
  - Up to Four Digital Filters
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug via Hardware
- 80-Pin PN Low-Profile Quad Flatpack (LQFP)

1.2 Applications

- White Goods
- Solar Microinverters and Converters
- Sewing and Textile Machines
- AC/DC Inverters
- General Motor Control

1.3 Description

The F2805x Piccolo™ family of microcontrollers (MCUs) provides the power of the C28x core and CLA coupled with highly integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code, and also provides a high level of analog integration.

An internal voltage regulator allows for single-rail operation. Analog comparators with internal 6-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0 to 3.3-V fixed full-scale range and supports ratio-metric V_{REFHI}/V_{REFLO} references. The ADC interface has been optimized for low overhead and latency.

The Analog Front End (AFE) contains up to seven comparators with up to three integrated DACs, one VREFOUT-buffered DAC, up to four PGAs, and up to four digital filters. The PGAs can amplify the input signal in three discrete gain modes. The actual number of AFE peripherals will depend upon the TMS320F2805x device number. See Section 8 for more details.

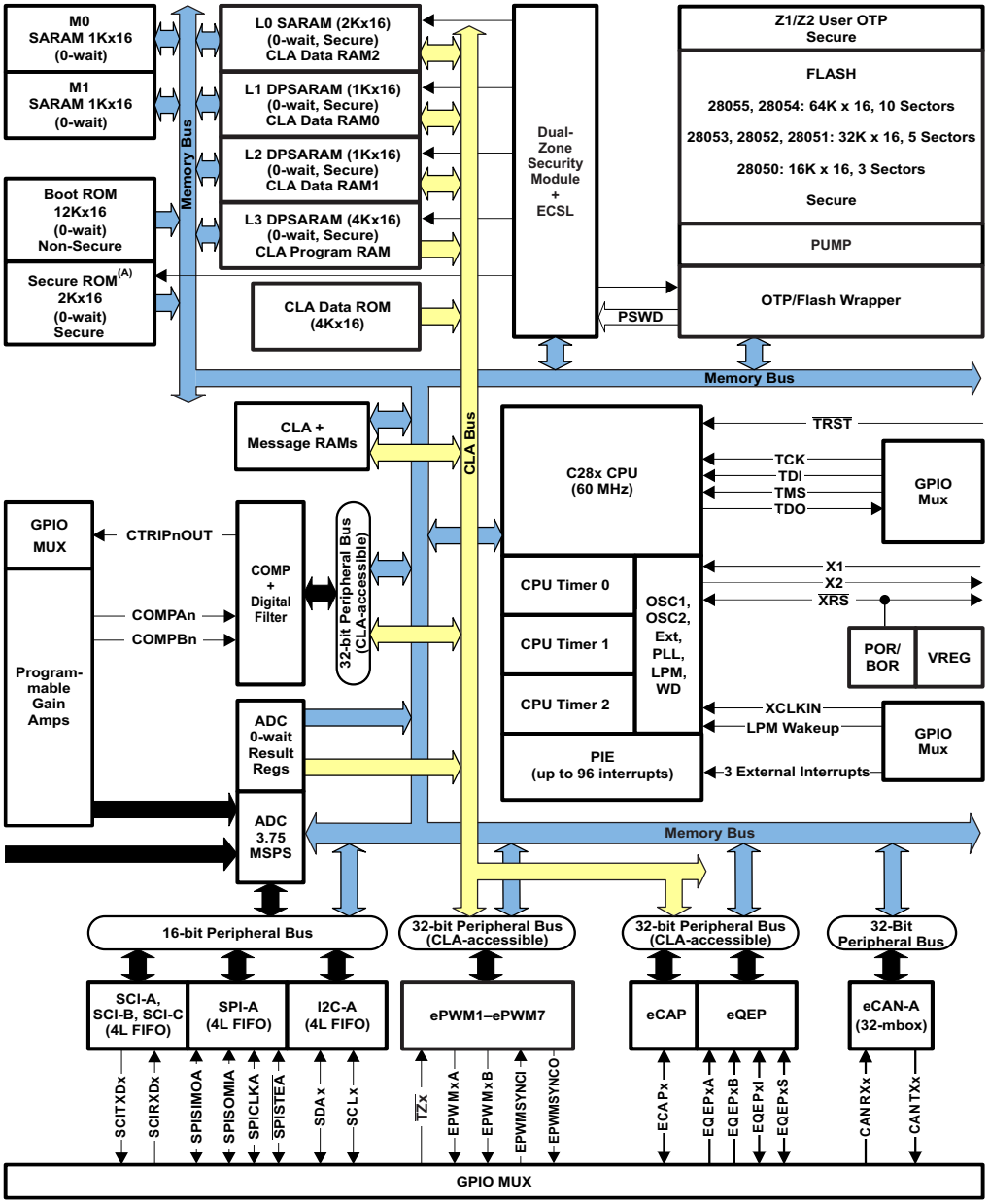
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TMS320F28055PN	LQFP (80)	12.0 mm x 12.0 mm
TMS320F28054PN	LQFP (80)	12.0 mm x 12.0 mm
TMS320F28053PN	LQFP (80)	12.0 mm x 12.0 mm
TMS320F28052PN	LQFP (80)	12.0 mm x 12.0 mm
TMS320F28051PN	LQFP (80)	12.0 mm x 12.0 mm

(1) For more information on these devices, see Section 8, Mechanical Packaging and Orderable Information.

1.4 Functional Block Diagram

Figure 1-1 shows a functional block diagram of the device.



A. Stores Secure Copy Code Functions on all devices.
B. Not all peripheral pins are available at the same time due to multiplexing.

Figure 1-1. Functional Block Diagram

Table of Contents

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data sheet revision history highlights the technical changes made to the SPRS797A device-specific data sheet to make it an SPRS797B revision.

Scope: Added InstaSPIN-MOTION™ devices TMS320F28054M and TMS320F28052M. See Table 3-1.

Added InstaSPIN-FOC™ devices TMS320F28054F and TMS320F28052F. See Table 3-1.

TMS320F2805x devices are now available in the Q temperature range (–40°C to 125°C, Q100 qualification for automotive applications). See Table 3-1.

Added Section 7.3, Related Links, which provides quick access to available resources.

Restructured document.

See the following table.

LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Global	• Restructured document • TMS320F2805x devices are now available in the Q temperature range (–40°C to 125°C, Q100 qualification for automotive applications). See Table 3-1. • Removed *Reliability Data for TMS320LF24xx and TMS320F28xx Devices* Application Report (SPRA963)
Section 1	Changed section title from "TMS320F2805x (Piccolo) Microcontrollers" to "Device Overview"
Section 1.1	Features: • Clocking: – Removed "Dynamic Phase-Locked Loop (PLL) Ratio Changes Supported"
Section 1.2	Added "Applications" section
Section 1.3	Description: • Added "Device Information" table
Section 3	Added "Device Comparison" section
Table 3-1	Changed title from "TMS320F2805x Hardware Features" to "Device Comparison"
Table 3-1	Device Comparison: • Added InstaSPIN-MOTION devices TMS320F28054M and TMS320F28052M • Added InstaSPIN-FOC devices TMS320F28054F and TMS320F28052F • Added "Q: –40ºC to 125ºC" to Temperature options • Added footnote with reference to a list of InstaSPIN™ Technical Reference Manuals (Section 7.2) • Added footnote about Q100 qualification
Section 4	Changed section title from "Device Pins" to "Terminal Configuration and Functions"
Section 4.1	Changed section title from "Terminal Functions" (Section 3.2 in SPRS797A) to "Signal Descriptions".
Table 4-1	Changed table title from "Terminal Functions" to "Signal Descriptions"
Table 4-1	Signal Descriptions: • Pin 8 ($\overline{XRS}$): Updated "I/O/Z" column and DESCRIPTION • Pins 6, 54, 73 (V_{DD}): Updated DESCRIPTION • Pin 42 (GPIO28): Changed SDAA from "I/OD" to "I/OC" • Pin 41 (GPIO29): Changed SCLA from "I/OD" to "I/OC" • Pin 2 (GPIO32): Changed SDAA from "I/OD" to "I/OC" • Pin 3 (GPIO33): Changed SCLA from "I/OD" to "I/OC" • Added definition of "OC" to footnote
Section 5	Changed title from "Device Operating Conditions" (Section 4 in SPRS797A) to "Specifications"
Section 5.1	Absolute Maximum Ratings: • Moved Storage temperature range, T_{stg}, to the new "Handling Ratings" section
Section 5.2	Added "Handling Ratings" section
Section 5.3	Recommended Operating Conditions: • Added Junction temperature, T_J, for Q version
Section 5.5	Changed title from "Thermal Model 80-Pin PN Results" (Table 9-1 in SPRS797A) to "Thermal Resistance Characteristics for PN Package"

LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Section 5.5	Thermal Resistance Characteristics for PN Package: • Reformatted table • Added footnotes
Table 5-7	Internal Zero-Pin Oscillator (INTOSC1, INTOSC2) Characteristics: • Accuracy using oscillator compensation: – Removed "TBD" from MAX column
Table 5-13	Added "Flash/OTP Endurance for Q Temperature Material" table
Table 5-14	Flash Parameters at 60-MHz SYSCLKOUT: • Updated "Typical parameters as seen at room temperature ..." footnote
Table 6-13	Device Emulation Registers: • Added PARTID for 28054M, 28054F, 28052M, and 28052F devices
Figure 6-5	Updated "VREG + POR + BOR + Reset Signal Connectivity" figure
Figure 6-11	Updated "CPU-watchdog Module" figure
Section 6.9	Changed title from "Peripheral Information and Timings" (Section 6 in SPRS797A) to "Peripherals"
Table 6-44	PGA Gain Stage: DC Accuracy Across Gain Settings: • Changed "COMPENSATED GAIN-ERROR **DRIFT** ACROSS TEMPERATURE AND SUPPLY VARIATIONS" column heading to "COMPENSATED GAIN-ERROR ACROSS TEMPERATURE AND SUPPLY VARIATIONS"
Table 6-45	Electrical Characteristics of the Comparator/DAC: • Removed "Input Offset" • Removed "Input Hysteresis"

LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Table 6-68	GPIOA MUX: • Updated **PERIPHERAL SELECTION 1** for the following **GPAMUX1** REGISTER BITS: – 25-24: Changed "$\overline{TZ1}$ (I)" to "$\overline{TZ1}$ (I)/CTRIPM1OUT (O)" – 29-28: Changed "$\overline{TZ3}$ (I)" to "$\overline{TZ3}$ (I)/CTRIPPFCOUT (O)" – 31-30: Changed "$\overline{TZ1}$ (I)" to "$\overline{TZ1}$ (I)/CTRIPM1OUT (O)" • Updated **PERIPHERAL SELECTION 2** for the following **GPAMUX1** REGISTER BITS: – 19-18: Changed "Reserved" to "SCITXDB (O)" – 23-22: Changed "Reserved" to "SCIRXDB (I)" – 29-28: Changed "Reserved" to "SCITXDB (O)" – 31-30: Changed "Reserved" to "SCIRXDB (I)" • Updated **PERIPHERAL SELECTION 3** for the following **GPAMUX1** REGISTER BITS: – 3-2: Changed "COMP1OUT (O)" to "CTRIPM1OUT (O)" – 7-6: Changed "COMP2OUT (O)" to "Reserved" • Updated **PERIPHERAL SELECTION 2** for the following **GPAMUX2** REGISTER BITS: – 1-0: Changed "Reserved" to "EQEP1S (I/O)" – 3-2: Changed "Reserved" to "EQEP1I (I/O)" – 5-4: Changed "Reserved" to "SCITXDB (O)" – 7-6: Changed "Reserved" to "SCIRXDB (I)" – 9-8: Changed "Reserved" to "EPWM7A (O)" – 11-10: Changed "Reserved" to "EPWM7B (O)" – 17-16: Changed "Reserved" to "EPWM7A (O)" – 21-20: Changed "Reserved" to "SCIRXDC (O)" – 23-22: Changed "Reserved" to "SCITXDC (O)" – 25-24: Changed "SDAA (I/OD)" to "SDAA (I/OC)" – 27-26: Changed "SCLA (I/OD)" to "SCLA (I/OC)" – 29-28: Changed "Reserved" to "SCIRXDB (I)" – 31-30: Changed "Reserved" to "SCITXDB (I)" • Updated **PERIPHERAL SELECTION 3** for the following **GPAMUX2** REGISTER BITS: – 3-2: Changed "$\overline{TZ3}$ (I)" to "$\overline{TZ3}$ (I)/CTRIPPFCOUT (O)" – 9-8: Changed "COMP1OUT (O)" to "CTRIPM1OUT (O)" – 11-10: Changed "COMP2OUT (O)" to "Reserved" – 13-12: Changed "Reserved" to "SCITXDB (O)" – 15-14: Changed "Reserved" to "SCIRXDB (I)" – 27-26: Changed "$\overline{TZ3}$ (I)" to "$\overline{TZ3}$ (I)/CTRIPPFCOUT (O)" – 29-28: Changed "Reserved" to "EPWM7A (O)" – 31-30: Changed "Reserved" to "EPWM7B (O)" • Added definition of "OC" to footnote
Table 6-69	GPIOB MUX: • Updated **PERIPHERAL SELECTION 1** for the following **GPBMUX1** REGISTER BITS: – 1-0: Changed "SDAA (I/OD)" to "SDAA (I/OC)" – 3-2: Changed "SCLA (I/OD)" to "SCLA (I/OC)" – 5-4: Changed "COMP2OUT (O)" to "Reserved" – 17-16: Changed "Reserved" to "EPWM7A (O)" – 19-18: Changed "EPWM7B (O)" to "Reserved" • Updated **PERIPHERAL SELECTION 2** for the following **GPBMUX1** REGISTER BITS: – 15-14: Changed "Reserved" to "SCIRXDC (I)" • Updated **PERIPHERAL SELECTION 3** for the following **GPBMUX1** REGISTER BITS: – 1-0: Changed "$\overline{ADCSOCAO}$ (O)" to "EQEP1S (I/O)" – 3-2: Changed "$\overline{ADCSOCBO}$ (O)" to "EQEP1I (I/O)" – 5-4: Changed "COMP3OUT (O)" to "CTRIPPFCOUT (O)" – 15-14: Changed "Reserved" to "CTRIPPFCOUT (O)" – 21-20: Changed "COMP1OUT (O)" to "CTRIPM1OUT (O)" • Added definition of "OC" to footnote
Section 7	Device and Documentation Support: • Added Section 7.3, Related Links • Added "Trademarks" section • Added "Electrostatic Discharge Caution" section • Added "Glossary" section

LOCATION	ADDITIONS, DELETIONS, AND MODIFICATIONS
Figure 7-1	Device Nomenclature: • Added "Q = −40°C to 125°C (Q refers to Q100 qualification for automotive applications.)" under TEMPERATURE RANGE
Section 7.2	Documentation Support: • Added InstaSPIN Technical Reference Manuals section: – Added *InstaSPIN-FOC™ and InstaSPIN-MOTION™ User's Guide* (SPRUHJ1) – Added *TMS320F28054F, TMS320F28052F InstaSPIN-FOC™ Software Technical Reference Manual* (SPRUHW0) – Added *TMS320F28054M, TMS320F28052M InstaSPIN-MOTION™ Software Technical Reference Manual* (SPRUHW1) • Added Application Reports section: – Added *Semiconductor Packing Methodology* Application Report (SZZA021)

3 Device Comparison

Table 3-1 lists the features of the TMS320F2805x devices.

Table 3-1. Device Comparison

FEATURE		28055 (60 MHz)	28054 28054M(1) 28054F(1) (60 MHz)	28053 (60 MHz)	28052 28052M(1) 28052F(1) (60 MHz)	28051 (60 MHz)	28050 (60 MHz)
Package Type		80-Pin PN LQFP	80-Pin PN LQFP	80-Pin PN LQFP	80-Pin PN LQFP	80-Pin PN LQFP	80-Pin PN LQFP
Instruction cycle		16.67 ns	16.67 ns	16.67 ns	16.67 ns	16.67 ns	16.67 ns
CLA		Yes	No	Yes	No	No	No
On-chip flash (16-bit word)		64K	64K	32K	32K	32K	16K
On-chip SARAM (16-bit word)		10K	10K (28054) 8K (28054M) 8K (28054F)	10K	10K (28052) 8K (28052M) 8K (28052F)	8K	6K
Dual-zone security for on-chip Flash, SARAM, OTP, and Secure ROM blocks		Yes	Yes	Yes	Yes	Yes	Yes
Boot ROM (12K x 16)		Yes	Yes	Yes	Yes	Yes	Yes
One-time programmable (OTP) ROM (16-bit word)		1K	1K	1K	1K	1K	1K
ePWM channels		14	14	14	14	14	14
eCAP inputs		1	1	1	1	1	1
eQEP modules		1	1	1	1	1	1
Watchdog timer		Yes	Yes	Yes	Yes	Yes	Yes
12-Bit ADC	MSPS	3.75	3.75	3.75	3.75	2	2
	Conversion Time	267 ns	267 ns	267 ns	267 ns	500 ns	500 ns
	Channels	16	16	16	16	16	16
	Temperature Sensor	Yes	Yes	Yes	Yes	Yes	Yes
	Dual Sample-and-Hold	Yes	Yes	Yes	Yes	Yes	Yes
PGA (Gains = ~3, ~6, ~11)		4	4	4	4	4	3
Fixed Gain Amplifier (Gain = ~3)		3	3	3	3	3	4
Comparators		7	7	7	7	7	6
Internal Comparator Reference DACs		3	3	3	3	3	2
Buffered Reference DAC		1	1	1	1	1	1
32-Bit CPU timers		3	3	3	3	3	3
I^2C		1	1	1	1	1	1
eCAN		1	1	1	1	1	1

(1) TMS320F2805xM devices are InstaSPIN-MOTION-enabled MCUs. TMS320F2805xF devices are InstaSPIN-FOC-enabled MCUs. For more information, see Section 7.2 for a list of InstaSPIN Technical Reference Manuals.

Table 3-1. Device Comparison (continued)

FEATURE		28055 (60 MHz)	28054 28054M(1) 28054F(1) (60 MHz)	28053 (60 MHz)	28052 28052M(1) 28052F(1) (60 MHz)	28051 (60 MHz)	28050 (60 MHz)
SPI		1	1	1	1	1	1
SCI		3	3	3	3	3	3
0-pin Oscillators		2	2	2	2	2	2
I/O pins (shared)	GPIO	42	42	42	42	42	42
External interrupts		3	3	3	3	3	3
Supply voltage (nominal)		3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Temperature options	T: –40ºC to 105ºC	Yes	Yes	Yes	Yes	Yes	Yes
	S: –40ºC to 125ºC	Yes	Yes (28054 only)	Yes	Yes (28052 only)	Yes	Yes
	Q: –40ºC to 125ºC(2)	Yes	Yes	Yes	Yes	Yes	Yes
Product status(3)		TMS	TMS	TMS	TMS	TMS	TMS

(2) "Q" refers to Q100 qualification for automotive applications.
(3) See Section 7.1.2, Device and Development Support Tool Nomenclature, for descriptions of device stages. The "TMS" product status denotes a fully qualified production device.

4 Terminal Configuration and Functions

Figure 4-1 shows the 80-pin PN Low-Profile Quad Flatpack pin assignments.

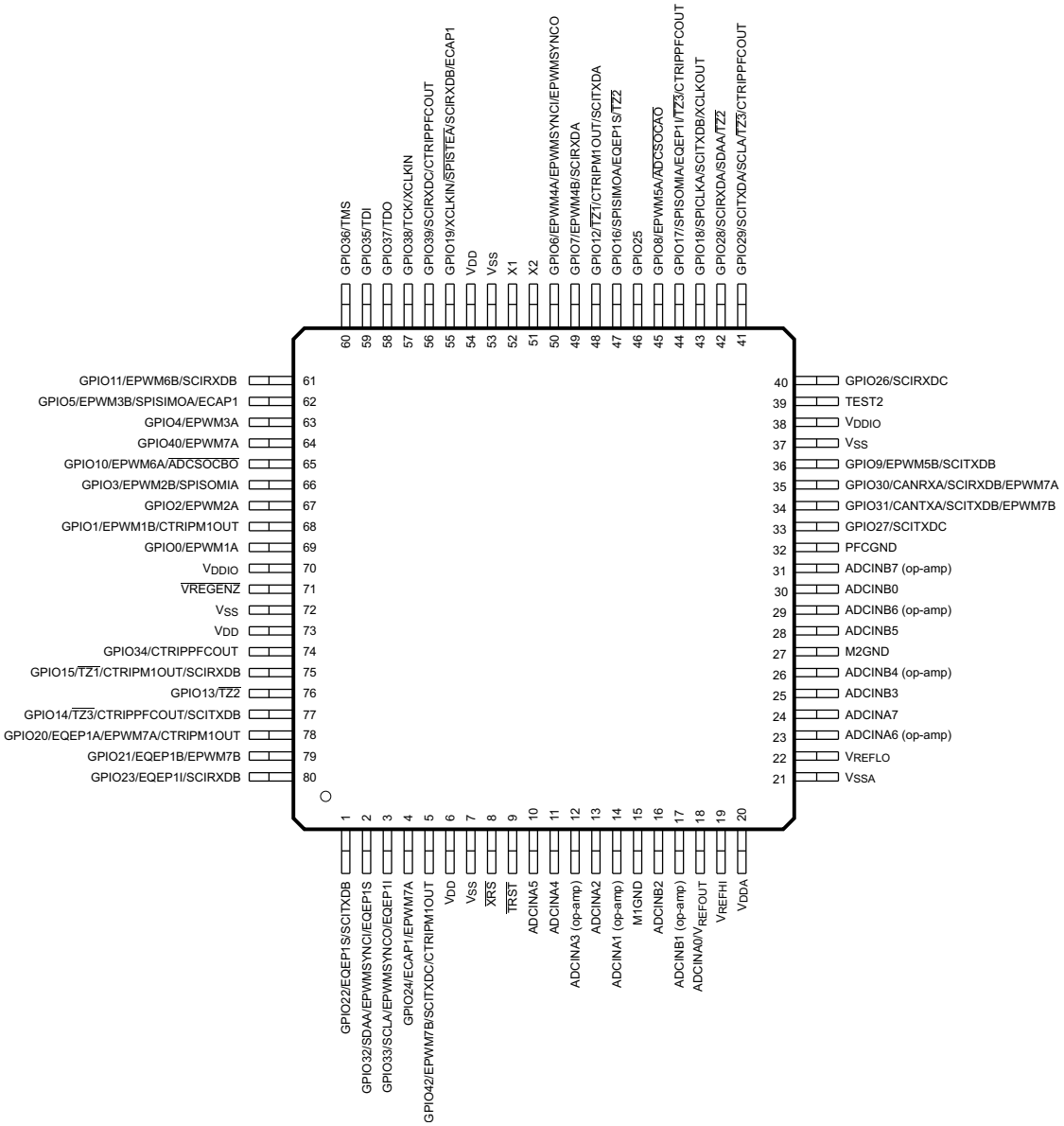


Figure 4-1. 2805x 80-Pin PN Low-Profile Quad Flatpack (Top View)

4.1 Signal Descriptions

Table 4-1 describes the signals. With the exception of the JTAG pins, the GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. See Table 3-1 for details. Inputs are not 5-V tolerant. All GPIO pins are I/O/Z and have an internal pullup (PU), which can be selectively enabled or disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups on the PWM pins are not enabled at reset. The pullups on other GPIO pins are enabled upon reset.

NOTE: When the on-chip VREG is used, the GPIO19, GPIO34, GPIO35, GPIO36, GPIO37, and GPIO38 pins could glitch during power up. If this behavior is unacceptable in an application, 1.8 V could be supplied externally. There is no power-sequencing requirement when using an external 1.8-V supply. However, if the 3.3-V transistors in the level-shifting output buffers of the I/O pins are powered prior to the 1.9-V transistors, it is possible for the output buffers to turn on, causing a glitch to occur on the pin during power up. To avoid this behavior, power the V_{DD} pins prior to or simultaneously with the V_{DDIO} pins, ensuring that the V_{DD} pins have reached 0.7 V before the V_{DDIO} pins reach 0.7 V.

Table 4-1. Signal Descriptions(1)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
JTAG			
$\overline{\text{TRST}}$	9	I	JTAG test reset with internal pulldown (PD). $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. **NOTE:** $\overline{\text{TRST}}$ is an active high test pin and must be maintained low at all times during normal device operation. An external pull-down resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since the value of the resistor is application-specific, TI recommends that each target board be validated for proper operation of the debugger and the application. (↓)
TCK	See GPIO38	I	See GPIO38. JTAG test clock with internal pullup. (↑)
TMS	See GPIO36	I	See GPIO36. JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.. (↑)
TDI	See GPIO35	I	See GPIO35. JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (↑)
TDO	See GPIO37	O/Z	See GPIO37. JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (8 mA drive)
FLASH			
TEST2	39	I/O	Test Pin. Reserved for TI. Must be left unconnected.

Table 4-1. Signal Descriptions[(1)] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
CLOCK			
XCLKOUT	See GPIO18	O/Z	See GPIO18. Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. The value of XCLKOUT is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.
XCLKIN	See GPIO19 and GPIO38	I	See GPIO19 and GPIO38. External oscillator input. Pin source for the clock is controlled by the XCLKINSEL bit in the XCLK register, GPIO38 is the default selection. This pin feeds a clock from an external 3.3-V oscillator. In this case, the X1 pin, if available, must be tied to GND and the on-chip crystal oscillator must be disabled via bit 14 in the CLKCTL register. If a crystal/resonator is used, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. **NOTE:** Designs that use the GPIO38/TCK/XCLKIN pin to supply an external clock for normal device operation may need to incorporate some hooks to disable this path during debug using the JTAG connector. This action is to prevent contention with the TCK signal, which is active during JTAG debug sessions. The zero-pin internal oscillators may be used during this time to clock the device.
X1	52	I	On-chip crystal-oscillator input. To use this oscillator, a quartz crystal or a ceramic resonator must be connected across X1 and X2. In this case, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. If this pin is not used, this pin must be tied to GND. (I)
X2	51	O	On-chip crystal-oscillator output. A quartz crystal or a ceramic resonator must be connected across X1 and X2. If X2 is not used, X2 must be left unconnected. (O)
RESET			
$\overline{\text{XRS}}$	8	I/OD	Device Reset (in) and Watchdog Reset (out). Piccolo devices have a built-in power-on reset (POR) and brown-out reset (BOR) circuitry. During a power-on or brown-out condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between $\overline{\text{XRS}}$ and V_{DDIO}. If a capacitor is placed between $\overline{\text{XRS}}$ and V_{SS} for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{\text{XRS}}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Regardless of the source, a device reset causes the device to terminate execution. The program counter points to the address contained at the location 0x3F FFC0. When reset is deactivated, execution begins at the location designated by the program counter. The output buffer of this pin is an open-drain with an internal pullup. (↑)

Table 4-1. Signal Descriptions[(1)] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
ADC, COMPARATOR, ANALOG I/O			
ADCINA7	24	I	ADC Group A, Channel 7 input
ADCINA6 (op-amp)	23	I	ADC Group A, Channel 6 input
ADCINA5	10	I	ADC Group A, Channel 5 input
ADCINA4	11	I	ADC Group A, Channel 4 input
ADCINA3 (op-amp)	12	I	ADC Group A, Channel 3 input
ADCINA2	13	I	ADC Group A, Channel 2 input
ADCINA1 (op-amp)	14	I	ADC Group A, Channel 1 input
ADCINA0 V_{REFOUT}	18	I	ADC Group A, Channel 0 input Voltage Reference out from buffered DAC
V_{REFHI}	19	I	ADC External Reference – used when in ADC external reference mode and used as V_{REFOUT} reference
ADCINB7 (op-amp)	31	I	ADC Group B, Channel 7 input
ADCINB6 (op-amp)	29	I	ADC Group B, Channel 6 input
ADCINB5	28	I	ADC Group B, Channel 5 input
ADCINB4 (op-amp)	26	I	ADC Group B, Channel 4 input
ADCINB3	25	I	ADC Group B, Channel 3 input
ADCINB2	16	I	ADC Group B, Channel 2 input
ADCINB1 (op-amp)	17	I	ADC Group B, Channel 1 input
ADCINB0	30	I	ADC Group B, Channel 0 input
V_{REFLO}	22	I	ADC Low Reference (always tied to ground)
CPU AND I/O POWER			
V_{DDA}	20		Analog Power Pin. Tie with a 2.2-µF capacitor (typical) close to the pin.
V_{SSA}	21		Analog Ground Pin
V_{DD}	6		CPU and Logic Digital Power Pins. When using internal VREG, place one 1.2-µF capacitor between each V_{DD} pin and ground. Higher value capacitors may be used.
	54		
	73		
V_{DDIO}	38		Digital I/O and Flash Power Pin – Single Supply source when VREG is enabled
	70		
V_{SS}	7		Digital Ground Pins
	37		
	53		
	72		
M1GND	15		Ground pin for amplifier (channels A1, A3, B1)
M2GND	27		Ground pin for amplifier (channels A6, B4, B6)
PFCGND	32		Ground pin for amplifier (channel B7)
VOLTAGE REGULATOR CONTROL SIGNAL			
$\overline{VREGENZ}$	71	I	Internal VREG Enable/Disable – pull low to enable VREG, pull high to disable VREG

Table 4-1. Signal Descriptions[1] (continued)

TERMINAL NAME	TERMINAL PN PIN NO.	I/O/Z	DESCRIPTION
GPIO AND PERIPHERAL SIGNALS[2]			
GPIO0	69	I/O/Z	General-purpose input/output 0
EPWM1A		O	Enhanced PWM1 Output A
GPIO1	68	I/O/Z	General-purpose input/output 1
EPWM1B		O	Enhanced PWM1 Output B
CTRIPM1OUT		O	CTRIPM1 CTRIPxx output
GPIO2	67	I/O/Z	General-purpose input/output 2
EPWM2A		O	Enhanced PWM2 Output A
GPIO3	66	I/O/Z	General-purpose input/output 3
EPWM2B		O	Enhanced PWM2 Output B
SPISOMIA		I/O	SPI-A slave out, master in
GPIO4	63	I/O/Z	General-purpose input/output 4
EPWM3A		O	Enhanced PWM3 output A
GPIO5	62	I/O/Z	General-purpose input/output 5
EPWM3B		O	Enhanced PWM3 output B
SPISIMOA		I/O	SPI-A slave in, master out
ECAP1		I/O	Enhanced Capture input/output 1
GPIO6	50	I/O/Z	General-purpose input/output 6
EPWM4A		O	Enhanced PWM4 output A
EPWMSYNCI		I	External ePWM sync pulse input
EPWMSYNCO		O	External ePWM sync pulse output
GPIO7	49	I/O/Z	General-purpose input/output 7
EPWM4B		O	Enhanced PWM4 output B
SCIRXDA		I	SCI-A receive data
GPIO8	45	I/O/Z	General-purpose input/output 8
EPWM5A		O	Enhanced PWM5 output A
$\overline{\text{ADCSOCAO}}$		O	ADC start-of-conversion A
GPIO9	36	I/O/Z	General-purpose input/output 9
EPWM5B		O	Enhanced PWM5 output B
SCITXDB		O	SCI-B transmit data
GPIO10	65	I/O/Z	General-purpose input/output 10
EPWM6A		O	Enhanced PWM6 output A
$\overline{\text{ADCSOCBO}}$		O	ADC start-of-conversion B
GPIO11	61	I/O/Z	General-purpose input/output 11
EPWM6B		O	Enhanced PWM6 output B
SCIRXDB		I	SCI-B receive data
GPIO12	48	I/O/Z	General-purpose input/output 12
$\overline{\text{TZ1}}$		I	Trip Zone input 1
CTRIPM1OUT		O	CTRIPM1 CTRIPxx output
SCITXDA		O	SCI-A transmit data
GPIO13	76	I/O/Z	General-purpose input/output 13
$\overline{\text{TZ2}}$		I	Trip zone input 2

Table 4-1. Signal Descriptions[(1)] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
GPIO14	77	I/O/Z	General-purpose input/output 14
$\overline{TZ3}$		I	Trip zone input 3
CTRIPPFCOUT		O	CTRIPPFC output
SCITXDB		O	SCI-B transmit data
GPIO15	75	I/O/Z	General-purpose input/output 15
$\overline{TZ1}$		I	Trip zone input 1
CTRIPM1OUT		O	CTRIPM1 CTRIPxx output
SCIRXDB		I	SCI-B receive data
GPIO16	47	I/O/Z	General-purpose input/output 16
SPISIMOA		I/O	SPI-A slave in, master out
EQEP1S		I/O	Enhanced QEP1 strobe
$\overline{TZ2}$		I	Trip Zone input 2
GPIO17	44	I/O/Z	General-purpose input/output 17
SPISOMIA		I/O	SPI-A slave out, master in
EQEP1I		I/O	Enhanced QEP1 index
$\overline{TZ3}$		I	Trip zone input 3
CTRIPPFCOUT		O	CTRIPPFC output
GPIO18	43	I/O/Z	General-purpose input/output 18
SPICLKA		I/O	SPI-A clock input/output
SCITXDB		O	SCI-B transmit data
XCLKOUT		O/Z	Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. The value of XCLKOUT is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.
GPIO19	55	I/O/Z	General-purpose input/output 19
XCLKIN		I	External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken not to enable this path for clocking if this path is being used for the other periperhal functions
$\overline{SPISTEA}$		I/O	SPI-A slave transmit enable input/output
SCIRXDB		I	SCI-B receive data
ECAP1		I/O	Enhanced Capture input/output 1
GPIO20	78	I/O/Z	General-purpose input/output 20
EQEP1A		I	Enhanced QEP1 input A
EPWM7A		O	Enhanced PWM7 output A
CTRIPM1OUT		O	CTRIPM1 CTRIPxx output
GPIO21	79	I/O/Z	General-purpose input/output 21
EQEP1B		I	Enhanced QEP1 input B
EPWM7B		O	Enhanced PWM7 output B
GPIO22	1	I/O/Z	General-purpose input/output 22
EQEP1S		I/O	Enhanced QEP1 strobe
SCITXDB		O	SCI-B transmit data
GPIO23	80	I/O/Z	General-purpose input/output 23
EQEP1I		I/O	Enhanced QEP1 index
SCIRXDB		I	SCI-B receive data

Table 4-1. Signal Descriptions[(1)] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
GPIO24	4	I/O/Z	General-purpose input/output 24
ECAP1		I/O	Enhanced Capture input/output 1
EPWM7A		O	Enhanced PWM7 output A
GPIO25	46	I/O/Z	General-purpose input/output 25
GPIO26	40	I/O/Z	General-purpose input/output 26
SCIRXDC		I	SCI-C receive data
GPIO27	33	I/O/Z	General-purpose input/output 27
SCITXDC		O	SCI-C transmit data
GPIO28	42	I/O/Z	General-purpose input/output 28
SCIRXDA		I	SCI-A receive data
SDAA		I/OC	I^2C data open-drain bidirectional port
$\overline{TZ2}$		I	Trip zone input 2
GPIO29	41	I/O/Z	General-purpose input/output 29
SCITXDA		O	SCI-A transmit data
SCLA		I/OC	I^2C clock open-drain bidirectional port
$\overline{TZ3}$		I	Trip zone input 3
CTRIPPFCOUT		O	CTRIPPFC output
GPIO30	35	I/O/Z	General-purpose input/output 30
CANRXA		I	CAN receive
SCIRXDB		I	SCI-B receive data
EPWM7A		O	Enhanced PWM7 output A
GPIO31	34	I/O/Z	General-purpose input/output 31
CANTXA		O	CAN transmit
SCITXDB		O	SCI-B transmit data
EPWM7B		O	Enhanced PWM7 output B
GPIO32	2	I/O/Z	General-purpose input/output 32
SDAA		I/OC	I^2C data open-drain bidirectional port
EPWMSYNCI		I	Enhanced PWM external sync pulse input
EQEP1S		I/O	Enhanced QEP1 strobe
GPIO33	3	I/O/Z	General-Purpose Input/Output 33
SCLA		I/OC	I^2C clock open-drain bidirectional port
EPWMSYNCO		O	Enhanced PWM external synch pulse output
EQEP1I		I/O	Enhanced QEP1 index
GPIO34	74	I/O/Z	General-Purpose Input/Output 34
CTRIPPFCOUT		O	CTRIPPFC output
GPIO35	59	I/O/Z	General-Purpose Input/Output 35
TDI		I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK
GPIO36	60	I/O/Z	General-Purpose Input/Output 36
TMS		I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
GPIO37	58	I/O/Z	General-Purpose Input/Output 37
TDO		O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK (8 mA drive)

Table 4-1. Signal Descriptions[1] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
GPIO38	57	I/O/Z	General-Purpose Input/Output 38
TCK		I	JTAG test clock with internal pullup
XCLKIN		I	External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken to not enable this path for clocking if this path is being used for the other functions.
GPIO39	56	I/O/Z	General-Purpose Input/Output 39
SCIRXDC		I	SCI-C receive data
CTRIPPFCOUT		O	CTRIPPFC output
GPIO40	64	I/O/Z	General-Purpose Input/Output 40. Internal pullup enabled by default.
EPWM7A		O	Enhanced PWM7 output A
GPIO42	5	I/O/Z	General-Purpose Input/Output 42
EPWM7B		O	Enhanced PWM7 output B
SCITXDC		O	SCI-C transmit data
CTRIPM1OUT		O	CTRIPM1 CTRIPxx output

(1) I = Input, O = Output, Z = High Impedance, OC = Open Collector, OD = Open Drain, ↑ = Pullup, ↓ = Pulldown

(2) The GPIO function (shown in bold italics) is the default at reset. The peripheral signals that are listed under them are alternate functions. For JTAG pins that have the GPIO functionality multiplexed, the input path to the GPIO block is always valid. The output path from the GPIO block and the path to the JTAG block from a pin is enabled or disabled based on the condition of the $\overline{\text{TRST}}$ signal. See the System Control and Interrupts chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5) for details.

5 Specifications

5.1 Absolute Maximum Ratings(1) (2)

Supply voltage range, V_{DDIO} (I/O and Flash)	with respect to V_{SS}	–0.3 V to 4.6 V
Supply voltage range, V_{DD}	with respect to V_{SS}	–0.3 V to 2.5 V
Analog voltage range, V_{DDA}	with respect to V_{SSA}	–0.3 V to 4.6 V
Input voltage range, V_{IN} (3.3 V)		–0.3 V to 4.6 V
Output voltage range, V_O		–0.3 V to 4.6 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})(3)		±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO})		±20 mA
Junction temperature range, T_J (4)		–40°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ± 2 mA.
(4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *IC Package Thermal Metrics Application Report* (SPRA953).

5.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range(1)			–65	150	°C
V_{ESD}	Electrostatic discharge (ESD)(2) performance	Human Body Model (HBM), per AEC Q100-002(3)		–2	2	kV
		Charged Device Model (CDM), per AEC Q100-011	All pins	–500	500	V
			Corner pins on 80-pin PN: 1, 20, 21, 40, 41, 60, 61, 80	–750	750	V

(1) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *IC Package Thermal Metrics Application Report* (SPRA953).
(2) ESD measures device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
(3) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO} (1)		2.97	3.3	3.63	V
Device supply voltage CPU, V_{DD} (When internal VREG is disabled and 1.8 V is supplied externally)		1.71	1.8	1.995	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA} (1)		2.97	3.3	3.63	V
Analog ground, V_{SSA}			0		V
Device clock frequency (system clock)		2		60	MHz
High-level input voltage, V_{IH} (3.3 V)		2		V_{DDIO} + 0.3	V
Low-level input voltage, V_{IL} (3.3 V)		V_{SS} – 0.3		0.8	V
High-level output source current, $V_{OH} = V_{OH(MIN)}$, I_{OH}	All GPIO pins			–4	mA
	Group 2 (2)			–8	mA
Low-level output sink current, $V_{OL} = V_{OL(MAX)}$, I_{OL}	All GPIO pins			4	mA
	Group 2 (2)			8	mA
Junction temperature, T_J	T version	–40		105	°C
	S version	–40		125	
	Q version (Q100 qualification)	–40		125	

(1) V_{DDIO} and V_{DDA} should be maintained within approximately 0.3 V of each other.
(2) Group 2 pins are as follows: GPIO16, GPIO17, GPIO18, GPIO28, GPIO29, GPIO30, GPIO31, GPIO36, GPIO37

5.4 Electrical Characteristics (1)

Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = I_{OH}$ MAX		2.4			V
			I_{OH} = 50 µA		V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		$I_{OL} = I_{OL}$ MAX				0.4	V
I_{IL}	Input current (low level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All GPIO pins	–80	–140	–205	µA
				$\overline{XRS}$ pin	–230	–300	–375	
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, $V_{IN} = V_{DDIO}$				±2	µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, $V_{IN} = V_{DDIO}$		28	50	80	
I_{OZ}	Output current, pullup or pulldown disabled		$V_O = V_{DDIO}$ or 0 V				±2	µA
C_I	Input capacitance					2		pF
	V_{DDIO} BOR trip point		Falling V_{DDIO}			2.78		V
	V_{DDIO} BOR hysteresis					35		mV
	Supervisor reset release delay time		Time after BOR/POR/OVR event is removed to $\overline{XRS}$ release		400		800	µs
	VREG V_{DD} output		Internal VREG on			1.9		V

(1) When the on-chip VREG is used, its output is monitored by the POR/BOR circuit, which will reset the device should the core voltage (V_{DD}) go out of range.

5.5 Thermal Resistance Characteristics for PN Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	14.2	0
$R\Theta_{JB}$	Junction-to-board thermal resistance	21.9	0
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	49.9	0
		38.3	150
		36.7	250
		34.4	500
Psi_{JT}	Junction-to-package top	0.8	0
		1.18	150
		1.34	250
		1.62	500
Psi_{JB}	Junction-to-board	21.6	0
		20.7	150
		20.5	250
		20.1	500

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

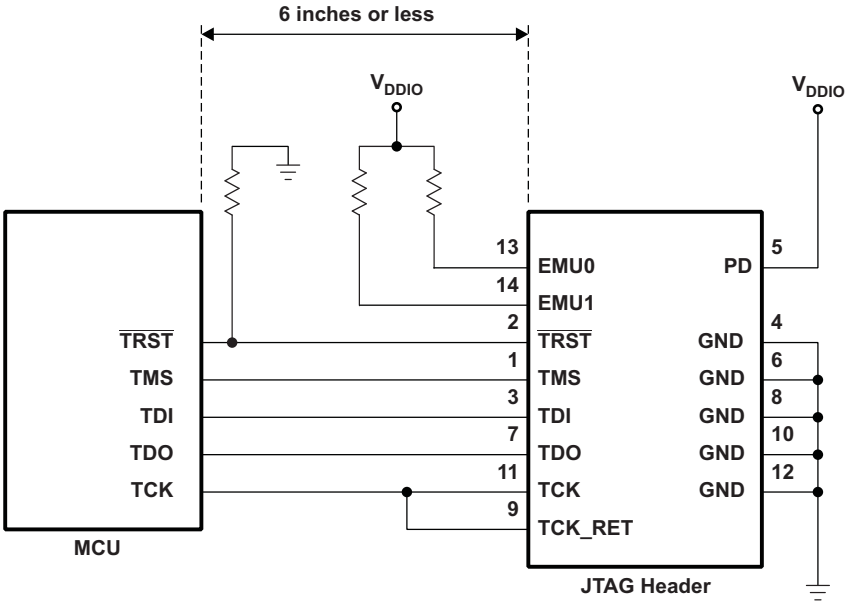
(2) lfm = linear feet per minute

5.6 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *IC Package Thermal Metrics* (SPRA953) helps to understand the thermal metrics and definitions.

5.7 Emulator Connection Without Signal Buffering for the MCU

Figure 5-1 shows the connection between the MCU and JTAG header for a single-processor configuration. If the distance between the JTAG header and the MCU is greater than 6 inches, the emulation signals must be buffered. If the distance is less than 6 inches, buffering is typically not needed. Figure 5-1 shows the simpler, no-buffering situation. For the pullup and pulldown resistor values, see Section 4.1.



A. See Figure 6-42 for JTAG/GPIO multiplexing.

Figure 5-1. Emulator Connection Without Signal Buffering for the MCU

NOTE

The 2805x devices do not have EMU0/EMU1 pins. For designs that have a JTAG Header on-board, the EMU0/EMU1 pins on the header must be tied to V_{DDIO} through a 4.7-kΩ (typical) resistor.

5.8 Current Consumption

Table 5-1. TMS320F2805x Current Consumption at 60-MHz SYSCLKOUT

MODE	TEST CONDITIONS	VREG ENABLED				VREG DISABLED					
		I_{DDIO} (1)		I_{DDA} (2)		I_{DD}		I_{DDIO} (1)		I_{DDA} (2)	
		TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM6, ePWM7 • eCAP1 • eQEP1 • eCAN-A • CLA • SCI-A, SCI-B, SCI-C • SPI-A • ADC • I2C-A • COMPA1, COMPA3, COMPB1, COMPB7 • CPU-TIMER0, CPU-TIMER1, CPU-TIMER2 All PWM pins are toggled at 60 kHz. All I/O pins are left unconnected. (4)(5) Code is running out of flash with 2 wait-states. XCLKOUT is turned off.	95 mA (6)	132 mA	40 mA	60 mA	85 mA (6)	110 mA	14 mA	25 mA	40 mA	60 mA
IDLE	Flash is powered down. XCLKOUT is turned off. All peripheral clocks are turned off.	14 mA	27 mA	15 µA	25 µA	14 mA	27 mA	120 µA	450 µA	15 µA	25 µA
STANDBY	Flash is powered down. Peripheral clocks are off.	9 mA	15 mA	15 µA	25 µA	9 mA	15 mA	120 µA	450 µA	15 µA	25 µA
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled. (7)	300 µA		15 µA	25 µA	50 µA		24 µA		15 µA	25 µA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) In order to realize the I_{DDA} currents shown for IDLE, STANDBY, and HALT, clock to the ADC module must be turned off explicitly by writing to the PCLKCR0 register.
(3) The TYP numbers are applicable over room temperature and nominal voltage.
(4) The following is done in a loop:
- Data is continuously transmitted out of SPI-A, SCI-A, SCI-B, SCI-C, eCAN-A, and I2C-A ports.
- The hardware multiplier is exercised.
- Watchdog is reset.
- ADC is performing continuous conversion.
- GPIO17 is toggled.

(5) CLA is continuously performing polynomial calculations.
(6) For F2805x devices that do not have CLA, subtract the I_{DD} current number for CLA (see Table 5-2) from the I_{DD} (VREG disabled)/I_{DDIO} (VREG enabled) current numbers shown in Table 5-1 for operational mode.
(7) If a quartz crystal or ceramic resonator is used as the clock source, the HALT mode shuts down the on-chip crystal oscillator.

NOTE

The peripheral-I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If the clocks to all the peripherals are turned on at the same time, the current drawn by the device will be more than the numbers specified in the current consumption tables.

5.8.1 Reducing Current Consumption

The 2805x devices incorporate a method to reduce the device current consumption. Since each peripheral unit has an individual clock-enable bit, significant reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application. Furthermore, any one of the three low-power modes could be taken advantage of to reduce the current consumption even further. Table 5-2 indicates the typical reduction in current consumption achieved by turning off the clocks.

Table 5-2. Typical Current Consumption by Various Peripherals (at 60 MHz)(1)

PERIPHERAL MODULE(2)	I_{DD} CURRENT REDUCTION (mA)
ADC	2(3)
I^2C	3
ePWM	2
eCAP	2
eQEP	2
SCI	2
SPI	2
COMP/DAC	1
PGA	2
CPU-TIMER	1
Internal zero-pin oscillator	0.5
CAN	2.5
CLA	20

(1) All peripheral clocks (except CPU Timer clock) are disabled upon reset. Writing to or reading from peripheral registers is possible only after the peripheral clocks are turned on.
(2) For peripherals with multiple instances, the current quoted is per module. For example, the 2 mA value quoted for ePWM is for one ePWM module.
(3) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA}) as well.

NOTE

I_{DDIO} current consumption is reduced by 15 mA (typical) when XCLKOUT is turned off.

NOTE

The baseline I_{DD} current (current when the core is executing a dummy loop with no peripherals enabled) is 40 mA, typical. To arrive at the I_{DD} current for a given application, the current-drawn by the peripherals (enabled by that application) must be added to the baseline I_{DD} current.

Following are other methods to reduce power consumption further:

- The flash module may be powered down if code is run off SARAM. This method results in a current reduction of 18 mA (typical) in the V_{DD} rail and 13 mA (typical) in the V_{DDIO} rail.
- Savings in I_{DDIO} may be realized by disabling the pullups on pins that assume an output function.

5.8.2 Current Consumption Graphs (VREG Enabled)

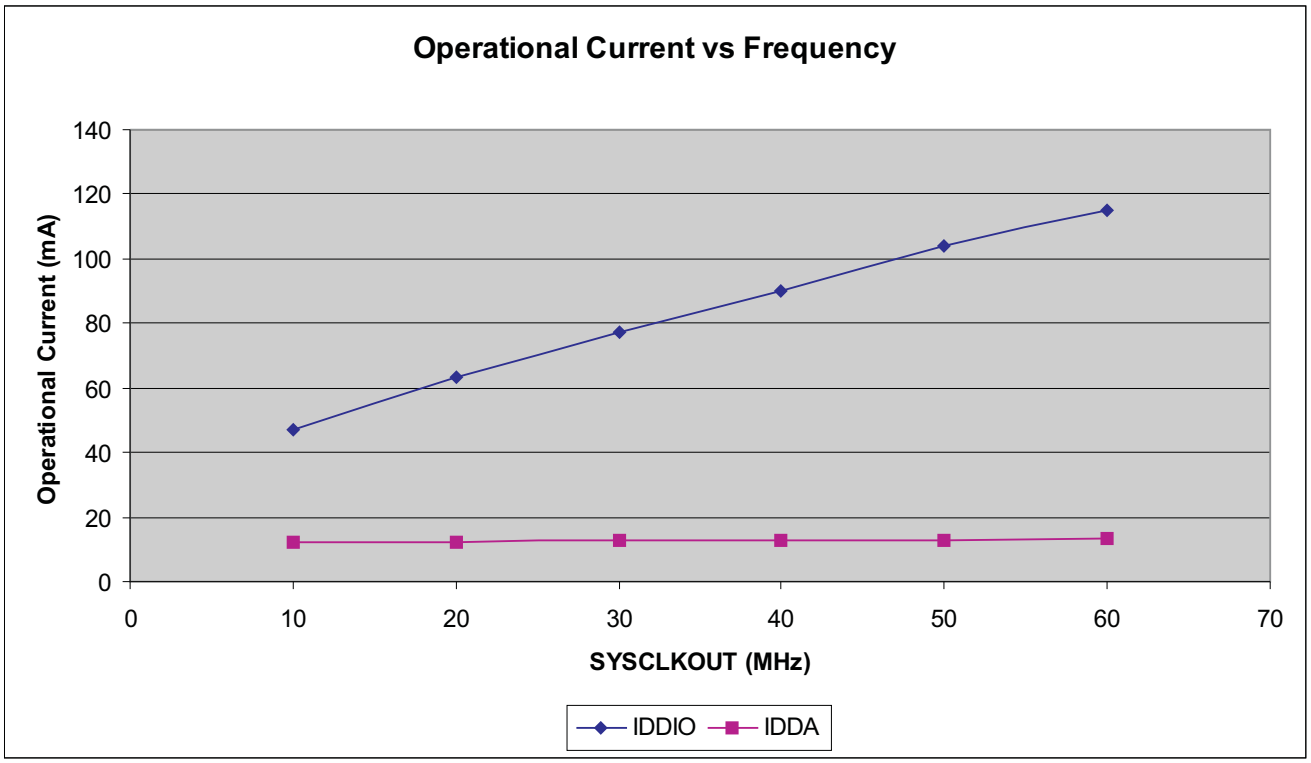


Figure 5-2. Typical Operational Current Versus Frequency (F2805x)

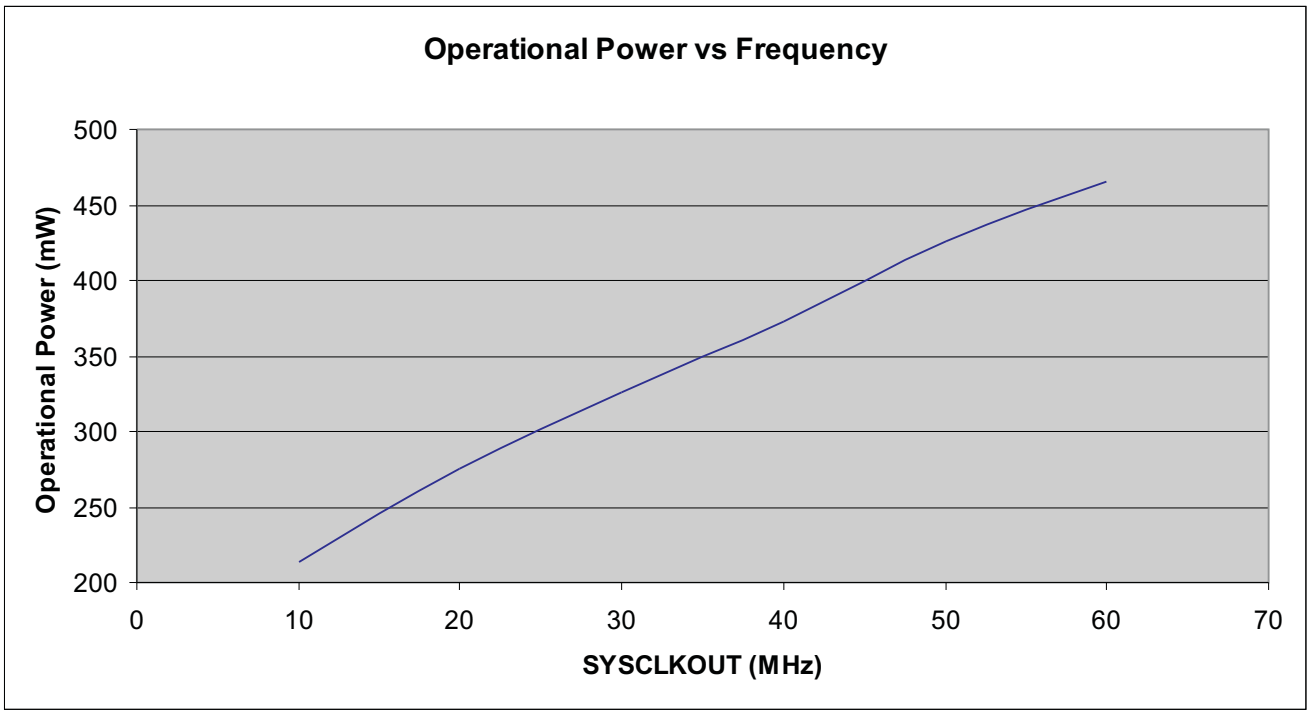


Figure 5-3. Typical Operational Power Versus Frequency (F2805x)

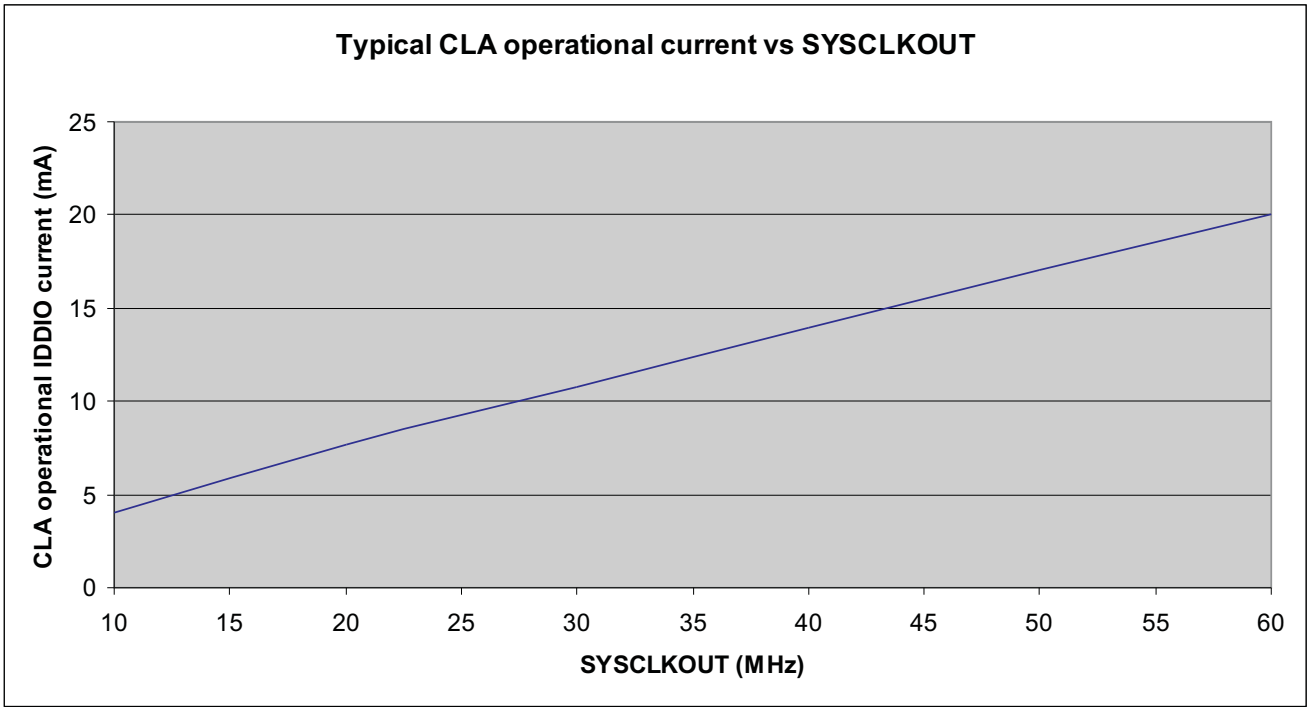


Figure 5-4. Typical CLA Operational Current Versus SYSCLKOUT

5.9 Parameter Information

5.9.1 Timing Parameter Symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:		Letters and symbols and their meanings:	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
f	fall time	X	Unknown, changing, or don't care level
h	hold time	Z	High impedance
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		

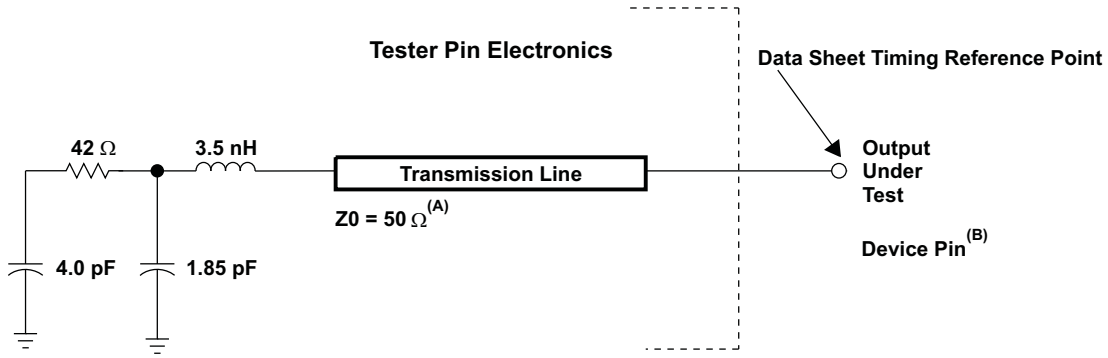
5.9.2 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, see the appropriate cycle description section of this document.

5.10 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.



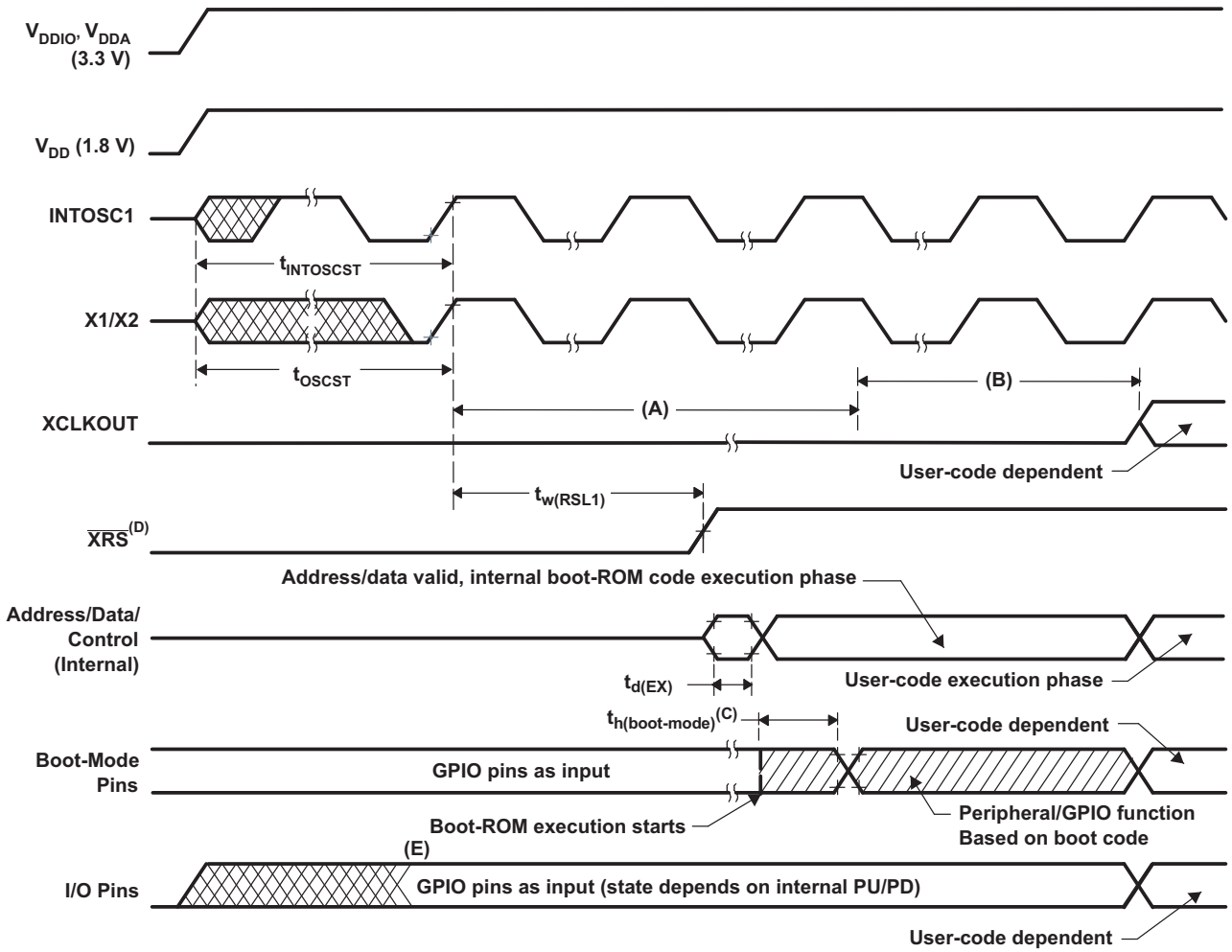
A. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

B. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timing.

Figure 5-5. 3.3-V Test Load Circuit

5.11 Power Sequencing

There is no power sequencing requirement needed to ensure the device is in the proper state after reset or to prevent the I/Os from glitching during power up or power down (GPIO19, GPIO34–38 do not have glitch-free I/Os). No voltage larger than a diode drop (0.7 V) above V_{DDIO} should be applied to any digital pin (for analog pins, this value is 0.7 V above V_{DDA}) prior to powering up the device. Voltages applied to pins on an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.



A. Upon power up, SYSCLKOUT is OSCCLK/4. Since the XCLKOUTDIV bits in the XCLK register come up with a reset state of 0, SYSCLKOUT is further divided by 4 before SYSCLKOUT appears at XCLKOUT. XCLKOUT = OSCCLK/16 during this phase.

B. Boot ROM configures the DIVSEL bits for /1 operation. XCLKOUT = OSCCLK/4 during this phase. Note that XCLKOUT will not be visible at the pin until explicitly configured by user code.

C. After reset, the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

D. Using the $\overline{\text{XRS}}$ pin is optional due to the on-chip POR circuitry.

E. The internal pullup or pulldown will take effect when BOR is driven high.

Figure 5-6. Power-on Reset

Table 5-3. Reset ($\overline{XRS}$) Timing Requirements

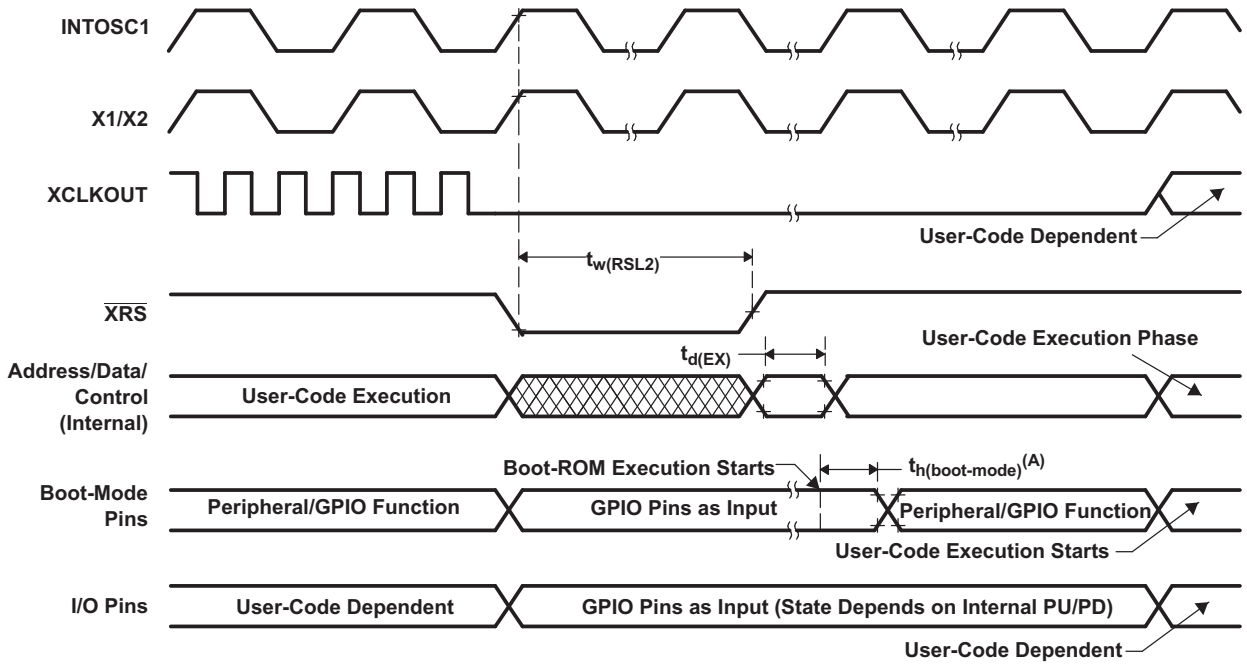
		MIN	MAX	UNIT
$t_{h(boot\text{-}mode)}$	Hold time for boot-mode pins	$1000t_{c(SCO)}$		cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low on warm reset	$32t_{c(OSCCLK)}$		cycles

Table 5-4. Reset ($\overline{XRS}$) Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, $\overline{XRS}$ driven by device		600		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles
$t_{d(EX)}$	Delay time, address/data valid after $\overline{XRS}$ high		$32t_{c(OSCCLK)}$		cycles
$t_{INTOSCST}$	Start up time, internal zero-pin oscillator		3		µs
t_{OSCST} (1)	On-chip crystal-oscillator start-up time	1	10		ms

(1) Dependent on crystal/resonator and board design.



A. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 5-7. Warm Reset

Figure 5-8 shows an example for the effect of writing into PLLCR register. In the first phase, PLLCR = 0x0004 and SYSCLKOUT = OSCCLK x 2. The PLLCR is then written with 0x0008. Right after the PLLCR register is written, the PLL lock-up phase begins. During this phase, SYSCLKOUT = OSCCLK/2. After the PLL lock-up is complete, SYSCLKOUT reflects the new operating frequency, OSCCLK x 4.

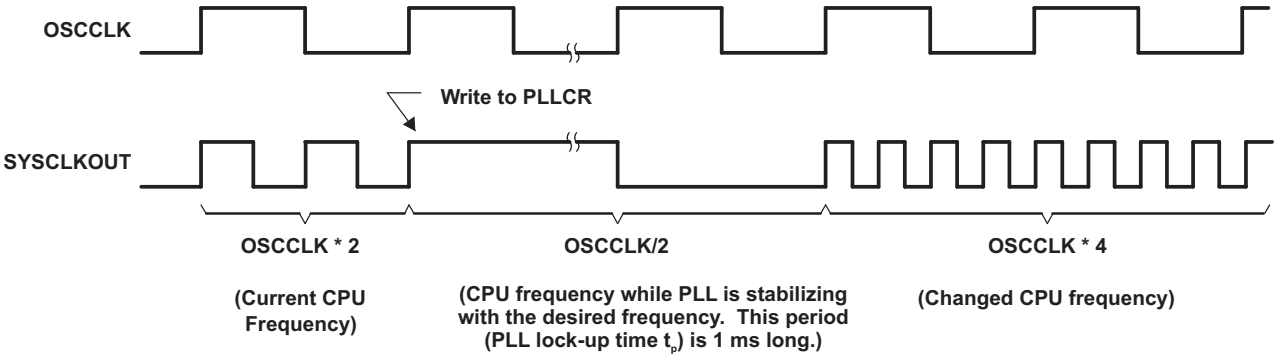


Figure 5-8. Example of Effect of Writing Into PLLCR Register

5.12 Clock Specifications

5.12.1 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the 2805x MCUs. Table 5-5 lists the cycle times of various clocks.

Table 5-5. 2805x Clock Table and Nomenclature (60-MHz Devices)

		MIN	NOM	MAX	UNIT
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	16.67		500	ns
	Frequency	2		60	MHz
LSPCLK (1)	$t_{c(LCO)}$, Cycle time	16.67	66.67 (2)		ns
	Frequency		15 (2)	60	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time	16.67			ns
	Frequency			60	MHz

(1) Lower LSPCLK will reduce device power consumption.
(2) This value is the default reset value if SYSCLKOUT = 60 MHz.

Table 5-6. Device Clocking Requirements/Characteristics

		MIN	NOM	MAX	UNIT
On-chip oscillator (X1/X2 pins) (Crystal/Resonator)	$t_{c(OSC)}$, Cycle time	50		200	ns
	Frequency	5		20	MHz
External oscillator/clock source (XCLKIN pin) — PLL Enabled	$t_{c(CI)}$, Cycle time (C8)	33.3		200	ns
	Frequency	5		30	MHz
External oscillator/clock source (XCLKIN pin) — PLL Disabled	$t_{c(CI)}$, Cycle time (C8)	33.33		250	ns
	Frequency	4		30	MHz
Limp mode SYSCLKOUT (with /2 enabled)	Frequency range		1 to 5		MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time (C1)	66.67		2000	ns
	Frequency	0.5		15	MHz
PLL lock time (1)	t_p			1	ms

(1) The PLLLOCKPRD register must be updated based on the number of OSCCLK cycles. If the zero-pin internal oscillators (10 MHz) are used as the clock source, then the PLLLOCKPRD register must be written with a value of 10,000 (minimum).

Table 5-7. Internal Zero-Pin Oscillator (INTOSC1, INTOSC2) Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
Internal zero-pin oscillator 1 (INTOSC1) at 30°C(1)(2)	Frequency		10.000		MHz
Internal zero-pin oscillator 2 (INTOSC2) at 30°C(1)(2)	Frequency		10.000		MHz
Accuracy using oscillator compensation(1)(2)			±1		%
Step size (coarse trim)			55		kHz
Step size (fine trim)			14		kHz
Temperature drift(3)			3.03	4.85	kHz/°C
Voltage (V_{DD}) drift(3)			175		Hz/mV

(1) In order to achieve better oscillator accuracy (10 MHz ± 1% or better) than shown, see the *Oscillator Compensation Guide Application Report* (SPRAB84). Refer to Figure 5-9 for TYP and MAX values.
(2) Frequency range ensured only when VREG is enabled, $\overline{\text{VREGENZ}}$ = V_{SS}.
(3) Output frequency of the internal oscillators follows the direction of both the temperature gradient and voltage (V_{DD}) gradient. For example:
- Increase in temperature will cause the output frequency to increase per the temperature coefficient.
- Decrease in voltage (V_{DD}) will cause the output frequency to decrease per the voltage coefficient.

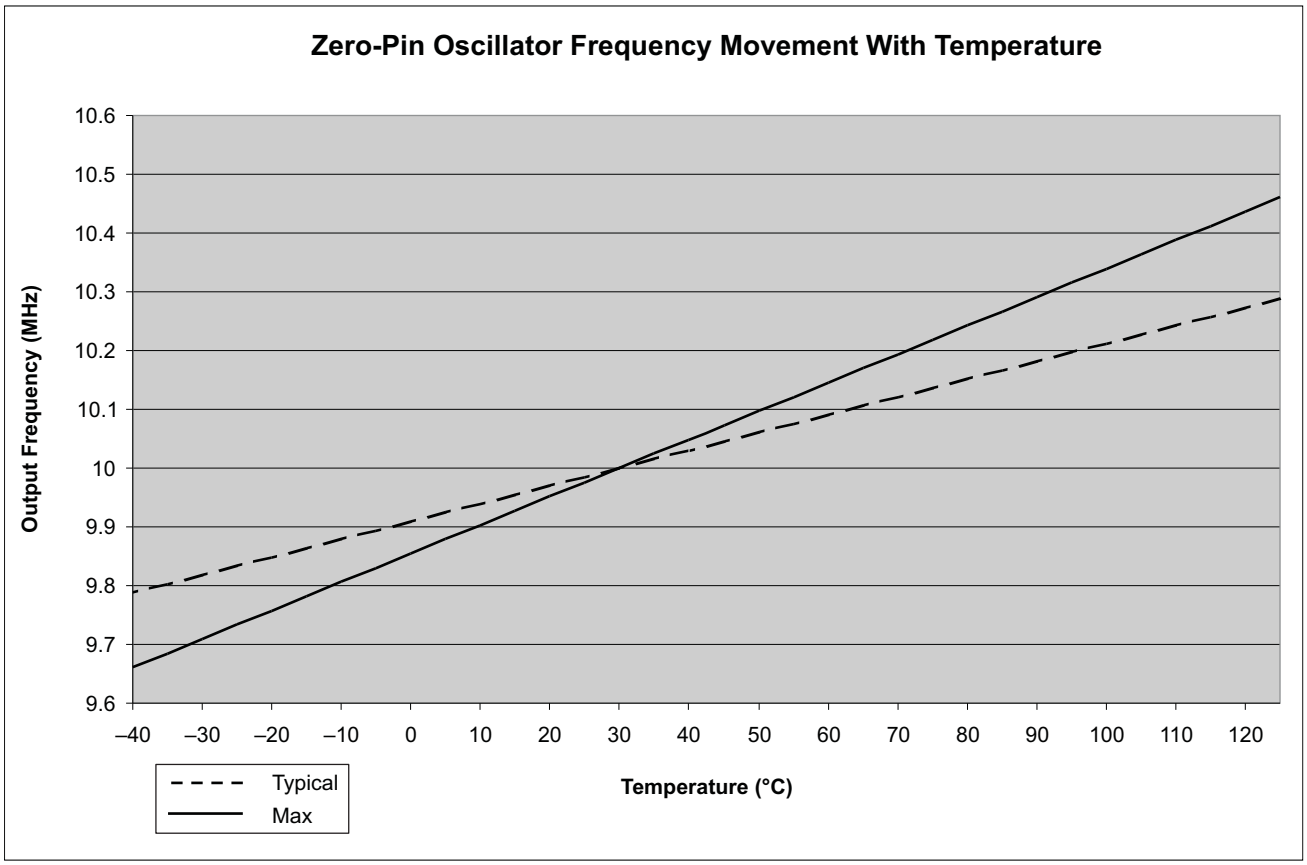


Figure 5-9. Zero-Pin Oscillator Frequency Movement With Temperature

5.12.2 Clock Requirements and Characteristics

Table 5-8. XCLKIN Timing Requirements - PLL Enabled

NO.			MIN	MAX	UNIT
C9	$t_{f(CI)}$	Fall time, XCLKIN		6	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN		6	ns
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	45	55	%

Table 5-9. XCLKIN Timing Requirements - PLL Disabled

NO.				MIN	MAX	UNIT
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 30 MHz		2	
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 30 MHz		2	
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$		45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$		45	55	%

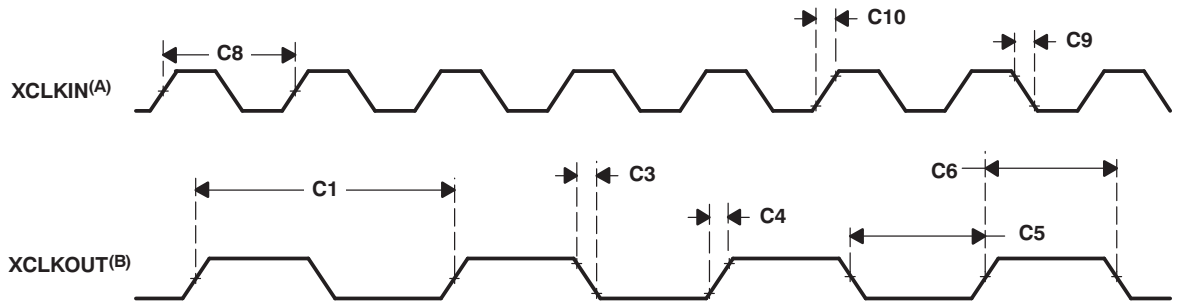
The possible configuration modes are shown in Table 6-21.

Table 5-10. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)(1) (2)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
C3	$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
C4	$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
C5	$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2	H + 2	ns
C6	$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2	H + 2	ns

(1) A load of 40 pF is assumed for these parameters.
(2) H = $0.5t_{c(XCO)}$



A. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown is intended to illustrate the timing parameters only and may differ based on actual configuration.
B. XCLKOUT configured to reflect SYSCLKOUT.

Figure 5-10. Clock Timing

5.13 Flash Timing

Table 5-11. Flash/OTP Endurance for T Temperature Material(1)

		ERASE/PROGRAM TEMPERATURE	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	0°C to 105°C (ambient)	20000	50000		cycles
N_{OTP}	OTP endurance for the array (write cycles)	0°C to 30°C (ambient)			1	write

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.

Table 5-12. Flash/OTP Endurance for S Temperature Material(1)

		ERASE/PROGRAM TEMPERATURE	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	0°C to 125°C (ambient)	20000	50000		cycles
N_{OTP}	OTP endurance for the array (write cycles)	0°C to 30°C (ambient)			1	write

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.

Table 5-13. Flash/OTP Endurance for Q Temperature Material(1)

		ERASE/PROGRAM TEMPERATURE	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	–40°C to 125°C (ambient)	20000	50000		cycles
N_{OTP}	OTP endurance for the array (write cycles)	–40°C to 30°C (ambient)			1	write

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.

Table 5-14. Flash Parameters at 60-MHz SYSCLKOUT

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Time	16-Bit Word			50		µs
	8K Sector			250		ms
	4K Sector			125		ms
Erase Time(1)	8K Sector			2		s
	4K Sector			2		s
I_{DDP} (2)	V_{DD} current consumption during Erase/Program cycle	VREG disabled		80		mA
I_{DDIOP} (2)	V_{DDIO} current consumption during Erase/Program cycle			60		
I_{DDIOP} (2)	V_{DDIO} current consumption during Erase/Program cycle	VREG enabled		120		mA

(1) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.
(2) Typical parameters as seen at room temperature including function call overhead, with all peripherals off. It is important to maintain a stable power supply during the entire flash programming process. It is conceivable that device current consumption during flash programming could be higher than normal operating conditions. The power supply used should ensure V_{MIN} on the supply rails at all times, as specified in the Recommended Operating Conditions of the data sheet. Any brown-out or interruption to power during erasing/programming could potentially corrupt the password locations and lock the device permanently. Powering a target board (during flash programming) through the USB port is not recommended, as the port may be unable to respond to the power demands placed during the programming process.

Table 5-15. Flash/OTP Access Timing

PARAMETER		MIN	MAX	UNIT
$t_{a(fp)}$	Paged Flash access time	40		ns
$t_{a(fr)}$	Random Flash access time	40		ns
$t_{a(OTP)}$	OTP access time	60		ns

Table 5-16. Flash Data Retention Duration

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{retention}$	Data retention duration	T_J = 55°C	15		years

Table 5-17. Minimum Required Flash/OTP Wait-States at Different Frequencies

SYSCLKOUT (MHz)	SYSCLKOUT (ns)	PAGE WAIT-STATE(1)	RANDOM WAIT-STATE(1)	OTP WAIT-STATE
60	16.67	2	2	3
55	18.18	2	2	3
50	20	1	1	2
45	22.22	1	1	2
40	25	1	1	2
35	28.57	1	1	2
30	33.33	1	1	1

(1) Page and random wait-state must be ≥ 1.

The equations to compute the Flash page wait-state and random wait-state in Table 5-17 are as follows:

$$\text{Flash Page Wait State} = \left[\left(\frac{t_{a(f \bullet p)}}{t_{c(SCO)}}\right) - 1\right] \text{ round up to the next highest integer}$$

$$\text{Flash Random Wait State} = \left[\left(\frac{t_{a(f \cdot r)}}{t_{c(SCO)}}\right) - 1\right] \text{ round up to the next highest integer, or 1, whichever is larger}$$

The equation to compute the OTP wait-state in Table 5-17 is as follows:

$$\text{OTP Wait State} = \left[\left(\frac{t_{a(OTP)}}{t_{c(SCO)}}\right) - 1\right] \text{ round up to the next highest integer, or 1, whichever is larger}$$

6 Detailed Description

6.1 Overview

6.1.1 CPU

The 2805x (C28x) family is a member of the TMS320C2000™ MCU platform. The C28x-based controllers have the same 32-bit fixed-point architecture as existing C28x MCUs. Each C28x-based controller, including the 2805x device, is a very efficient C/C++ engine, enabling users to develop not only their system control software in a high-level language, but also enabling development of math algorithms using C/C++. The device is as efficient at MCU math tasks as it is at system control tasks. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC 64-bit processing capabilities enable the controller to handle higher numerical resolution problems efficiently. Add to this feature the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The device has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the device to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

6.1.2 Control Law Accelerator

The C28x CLA is a single-precision (32-bit) floating-point unit that extends the capabilities of the C28x CPU by adding parallel processing. The CLA is an independent processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks, or routines, can be specified. Each task is started by software or a peripheral such as the ADC, ePWM, eCAP, eQEP, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers, ePWM, eCAP, eQEP, and the Comparator and DAC registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

6.1.3 Memory Bus (Harvard Bus Architecture)

As with many MCU-type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The memory bus architecture contains a program read bus, data read bus, and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed Harvard Bus, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)

6.1.4 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) MCU family of devices, the devices adopt a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor Memory Bus into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Three versions of the peripheral bus are supported. One version supports only 16-bit accesses (called peripheral frame 2). Another version supports both 16- and 32-bit accesses (called peripheral frame 1). The third version supports CLA access and both 16- and 32-bit accesses (called peripheral frame 3).

6.1.5 Real-Time JTAG and Analysis

The devices implement the standard IEEE 1149.1 JTAG (1) interface for in-circuit based debug. Additionally, the devices support real-time mode of operation allowing modification of the contents of memory, peripheral, and register locations while the processor is running and executing code and servicing interrupts. The user can also single step through non-time-critical code while enabling time-critical interrupts to be serviced without interference. The device implements the real-time mode in hardware within the CPU. This feature is unique to the 28x family of devices, and requires no software monitor. Additionally, special analysis hardware is provided that allows setting of hardware breakpoint or data/address watch-points and generating various user-selectable break events when a match occurs.

6.1.6 Flash

The F28055 and F28054 devices contain 64K x 16 of embedded flash memory, segregated into six 8K x 16 sectors and four 4K x 16 sectors. The F28053, F28052, and F28051 devices contain 32K x 16 of embedded flash memory, segregated into three 8K x 16 sectors and two 4K x 16 sectors. The F28050 device contains 16K x 16 of embedded flash memory, segregated into one 8K x 16 sector and two 4K x 16 sectors. The devices also contain a single 1K x 16 of OTP memory at address range 0x3D 7800 – 0x3D 7BFF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase or program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, the flash/OTP can be used to execute code or store data information.

NOTE

The Flash and OTP wait-states can be configured by the application. This feature allows applications running at slower frequencies to configure the flash to use fewer wait-states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait-state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait-state, and OTP wait-state registers, see the System Control and Interrupts chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5).

(1) IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

6.1.7 M0, M1 SARAMs

All devices contain these two blocks of single access memory, each 1K x 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer, which makes for easier programming in high-level languages.

6.1.8 L0 SARAM, and L1, L2, and L3 DPSARAMs

The device contains up to 8K x 16 of single-access RAM. To ascertain the exact size for a given device, see the device-specific memory map figures in Section 6.2. This block is mapped to both program and data space. Block L0 is 2K in size and is dual mapped to both program and data space. Blocks L1 and L2 are both 1K in size, and together with L0, are shared with the CLA which can ultilize these blocks for its data space. Block L3 is 4K in size and is shared with the CLA which can ultilize this block for its program space. DPSARAM refers to the dual-port configuration of these blocks.

6.1.9 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math-related algorithms.

Table 6-1. Boot Mode Selection

MODE	GPIO37/TDO	GPIO34/COMP2OUT/ COMP3OUT	$\overline{\text{TRST}}$	MODE
3	1	1	0	GetMode
2	1	0	0	Wait (see Section 6.1.10 for description)
1	0	1	0	SCI
0	0	0	0	Parallel IO
EMU	x	x	1	Emulation Boot

6.1.9.1 Emulation Boot

When the emulator is connected, the GPIO37/TDO pin cannot be used for boot mode selection. In this case, the boot ROM detects that an emulator is connected and uses the contents of two reserved SARAM locations in the PIE vector table to determine the boot mode. If the content of either location is invalid, then the *Wait* boot option is used. All boot mode options can be accessed in emulation boot.

6.1.9.2 GetMode

The default behavior of the *GetMode* option is to boot to flash. This behavior can be changed to another boot option by programming two locations in the OTP. If the content of either OTP location is invalid, then boot to flash is used. One of the following loaders can be specified: SCI, SPI, I^2C, CAN, or OTP.

6.1.9.3 Peripheral Pins Used by the Bootloader

Table 6-2 shows which GPIO pins are used by each peripheral bootloader. Refer to the GPIO mux table to see if these conflict with any of the peripherals you would like to use in your application.

Table 6-2. Peripheral Bootload Pins

BOOTLOADER	PERIPHERAL LOADER PINS
SCI	SCIRXDA (GPIO28) SCITXDA (GPIO29)
Parallel Boot	Data (GPIO31,30,5:0) 28x Control (GPIO26) Host Control (GPIO27)
SPI	SPISIMOA (GPIO16) SPISOMIA (GPIO17) SPICLKA (GPIO18) SPISTEA (GPIO19)
I^2C	SDAA (GPIO28) SCLA (GPIO29)
CAN	CANRXA (GPIO30) CANTXA (GPIO31)

6.1.10 Security

The TMS320F2805x device supports high levels of security with a dual-zone (Z1/Z2) feature to protect user's firmware from being reverse-engineered. The dual-zone feature enables the user to co-develop application software with a third-party or sub-contractor by preventing visibility into each other's software IP. The security features a 128-bit password (hardcoded for 16 wait states) for each zone, which the user programs into the USER-OTP. Each zone has its own dedicated USER-OTP, which needs to be programmed by the user with the required security settings, including the 128-bit password. Since OTP cannot be erased, in order to provide the user with the flexibility of changing security-related settings and passwords multiple times, a 32-bit link pointer is stored at the beginning of each USER-OTP. Considering the fact that user can only flip a '1' in USER-OTP to '0', the most significant bit position in the link pointer, programmed as 0, defines the USER-OTP region (zone-select) for each zone in which security-related settings and passwords are stored.

Table 6-3. Location of Zone-Select Block Based on Link Pointer

Zx LINK POINTER VALUE	ADDRESS OFFSET FOR ZONE-SELECT
32'bxx11111111111111111111111111111	0x10
32'bxx11111111111111111111111111110	0x20
32'bxx1111111111111111111111111110x	0x30
32'bxx1111111111111111111111111110xx	0x40
32'bxx1111111111111111111111111110xxx	0x50
32'bxx1111111111111111111111111110xxxx	0x60
32'bxx1111111111111111111111111110xxxxx	0x70
32'bxx1111111111111111111111111110xxxxxx	0x80
32'bxx1111111111111111111111111110xxxxxxx	0x90
32'bxx1111111111111111111111111110xxxxxxxx	0xa0
32'bxx1111111111111111111111111110xxxxxxxxx	0xb0
32'bxx1111111111111111111111111110xxxxxxxxxx	0xc0
32'bxx1111111111111111111111111110xxxxxxxxxxx	0xd0
32'bxx1111111111111111111111111110xxxxxxxxxxxx	0xe0
32'bxx1111111111111111111111111110xxxxxxxxxxxxx	0xf0

Table 6-3. Location of Zone-Select Block Based on Link Pointer (continued)

Zx LINK POINTER VALUE	ADDRESS OFFSET FOR ZONE-SELECT
32'bxx11111111111110xxxxxxxxxxxxxx	0x100
32'bxx11111111111110xxxxxxxxxxxxxx	0x110
32'bxx11111111111110xxxxxxxxxxxxxx	0x120
32'bxx11111111111110xxxxxxxxxxxxxx	0x130
32'bxx1111111111110xxxxxxxxxxxxxx	0x140
32'bxx1111111111110xxxxxxxxxxxxxx	0x150
32'bxx1111111110xxxxxxxxxxxxxxxxx	0x160
32'bxx1111111110xxxxxxxxxxxxxxxxx	0x170
32'bxx1111111110xxxxxxxxxxxxxxxxx	0x180
32'bxx1111110xxxxxxxxxxxxxxxxxxx	0x190
32'bxx1111110xxxxxxxxxxxxxxxxxxx	0x1a0
32'bxx111110xxxxxxxxxxxxxxxxxxxx	0x1b0
32'bxx111110xxxxxxxxxxxxxxxxxxxx	0x1c0
32'bxx11110xxxxxxxxxxxxxxxxxxxxx	0x1d0
32'bxx11110xxxxxxxxxxxxxxxxxxxxx	0x1e0
32'bxx1110xxxxxxxxxxxxxxxxxxxxxx	0x1f0

Table 6-4. Zone-Select Block Organization in USER-OTP

16-BIT ADDRESS OFFSET (WITH RESPECT TO OFFSET OF ZONE-SELECT)	CONTENT
0x0	Zx-EXEONLYRAM
0x1	
0x2	Zx-EXEONLYSECT
0x3	
0x4	Zx-GRABRAM
0x5	
0x6	Zx-GRABSECT
0x7	
0x8	Zx-CSMPSWD0
0x9	
0xa	Zx-CSMPSWD1
0xb	
0xc	Zx-CSMPSWD2
0xd	
0xe	Zx-CSMPSWD3
0xf	

The Dual Code Security Module (DCSM) is used to protect the Flash/OTP/Lx SARAM blocks/CLA/Secure ROM content. Individual flash sectors and SARAM blocks can be attached to any of the secure zone at start-up time. Secure ROM and the CLA are always attached to Z1. Resources attached to (owned by) one zone do not have any access to code running in the other zone when it is secured. Individual flash sectors, as well as SARAM blocks, can be further protected by enabling the EXEONLY protection. EXEONLY flash sectors or SARAM blocks do not have READ/WRITE access. Only code execution is allowed from such memory blocks.

The security feature prevents unauthorized users from examining memory contents via the JTAG port, executing code from external memory, or trying to boot load an undesirable software that would export the secure memory contents. To enable access to the secure blocks of a particular zone, the user must write a 128-bit value in the zone's CSMKEY registers that matches the values stored in the password locations in USER-OTP. If the 128 bits of the password locations in USER-OTP of a particular zone are all ones (un-programmed), then the security for that zone gets UNLOCKED as soon as a dummy read is done to the password locations in USER-OTP (the value in the CSMKEY register becomes "Don't care" in this case).

In addition to the DCSM, the Emulation Code Security Logic (ECSL) has been implemented for each zone to prevent unauthorized users from stepping through secure code. A halt inside secure code will trip the ECSL and break the emulation connection. To allow emulation of secure code while maintaining DCSM protection against secure memory reads, the user must write the lower 64 bits of the USER-OTP password into the zone's CSMKEY register to disable the ECSL. Note that dummy reads of all 128 bits of the password for that particular zone in USER-OTP must still be performed. If the lower 64 bits of the password locations of a particular zone are all zeros, then the ECSL for that zone gets disabled as soon as a dummy read is done to the password locations in USER-OTP (the value in the CSMKEY register becomes "Don't care" in this case).

When initially debugging a device with the password locations in OTP (that is, secured), the CPU will start running and may execute an instruction that performs an access to ECSL-protected area. If the CPU execution is halted when the program counter belongs to the secure code region, the ECSL will trip and cause the emulator connection to be cut. The solution is to use the *Wait* boot option. The *Wait* boot option will sit in a loop around a software breakpoint to allow an emulator to be connected without tripping security. The user can then exit this mode once the emulator is connected by using one of the emulation boot options as described in the Boot ROM chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5). 2805x devices do not support hardware wait-in-reset mode.

To prevent reverse-engineering of the code in secure zone, unauthorized users are prevented from looking at the CPU registers in the CCS Expressions Window. The values in the Expressions Window for all of these registers, except for PC and some status bits, display false values when code is running from a secure zone. This feature gets disabled if the zone is unlocked.

NOTE

- The USER-OTP contains security-related settings for their respective zone. Execution is not allowed from the USER-OTP; therefore, the user should not keep any code/data in this region.
- The 128-bit password must not be programmed to zeros. Doing so would permanently lock the device.
- The user must try not to write into the CPU registers through the debugger watch window when code is running/halted from/inside secure zone. This may corrupt the execution of the actual program.

Disclaimer

Dual Code Security Module Disclaimer

THE DUAL CODE SECURITY MODULE (DCSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE DCSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE DCSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE DCSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

6.1.11 Peripheral Interrupt Expansion Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F2805x devices, 54 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. Eight CPU clock cycles are needed to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled or disabled within the PIE block.

6.1.12 External Interrupts (XINT1–XINT3)

The devices support three masked external interrupts (XINT1–XINT3). Each of the interrupts can be selected for negative, positive, or both negative and positive edge triggering and can also be enabled or disabled. These interrupts also contain a 16-bit free running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt. There are no dedicated pins for the external interrupts. XINT1, XINT2, and XINT3 interrupts can accept inputs from GPIO0–GPIO31 pins.

6.1.13 Internal Zero-Pin Oscillators, Oscillator, and PLL

The device can be clocked by either of the two internal zero-pin oscillators, an external oscillator, or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 12 input-clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to Section 5.12 for timing details. The PLL block can be set in bypass mode.

6.1.14 Watchdog

Each device contains two watchdogs: CPU-Watchdog that monitors the core and NMI-Watchdog that is a missing clock-detect circuit. The user software must regularly reset the CPU-watchdog counter within a certain time frame; otherwise, the CPU-watchdog generates a reset to the processor. The CPU-watchdog can be disabled if necessary. The NMI-Watchdog engages only in case of a clock failure and can either generate an interrupt or a device reset.

6.1.15 Peripheral Clocking

The clocks to each individual peripheral can be enabled or disabled to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except I^2C) can be scaled relative to the CPU clock.

6.1.16 Low-power Modes

The devices are full-static CMOS devices. Three low-power modes are provided:

- IDLE: Place CPU in low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that need to function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.
- STANDBY: Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event
- HALT: This mode basically shuts down the device and places the device in the lowest possible power consumption mode. If the internal zero-pin oscillators are used as the clock source, the HALT mode turns them off, by default. To keep these oscillators from shutting down, the INTOSCnHALTI bits in CLKCTL register may be used. The zero-pin oscillators may thus be used to clock the CPU-watchdog in this mode. If the on-chip crystal oscillator is used as the clock source, the crystal oscillator is shut down in this mode. A reset or an external signal (through a GPIO pin) or the CPU-watchdog can wake the device from this mode.

The CPU clock (OSCCLK) and WDCLK should be from the same clock source before attempting to put the device into HALT or STANDBY.

6.1.17 Peripheral Frames 0, 1, 2, 3 (PFn)

The device segregates peripherals into four sections. The mapping of peripherals is as follows:

PF0:	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Waitstate Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	DCSM:	Dual Zone Security Module Registers
	ADC:	ADC Result Registers
	CLA	CLA Registers and Message RAMs
PF1:	GPIO:	GPIO MUX Configuration and Control Registers
	eCAN:	eCAN Configuration and Control Registers
	eCAP:	eCAP Module and Registers
	eQEP:	eQEP Module and Registers
PF2:	SYS:	System Control Registers
	SCI:	SCI Control and RX/TX Registers
	SPI:	SPI Control and RX/TX Registers
	ADC:	ADC Status, Control, and Configuration Registers
	I^2C:	I^2C Module and Registers
	XINT:	External Interrupt Registers
PF3:	ePWM:	ePWM Module and Registers
	AFE:	Comparator Modules, Digital Filters, and PGA Control Registers
	eCAP:	eCAP Module and Registers
	eQEP:	eQEP Module and Registers
	ADC:	ADC Status, Control, and Configuration Registers
	ADC:	ADC Result Registers
	DAC:	DAC Control Registers

6.1.18 General-Purpose Input/Output Multiplexer

Most of the peripheral signals are multiplexed with GPIO signals. This muxing enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles. This selection is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low-power modes.

6.1.19 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, the counter is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and can be connected to INT13 of the CPU. CPU-Timer 2 is reserved for DSP/BIOS™. CPU-Timer 2 is connected to INT14 of the CPU. If DSP/BIOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLKOUT (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTSOC2)
- External clock source

6.1.20 Control Peripherals

The devices support the following peripherals that are used for embedded control and communication:

ePWM:	The ePWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. The type 1 module found on 2805x devices also supports increased dead-band resolution, enhanced SOC and interrupt generation, and advanced triggering including trip functions based on comparator outputs.
eCAP:	The eCAP peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes. This peripheral can also be configured to generate an auxiliary PWM signal.
eQEP:	The eQEP peripheral uses a 32-bit position counter, supports low-speed measurement using capture unit and high-speed measurement using a 32-bit unit timer. This peripheral has a watchdog timer to detect motor stall and input error detection logic to identify simultaneous edge transition in QEP signals.
ADC:	The ADC block is a 12-bit converter. The ADC has up to 16 single-ended channels pinned out, depending on the device. The ADC also contains two sample-and-hold units for simultaneous sampling. Some ADC channels also have PGAs, which can amplify the input signal by 3, 6, or 11.
Comparator and Digital Filter Subsystems:	Each comparator block consists of one analog comparator along with an internal 6-bit reference for supplying one input of the comparator. The comparator output signal filtering is achieved using the Digital Filter present on each input line and qualifies the output of the COMP/DAC subsystem. The filtered or unfiltered output of the COMP/DAC subsystem can be configured to be an input to the Digital Compare submodule of the ePWM peripheral. There is also a configurable option to bring the output of the COMP/DAC subsystem onto the GPIO's.

6.1.21 Serial Port Peripherals

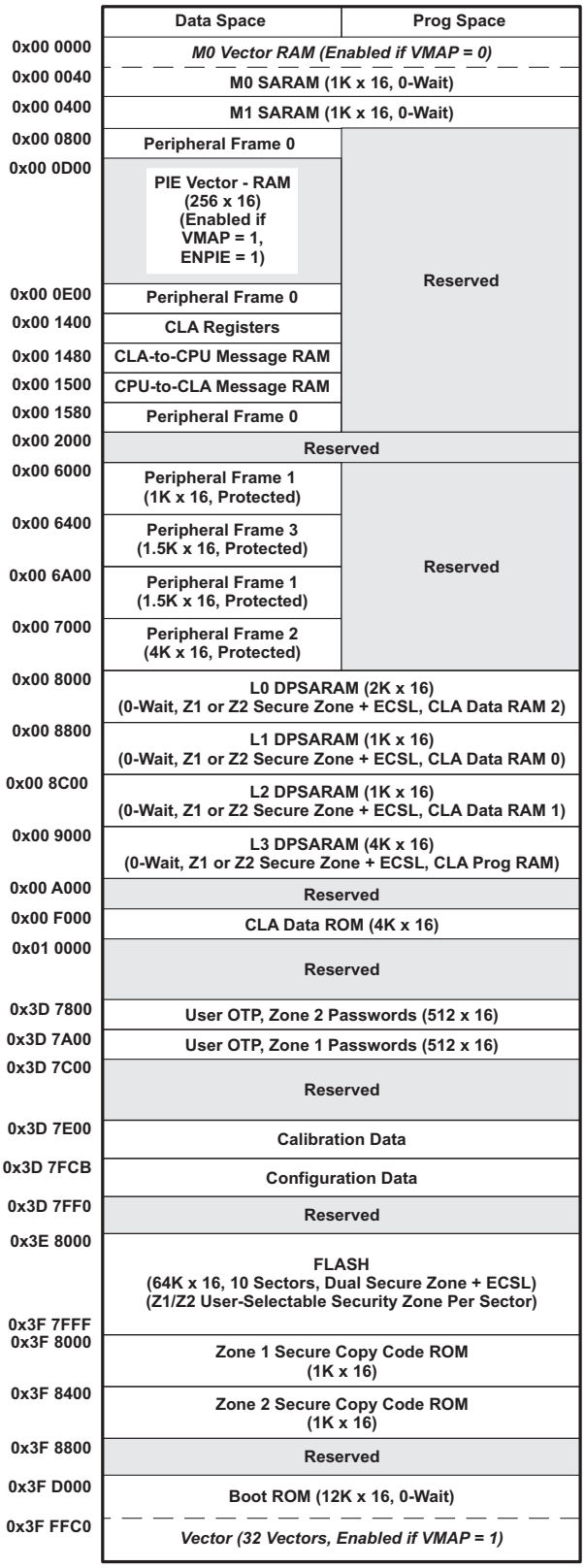
The devices support the following serial communication peripherals:

- SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. The SPI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.
- SCI: The SCI is a two-wire asynchronous serial port, commonly known as UART. The SCI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.
- I^2C: The I^2C module provides an interface between an MCU and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit data to and from the MCU through the I^2C module. The I^2C contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.
- eCAN: The eCAN is the enhanced version of the CAN peripheral. The eCAN supports 32 mailboxes, time stamping of messages, and is CAN 2.0B-compliant.

6.2 Memory Maps

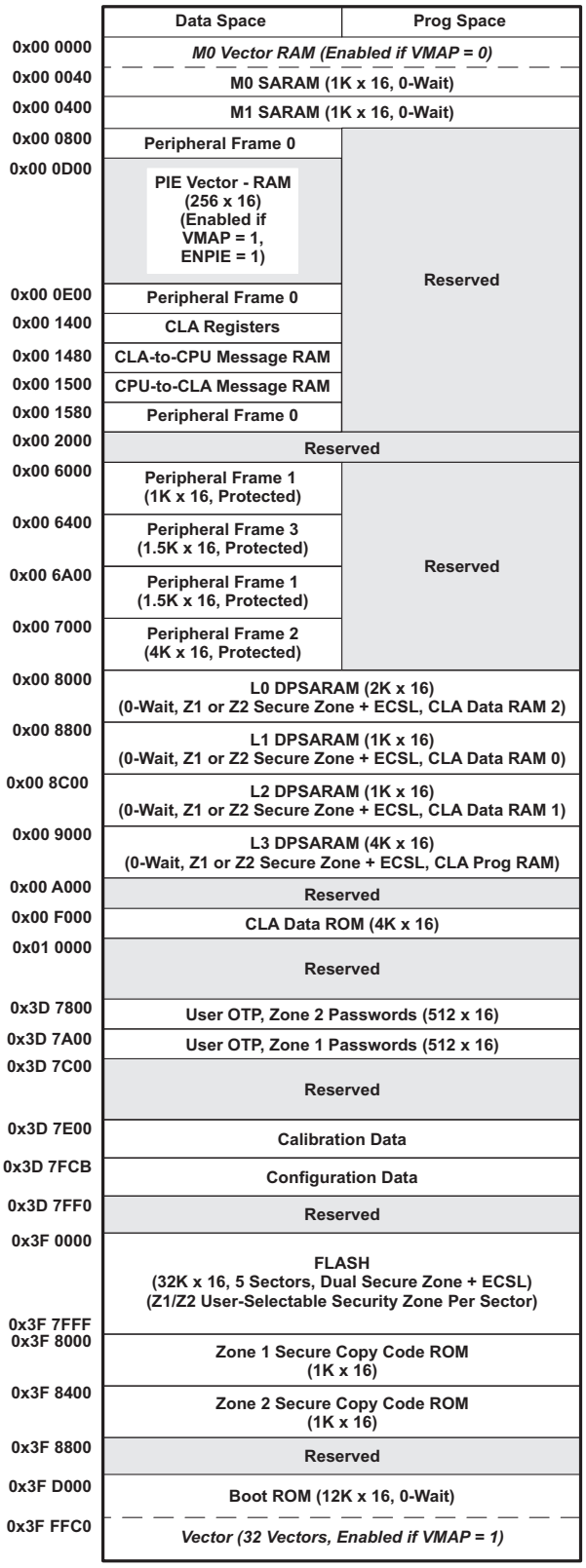
In Figure 6-1, Figure 6-2, Figure 6-3, and Figure 6-4, the following apply:

- Memory blocks are not to scale.
- Peripheral Frame 0, Peripheral Frame 1, Peripheral Frame 2, and Peripheral Frame 3 memory maps are restricted to data memory only. A user program cannot access these memory maps in program space.
- *Protected* means the order of Write-followed-by-Read operations is preserved rather than the pipeline order.
- Certain memory ranges are EALLOW protected against spurious writes after configuration.



A. CLA-specific registers and RAM apply to the 28055 device only.

Figure 6-1. 28055 and 28054 Memory Map



A. CLA-specific registers and RAM apply to the 28053 device only.

Figure 6-2. 28053 and 28052 Memory Map

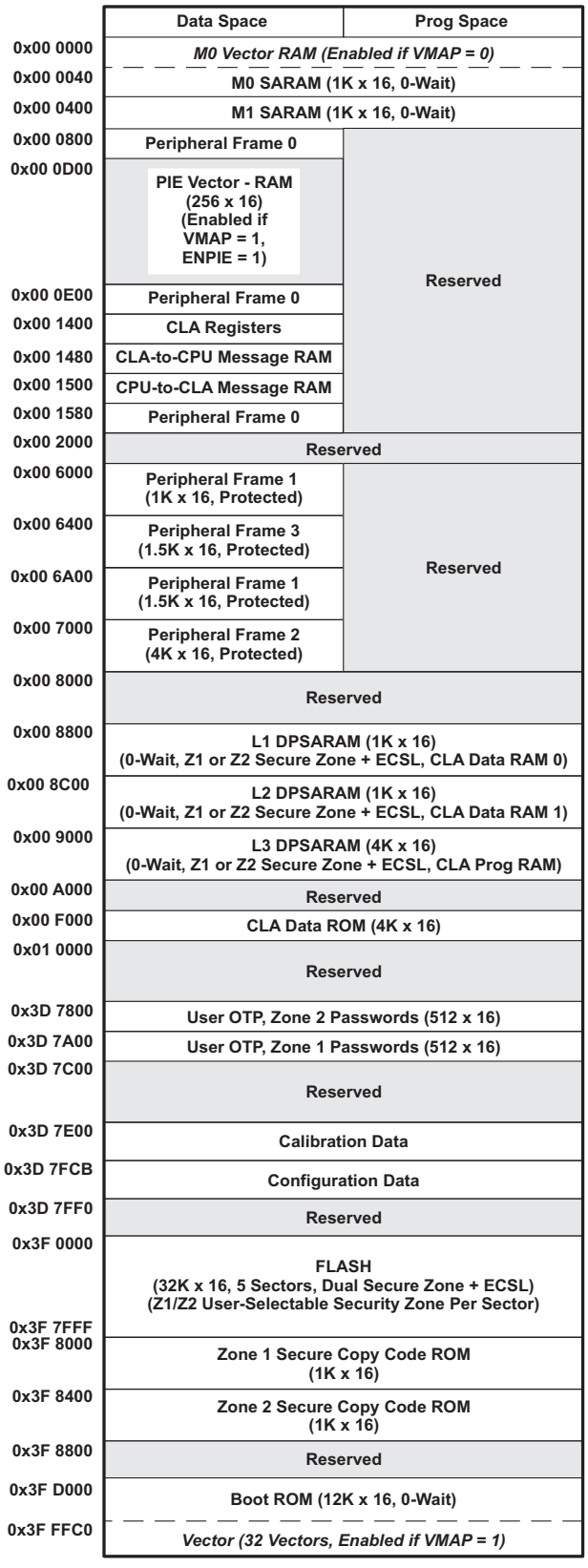


Figure 6-3. 28051 Memory Map

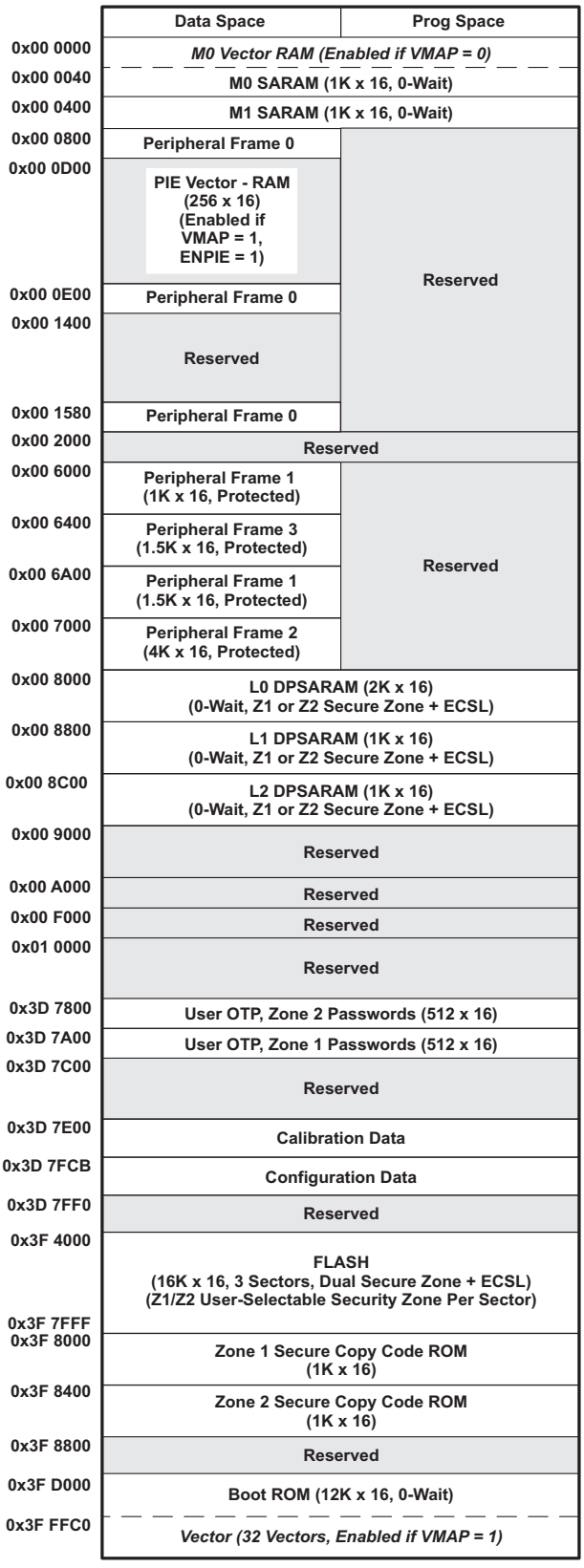


Figure 6-4. 28050 Memory Map

Table 6-5. Addresses of Flash Sectors in F28055 and F28054

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3E 8000 – 0x3E 8FFF	Sector J (4K x 16)
0x3E 9000 – 0x3E 9FFF	Sector I (4K x 16)
0x3E A000 – 0x3E BFFF	Sector H (8K x 16)
0x3E C000 – 0x3E DFFF	Sector G (8K x 16)
0x3E E000 – 0x3E FFFF	Sector F (8K x 16)
0x3F 0000 – 0x3F 1FFF	Sector E (8K x 16)
0x3F 2000 – 0x3F 3FFF	Sector D (8K x 16)
0x3F 4000 – 0x3F 5FFF	Sector C (8K x 16)
0x3F 6000 – 0x3F 6FFF	Sector B (4K x 16)
0x3F 7000 – 0x3F 7FFF	Sector A (4K x 16)

Table 6-6. Addresses of Flash Sectors in F28053, F28052, and F28051

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3F 0000 – 0x3F 1FFF	Sector E (8K x 16)
0x3F 2000 – 0x3F 3FFF	Sector D (8K x 16)
0x3F 4000 – 0x3F 5FFF	Sector C (8K x 16)
0x3F 6000 – 0x3F 6FFF	Sector B (4K x 16)
0x3F 7000 – 0x3F 7FFF	Sector A (4K x 16)

Table 6-7. Addresses of Flash Sectors in F28050

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3F 4000 – 0x3F 5FFF	Sector C (8K x 16)
0x3F 6000 – 0x3F 6FFF	Sector B (4K x 16)
0x3F 7000 – 0x3F 7FFF	Sector A (4K x 16)

Peripheral Frame 1, Peripheral Frame 2, and Peripheral Frame 3 are grouped together to enable these blocks to be write/read peripheral block protected. The protected mode makes sure that all accesses to these blocks happen as written. Because of the pipeline, a write immediately followed by a read to different memory locations will appear in reverse order on the memory bus of the CPU. This action can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The CPU supports a block protection mode where a region of memory can be protected so that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable, and by default, it protects the selected zones.

The wait-states for the various spaces in the memory map area are listed in Table 6-8.

Table 6-8. Wait-States

AREA	WAIT-STATES (CPU)	COMMENTS
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	0-wait	
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Cycles can be extended by peripheral generated ready. Back-to-back write operations to Peripheral Frame 1 registers will incur a 1-cycle stall (1-cycle delay).
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed. Cycles cannot be extended by the peripheral.
Peripheral Frame 3	0-wait (writes) 2-wait (reads)	Assumes no conflict between CPU and CLA. Cycles can be extended by peripheral-generated ready.
L0 SARAM	0-wait data and program	Assumes no CPU conflicts
L1 SARAM	0-wait data and program	Assumes no CPU conflicts
L2 SARAM	0-wait data and program	Assumes no CPU conflicts
L3 SARAM	0-wait data and program	Assumes no CPU conflicts
OTP	Programmable 1-wait minimum	Programmed via the Flash registers. 1-wait is minimum number of wait states allowed.
FLASH	Programmable 0-wait Paged min 1-wait Random min Random ≥ Paged	Programmed via the Flash registers.
FLASH Password	16-wait fixed	Wait states of password locations are fixed.
Boot-ROM	0-wait	
Secure ROM	0-wait	

6.3 Register Map

The devices contain four peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 6-9.

Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 6-10.

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 6-11.

Peripheral Frame 3: These are peripherals that are mapped to CLA in addition to their respective Peripheral Frame. See Table 6-12.

Table 6-9. Peripheral Frame 0 Registers(1)

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED(2)
Device Emulation Registers	0x00 0880 – 0x00 0984	261	Yes
System Power Control Registers	0x00 0985 – 0x00 0987	3	Yes
FLASH Registers(3)	0x00 0A80 – 0x00 0ADF	96	Yes
ADC registers (0 wait read only)	0x00 0B00 – 0x00 0B0F	16	No
DCSM Zone 1 Registers	0x00 0B80 – 0x00 0BBF	64	Yes
DCSM Zone 2 Registers	0x00 0BC0 – 0x00 0BEF	48	Yes
CPU-TIMER0, CPU-TIMER1, CPU-TIMER2 Registers	0x00 0C00 – 0x00 0C3F	64	No
PIE Registers	0x00 0CE0 – 0x00 0CFF	32	No
PIE Vector Table	0x00 0D00 – 0x00 0DFF	256	No
CLA Registers	0x00 1400 – 0x00 147F	128	Yes
CLA to CPU Message RAM (CPU writes ignored)	0x00 1480 – 0x00 14FF	128	NA
CPU to CLA Message RAM (CLA writes ignored)	0x00 1500 – 0x00 157F	128	NA

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
(3) The Flash Registers are also protected by the Dual Code Security Module.

Table 6-10. Peripheral Frame 1 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
eCAN-A Registers	0x00 6000 – 0x00 61FF	512	(1)
eCAP1 Registers	0x00 6A00 – 0x00 6A1F	32	No
eQEP1 Registers	0x00 6B00 – 0x00 6B3F	64	(1)
GPIO Registers	0x00 6F80 – 0x00 6FFF	128	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

Table 6-11. Peripheral Frame 2 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
System Control Registers	0x00 7010 – 0x00 702F	32	Yes
SPI-A Registers	0x00 7040 – 0x00 704F	16	No
SCI-A Registers	0x00 7050 – 0x00 705F	16	No
NMI Watchdog Interrupt Registers	0x00 7060 – 0x00 706F	16	Yes
External Interrupt Registers	0x00 7070 – 0x00 707F	16	Yes
ADC Registers	0x00 7100 – 0x00 717F	128	(1)
I2C-A Registers	0x00 7900 – 0x00 793F	64	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

Table 6-12. Peripheral Frame 3 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
ADC registers (0 wait read only)	0x00 0B00 – 0x00 0B0F	16	No
DAC Control Registers	0x00 6400 – 0x00 640F	16	Yes
DAC, PGA, Comparator, and Filter Enable Registers	0x00 6410 – 0x00 641F	16	Yes
SWITCH Registers	0x00 6420 – 0x00 642F	16	Yes
Digital Filter and Comparator Control Registers	0x00 6430 – 0x00 647F	80	Yes
LOCK Registers	0x00 64F0 – 0x00 64FF	16	Yes
ePWM1 registers	0x00 6800 – 0x00 683F	64	(1)
ePWM2 registers	0x00 6840 – 0x00 687F	64	(1)
ePWM3 registers	0x00 6880 – 0x00 68BF	64	(1)
ePWM4 registers	0x00 68C0 – 0x00 68FF	64	(1)
ePWM5 registers	0x00 6900 – 0x00 693F	64	(1)
ePWM6 registers	0x00 6940 – 0x00 697F	64	(1)
ePWM7 registers	0x00 6980 – 0x00 69BF	64	(1)
eCAP1 Registers	0x00 6A00 – 0x00 6A1F	32	No
eQEP1 Registers	0x00 6B00 – 0x00 6B3F	64	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

6.4 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 6-13.

Table 6-13. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION			EALLOW PROTECTED
DEVICECNF	0x0880 – 0x0881	2	Device Configuration Register			Yes
PARTID	0x0882	1	PARTID Register	TMS320F28055	0x0105	No
				TMS320F28054	0x0104	
				TMS320F28054M	0x0184	
				TMS320F28054F	0x0144	
				TMS320F28053	0x0103	
				TMS320F28052	0x0102	
				TMS320F28052M	0x0182	
				TMS320F28052F	0x0142	
				TMS320F28051	0x0101	
				TMS320F28050	0x0100	
REVID(1)	0x0883	1	Revision ID Register	0x0000 - Silicon Rev. 0 - TMX 0x0000 - Silicon Rev. A - TMS		No
DC1	0x0886 – 0x0887	2	Device Capability Register 1. The Device Capability Register is predefined by the part and can be used to verify features. If any bit is “zero” in this register, the module is not present. See Table 6-14.			Yes
DC2	0x0888 – 0x0889	2	Device Capability Register 2. The Device Capability Register is predefined by the part and can be used to verify features. If any bit is “zero” in this register, the module is not present. See Table 6-15.			Yes
DC3	0x088A – 0x088B	2	Device Capability Register 3. The Device Capability Register is predefined by the part and can be used to verify features. If any bit is “zero” in this register, the module is not present. See Table 6-16.			Yes

(1) Boot-ROM contents changed between Rev. 0 silicon and Rev. A silicon. For more details, see the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5).

Table 6-14. Device Capability Register 1 (DC1) Field Descriptions(1)

BIT	FIELD	TYPE	DESCRIPTION
31–30	RSVD	R = 0	Reserved
29–22	PARTNO	R	These 8 bits set the PARTNO field value in the PARTID register for the device. They are readable in the PARTID[7:0] register bits.
21–14	RSVD	R = 0	Reserved
13	CLA	R	CLA is present when this bit is set.
12–7	RSVD	R = 0	Reserved
6	L3	R	L3 is present when this bit is set.
5	L2	R	L2 is present when this bit is set.
4	L1	R	L1 is present when this bit is set.
3	L0	R	L0 is present when this bit is set.
2	RSVD	R = 0	Reserved
1–0	RSVD	R = 0	Reserved

(1) All reserved bits should not be written to but if any use case demands that they must be written to, then software must write the same value that is read back from the reserved bits. These bits are reserved for future enhancements.

Table 6-15. Device Capability Register 2 (DC2) Field Descriptions(1)

BIT	FIELD	TYPE	DESCRIPTION
31–28	RSVD	R = 0	Reserved
27	eCAN-A	R	eCAN-A is present when this bit is set.
26–17	RSVD	R = 0	Reserved
16	EQEP-1	R	eQEP-1 is present when this bit is set.
15–13	RSVD	R = 0	Reserved
12	ECAP-1	R	eCAP-1 is present when this bit is set.
11–9	RSVD	R = 0	Reserved
8	I2C-A	R	I2C-A is present when this bit is set.
7–5	RSVD	R = 0	Reserved
4	SPI-A	R	SPI-A is present when this bit is set.
3	RSVD	R = 0	Reserved
2	SCI-C	R	SCI-C is present when this bit is set.
1	SCI-B	R	SCI-B is present when this bit is set.
0	SCI-A	R	SCI-A is present when this bit is set.

(1) All reserved bits should not be written to but if any use case demands that they must be written to, then software must write the same value that is read back from the reserved bits. These bits are reserved for future enhancements.

Table 6-16. Device Capability Register 3 (DC3) Field Descriptions(1)

BIT	FIELD	TYPE	DESCRIPTION
31–20	RSVD	R = 0	Reserved
19	CTRIPFIL7	R	CTRIPFIL7(B7) is present when this bit is set.
18	CTRIPFIL6	R	CTRIPFIL6(B6) is present when this bit is set.
17	CTRIPFIL5	R	CTRIPFIL5(B4) is present when this bit is set.
16	CTRIPFIL4	R	CTRIPFIL4(A6) is present when this bit is set.
15	CTRIPFIL3	R	CTRIPFIL3(B1) is present when this bit is set.
14	CTRIPFIL2	R	CTRIPFIL2(A3) is present when this bit is set.
13	CTRIPFIL1	R	CTRIPFIL1(A1) is present when this bit is set.
12–8	RSVD	R = 0	Reserved
7	RSVD	R = 0	Reserved
6	ePWM7	R	ePWM7 is present when this bit is set.
5	ePWM6	R	ePWM6 is present when this bit is set.
4	ePWM5	R	ePWM5 is present when this bit is set.
3	ePWM4	R	ePWM4 is present when this bit is set.
2	ePWM3	R	ePWM3 is present when this bit is set.
1	ePWM2	R	ePWM2 is present when this bit is set.
0	ePWM1	R	ePWM1 is present when this bit is set.

(1) All reserved bits should not be written to but if any use case demands that they must be written to, then software must write the same value that is read back from the reserved bits. These bits are reserved for future enhancements.

6.5 VREG, BOR, POR

Although the core and I/O circuitry operate on two different voltages, these devices have an on-chip voltage regulator (VREG) to generate the V_{DD} voltage from the V_{DDIO} supply. This feature eliminates the cost and space of a second external regulator on an application board. Additionally, internal power-on reset (POR) and brown-out reset (BOR) circuits monitor both the V_{DD} and V_{DDIO} rails during power-up and run mode.

6.5.1 On-chip VREG

A linear regulator generates the core voltage (V_{DD}) from the V_{DDIO} supply. Therefore, although capacitors are required on each V_{DD} pin to stabilize the generated voltage, power need not be supplied to these pins to operate the device. Conversely, the VREG can be disabled, should power or redundancy be the primary concern of the application.

6.5.1.1 Using the On-chip VREG

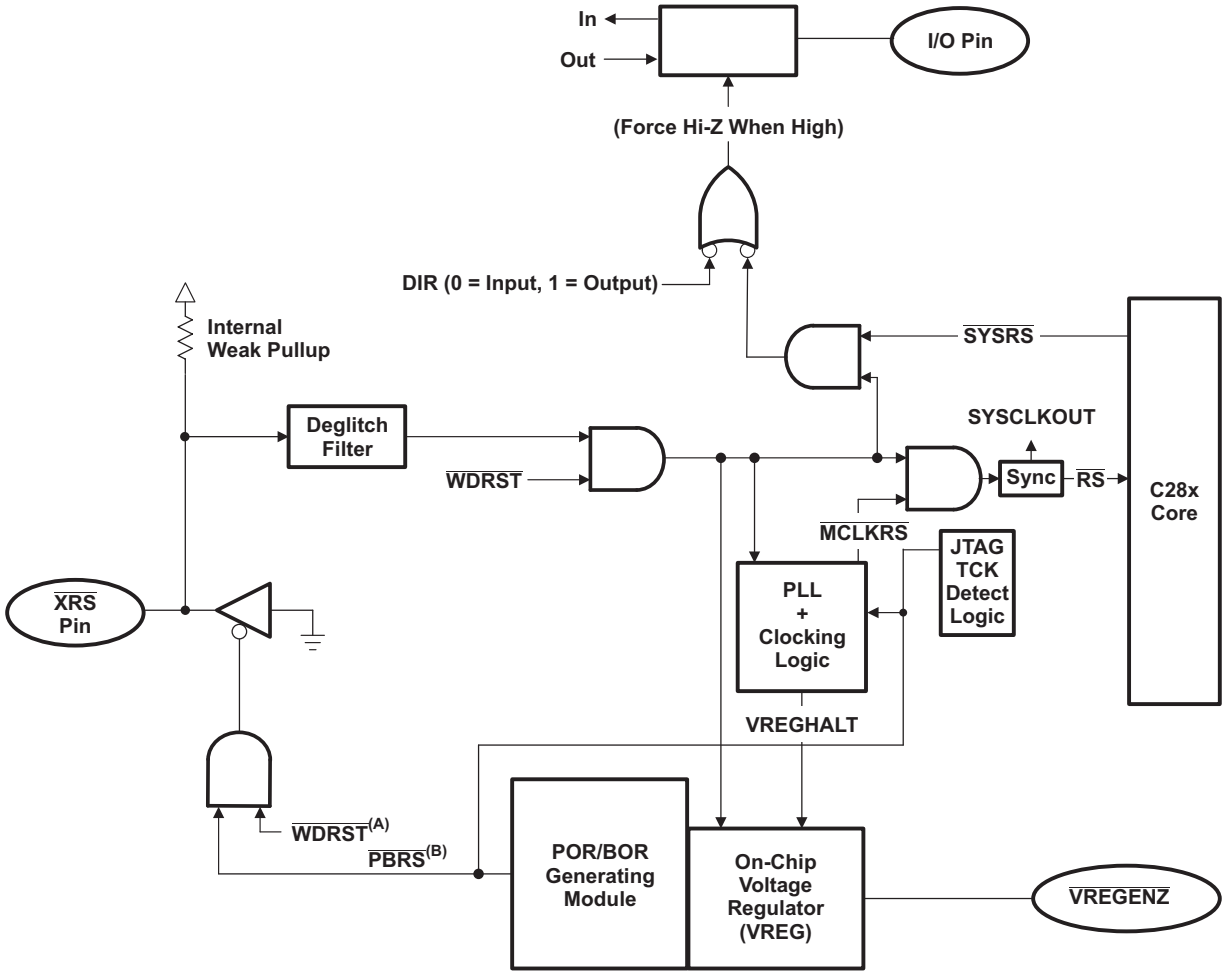
To utilize the on-chip VREG, the $\overline{\text{VREGENZ}}$ pin should be tied low and the appropriate recommended operating voltage should be supplied to the V_{DDIO} and V_{DDA} pins. In this case, the V_{DD} voltage needed by the core logic will be generated by the VREG. Each V_{DD} pin requires on the order of 1.2 µF (minimum) capacitance for proper regulation of the VREG. These capacitors should be located as close as possible to the V_{DD} pins.

6.5.1.2 Disabling the On-chip VREG

To conserve power, it is also possible to disable the on-chip VREG and supply the core logic voltage to the V_{DD} pins with a more efficient external regulator. To enable this option, the $\overline{\text{VREGENZ}}$ pin must be tied high.

6.5.2 On-chip Power-On Reset and Brown-Out Reset Circuit

The purpose of the POR is to create a clean reset throughout the device during the entire power-up procedure. The trip point is a looser, lower trip point than the BOR, which watches for dips in the V_{DD} or V_{DDIO} rail during device operation. The POR function is present on both V_{DD} and V_{DDIO} rails at all times. After initial device power-up, the BOR function is present on V_{DDIO} at all times, and on V_{DD} when the internal VREG is enabled ($\overline{\text{VREGENZ}}$ pin is tied low). Both functions tie the $\overline{\text{XRS}}$ pin low when one of the voltages is below their respective trip point. Additionally, when the internal voltage regulator is enabled, an over-voltage protection circuit will tie $\overline{\text{XRS}}$ low if the V_{DD} rail rises above its trip point. See Section 5.4 for the various trip points as well as the delay time for the device to release the $\overline{\text{XRS}}$ pin after the under-voltage or over-voltage condition is removed. Figure 6-5 shows the VREG, POR, and BOR. To disable both the V_{DD} and V_{DDIO} BOR functions, a bit is provided in the BORCFG register. See the System Control and Interrupts chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5) for details.



A. $\overline{\text{WDRST}}$ is the reset signal from the CPU-watchdog.
B. $\overline{\text{PBRS}}$ is the reset signal from the POR/BOR module.

Figure 6-5. VREG + POR + BOR + Reset Signal Connectivity

6.6 System Control

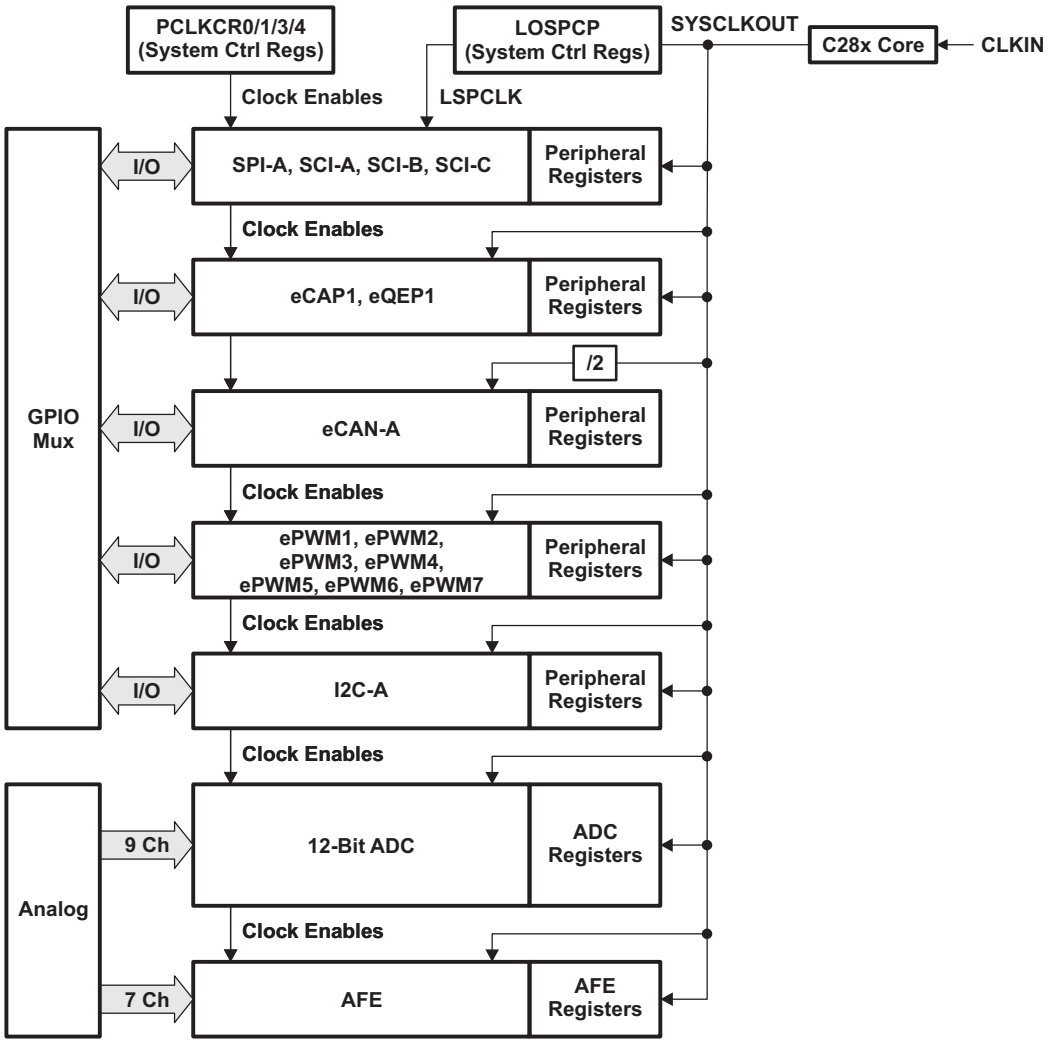
This section describes the oscillator and clocking mechanisms, the watchdog function and the low power modes.

Table 6-17. PLL, Clocking, Watchdog, and Low-Power Mode Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION(1)
BORCFG	0x00 0985	1	BOR Configuration Register
XCLK	0x00 7010	1	XCLKOUT Control
PLLSTS	0x00 7011	1	PLL Status Register
CLKCTL	0x00 7012	1	Clock Control Register
PLLLOCKPRD	0x00 7013	1	PLL Lock Period
INTOSC1TRIM	0x00 7014	1	Internal Oscillator 1 Trim Register
INTOSC2TRIM	0x00 7016	1	Internal Oscillator 2 Trim Register
LOSPCP	0x00 701B	1	Low-Speed Peripheral Clock Prescaler Register
PCLKCR0	0x00 701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x00 701D	1	Peripheral Clock Control Register 1
LPMCR0	0x00 701E	1	Low Power Mode Control Register 0
PCLKCR3	0x00 7020	1	Peripheral Clock Control Register 3
PLLCR	0x00 7021	1	PLL Control Register
SCSR	0x00 7022	1	System Control and Status Register
WDCNTR	0x00 7023	1	Watchdog Counter Register
PCLKCR4	0x00 7024	1	Peripheral Clock Control Register 4
WDKEY	0x00 7025	1	Watchdog Reset Key Register
WDCR	0x00 7029	1	Watchdog Control Register

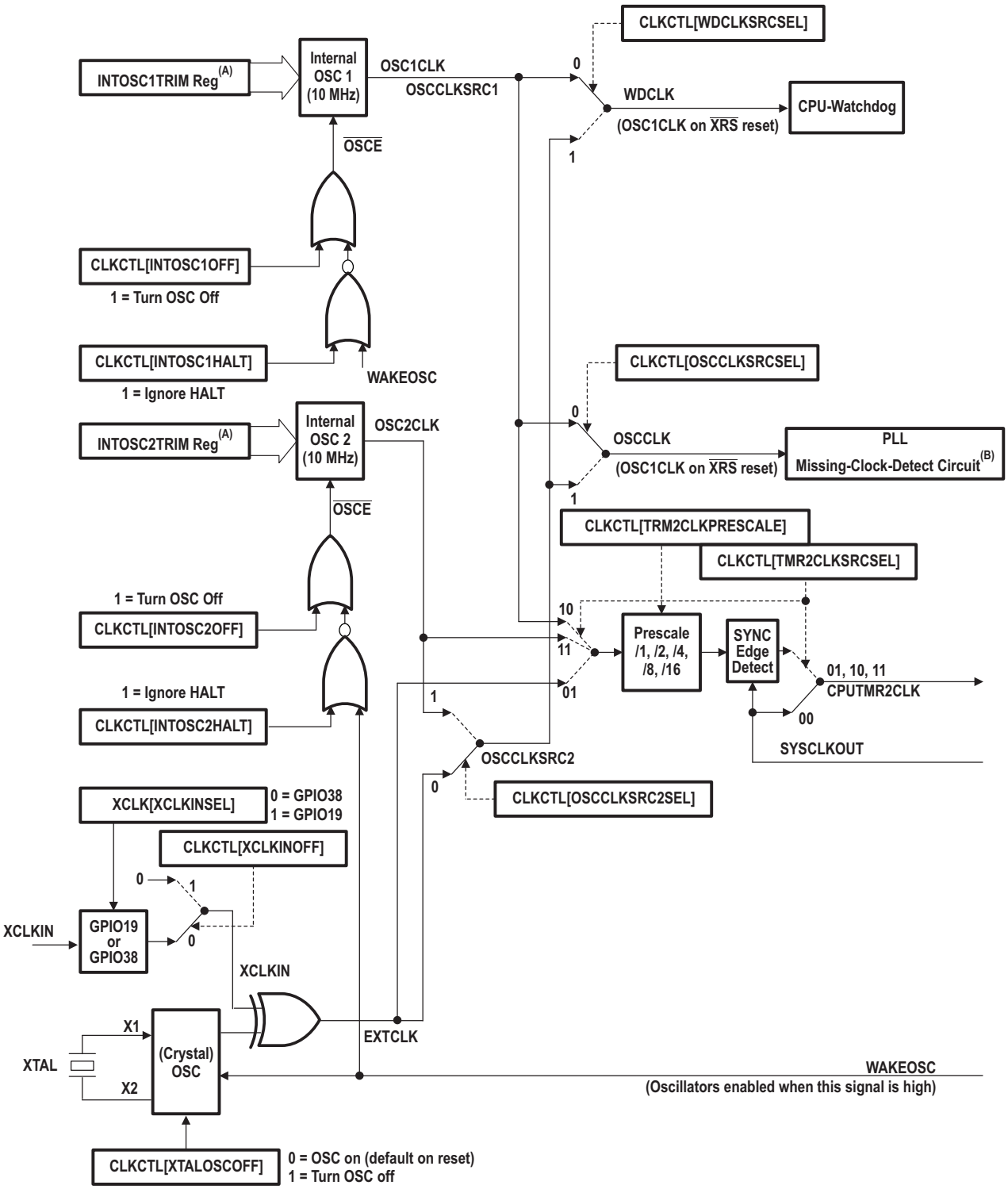
(1) All registers in this table are EALLOW protected.

Figure 6-6 shows the various clock domains that are discussed. Figure 6-7 shows the various clock sources (both internal and external) that can provide a clock for device operation.



A. CLKIN is the clock into the CPU. CLKIN is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 6-6. Clock and Reset Domains



A. Register loaded from TI OTP-based calibration function.
B. See Section 6.6.4 for details on missing clock detection.

Figure 6-7. Clock Tree

6.6.1 Internal Zero-Pin Oscillators

The F2805x devices contain two independent internal zero-pin oscillators. By default both oscillators are turned on at power up, and internal oscillator 1 is the default clock source at this time. For power savings, unused oscillators may be powered down by the user. The center frequency of these oscillators is determined by their respective oscillator trim registers, written to in the calibration routine as part of the boot ROM execution. See Section 5.12.1 for more information on these oscillators.

6.6.2 Crystal Oscillator Option

The typical specifications for the external quartz crystal (fundamental mode, parallel resonant) are listed in Table 6-18. Furthermore, ESR range = 30 to 150 Ω.

Table 6-18. Typical Specifications for External Quartz Crystal(1)

FREQUENCY (MHz)	R_d (Ω)	C_{L1} (pF)	C_{L2} (pF)
5	2200	18	18
10	470	15	15
15	0	15	15
20	0	12	12

(1) C_{shunt} should be less than or equal to 5 pF.

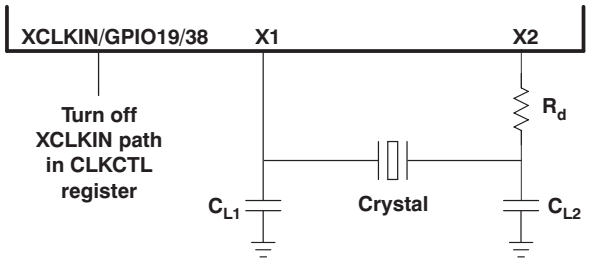


Figure 6-8. Using the On-chip Crystal Oscillator

NOTE

1. C_{L1} and C_{L2} are the total capacitance of the circuit board and components excluding the IC and crystal. The value is usually approximately twice the value of the crystal's load capacitance.
2. The load capacitance of the crystal is described in the crystal specifications of the manufacturers.
3. TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the MCU chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start up and stability over the entire operating range.

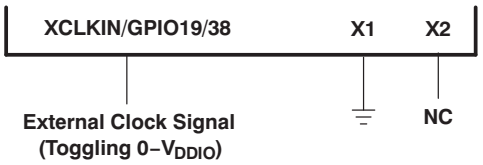


Figure 6-9. Using a 3.3-V External Oscillator

6.6.3 PLL-Based Clock Module

The devices have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. The watchdog module can be re-enabled (if need be) after the PLL module has stabilized, which takes 1 ms. The input clock and PLLCR[DIV] bits should be chosen in such a way that the output frequency of the PLL (VCOCLK) is at least 50 MHz.

Table 6-19. PLL Settings

PLLCR[DIV] VALUE(1) (2)	SYSCLKOUT (CLKIN)		
	PLLSTS[DIVSEL] = 0 or 1(3)	PLLSTS[DIVSEL] = 2	PLLSTS[DIVSEL] = 3
0000 (PLL bypass)	OSCCLK/4 (Default)(1)	OSCCLK/2	OSCCLK
0001	(OSCCLK * 1)/4	(OSCCLK * 1)/2	(OSCCLK * 1)/1
0010	(OSCCLK * 2)/4	(OSCCLK * 2)/2	(OSCCLK * 2)/1
0011	(OSCCLK * 3)/4	(OSCCLK * 3)/2	(OSCCLK * 3)/1
0100	(OSCCLK * 4)/4	(OSCCLK * 4)/2	(OSCCLK * 4)/1
0101	(OSCCLK * 5)/4	(OSCCLK * 5)/2	(OSCCLK * 5)/1
0110	(OSCCLK * 6)/4	(OSCCLK * 6)/2	(OSCCLK * 6)/1
0111	(OSCCLK * 7)/4	(OSCCLK * 7)/2	(OSCCLK * 7)/1
1000	(OSCCLK * 8)/4	(OSCCLK * 8)/2	(OSCCLK * 8)/1
1001	(OSCCLK * 9)/4	(OSCCLK * 9)/2	(OSCCLK * 9)/1
1010	(OSCCLK * 10)/4	(OSCCLK * 10)/2	(OSCCLK * 10)/1
1011	(OSCCLK * 11)/4	(OSCCLK * 11)/2	(OSCCLK * 11)/1
1100	(OSCCLK * 12)/4	(OSCCLK * 12)/2	(OSCCLK * 12)/1

(1) The PLL control register (PLLCR) and PLL Status Register (PLLSTS) are reset to their default state by the $\overline{\text{XRS}}$ signal or a watchdog reset only. A reset issued by the debugger or the missing clock detect logic has no effect.
(2) This register is EALLOW protected. See the System Control and Interrupts chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5) for more information.
(3) By default, PLLSTS[DIVSEL] is configured for /4. (The boot ROM changes the PLLSTS[DIVSEL] configuration to /1.) PLLSTS[DIVSEL] must be 0 before writing to the PLLCR and should be changed only after PLLSTS[PLLLOCKS] = 1.

Table 6-20. CLKIN Divide Options

PLLSTS [DIVSEL]	CLKIN DIVIDE
0	/4
1	/4
2	/2
3	/1

The PLL-based clock module provides four modes of operation:

- **INTOSC1 (Internal Zero-pin Oscillator 1):** INTOSC1 is the on-chip internal oscillator 1. INTOSC1 can provide the clock for the Watchdog block, core and CPU-Timer 2.
- **INTOSC2 (Internal Zero-pin Oscillator 2):** INTOSC2 is the on-chip internal oscillator 2. INTOSC2 can provide the clock for the Watchdog block, core and CPU-Timer 2. Both INTOSC1 and INTOSC2 can be independently chosen for the Watchdog block, core and CPU-Timer 2.
- **Crystal/Resonator Operation:** The on-chip (crystal) oscillator enables the use of an external crystal/resonator attached to the device to provide the time base. The crystal/resonator is connected to the X1/X2 pins. Some devices may not have the X1/X2 pins. See Table 4-1 for details.
- **External Clock Source Operation:** If the on-chip (crystal) oscillator is not used, this mode allows the on-chip (crystal) oscillator to be bypassed. The device clocks are generated from an external clock source input on the XCLKIN pin. Note that the XCLKIN is multiplexed with GPIO19 or GPIO38 pin. The XCLKIN input can be selected as GPIO19 or GPIO38 via the XCLKINSEL bit in XCLK register. The CLKCTL[XCLKINOFF] bit disables this clock input (forced low). If the clock source is not used or the respective pins are used as GPIOs, the user should disable at boot time.

Before changing clock sources, ensure that the target clock is present. If a clock is not present, then that clock source must be disabled (using the CLKCTL register) before switching clocks.

Table 6-21. Possible PLL Configuration Modes

PLL MODE	REMARKS	PLLSTS[DIVSEL]	CLKIN AND SYSCLKOUT
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. The PLL block being disabled can be useful in reducing system noise and for low-power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN.	0, 1	OSCCLK/4
		2	OSCCLK/2
		3	OSCCLK/1
PLL Bypass	PLL Bypass is the default PLL configuration upon power-up or after an external reset (XRS). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL itself is bypassed but the PLL is not turned off.	0, 1	OSCCLK/4
		2	OSCCLK/2
		3	OSCCLK/1
PLL Enable	Achieved by writing a non-zero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks.	0, 1	OSCCLK * n/4
		2	OSCCLK * n/2
		3	OSCCLK * n/1

6.6.4 Loss of Input Clock (NMI Watchdog Function)

The 2805x devices may be clocked from either one of the internal zero-pin oscillators (INTOSC1 or INTOSC2), the on-chip crystal oscillator, or from an external clock input. Regardless of the clock source, in PLL-enabled and PLL-bypass mode, if the input clock to the PLL vanishes, the PLL will issue a limp-mode clock at its output. This limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1–5 MHz.

When the limp mode is activated, a $\overline{\text{CLOCKFAIL}}$ signal is generated that is latched as an NMI interrupt. Depending on how the NMIRESETSEL bit has been configured, a reset to the device can be fired immediately or the NMI watchdog counter can issue a reset when the counter overflows. In addition to this action, the Missing Clock Status (MCLKSTS) bit is set. The NMI interrupt could be used by the application to detect the input clock failure and initiate necessary corrective action such as switching over to an alternative clock source (if available) or initiate a shut-down procedure for the system.

If the software does not respond to the clock-fail condition, the NMI watchdog triggers a reset after a preprogrammed time interval. Figure 6-10 shows the interrupt mechanisms involved.

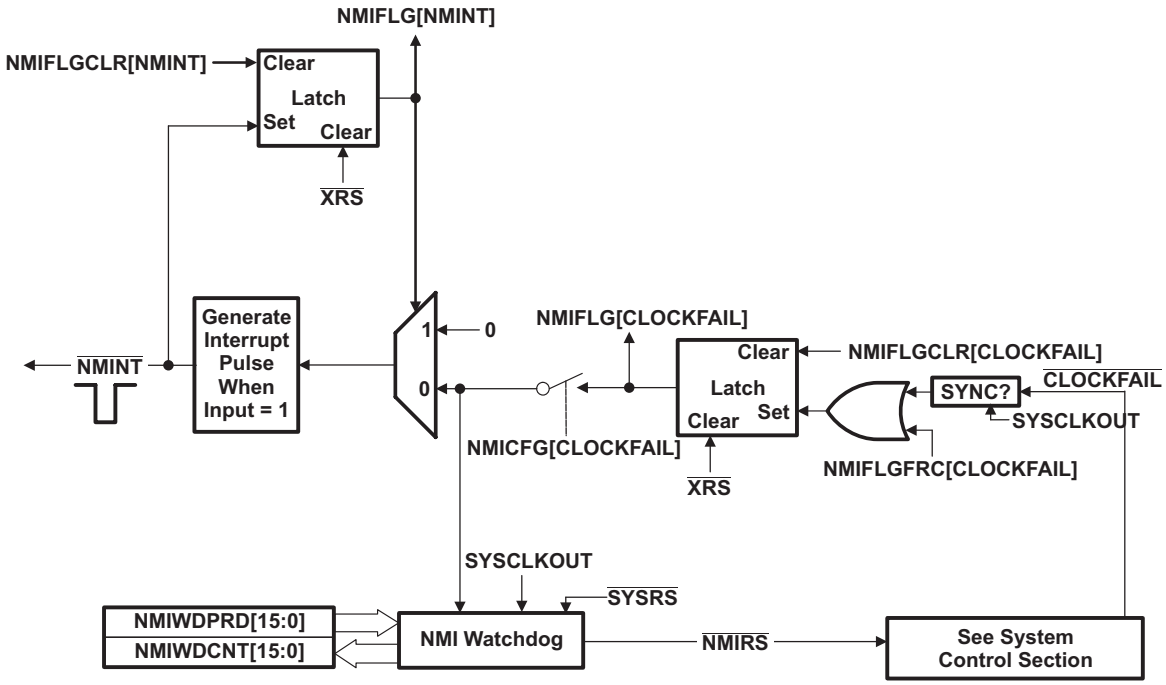


Figure 6-10. NMI-watchdog

6.6.5 CPU-Watchdog Module

The CPU-watchdog module on the 2805x device is similar to the one used on the 281x, 280x, and 283xx devices. This module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this occurrence, the user must disable the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register that resets the watchdog counter. Figure 6-11 shows the various functional blocks within the watchdog module.

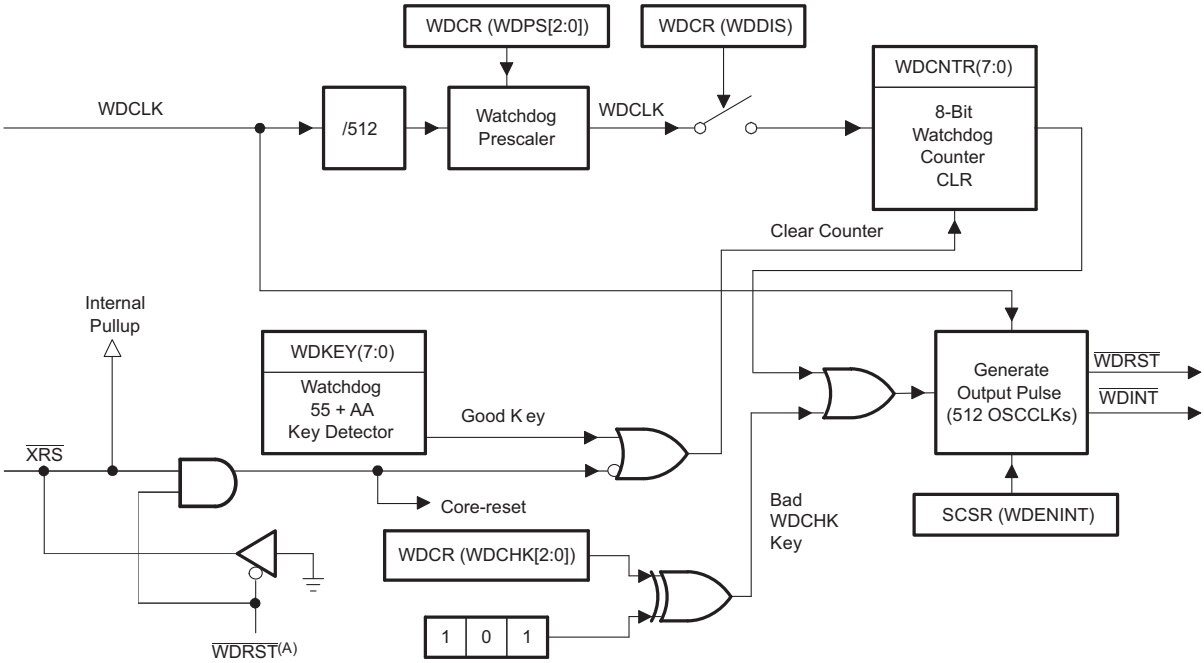
Normally, when the input clocks are present, the CPU-watchdog counter decrements to initiate a CPU-watchdog reset or WDINT interrupt. However, when the external input clock fails, the CPU-watchdog counter stops decrementing (that is, the watchdog counter does not change with the limp-mode clock).

NOTE

The CPU-watchdog is different from the NMI watchdog. The CPU-watchdog is the legacy watchdog that is present in all 28x devices.

NOTE

Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the MCU will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{\text{XRS}}$ pin of the MCU, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent the capacitor from getting fully charged. Such a circuit would also help in detecting failure of the flash memory.



A. The $\overline{\text{WDRST}}$ signal is driven low for 512 OSCCLK cycles.

Figure 6-11. CPU-watchdog Module

The $\overline{\text{WDINT}}$ signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the CPU-watchdog. This module will run off OSCCLK. The $\overline{\text{WDINT}}$ signal is fed to the LPM block so that the signal can wake the device from STANDBY (if enabled). See Section 6.7, Low-power Modes Block, for more details.

In IDLE mode, the $\overline{\text{WDINT}}$ signal can generate an interrupt to the CPU, via the PIE, to take the CPU out of IDLE mode.

In HALT mode, the CPU-watchdog can be used to wake up the device through a device reset.

6.7 Low-power Modes Block

Table 6-22 summarizes the various modes.

Table 6-22. Low-power Modes

MODE	LPMCR0(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT(1)
IDLE	00	On	On	On	$\overline{\text{XRS}}$, CPU-watchdog interrupt, any enabled interrupt
STANDBY	01	On (CPU-watchdog still running)	Off	Off	$\overline{\text{XRS}}$, CPU-watchdog interrupt, GPIO Port A signal, debugger(2)
HALT(3)	1X	Off (on-chip crystal oscillator and PLL turned off, zero-pin oscillator and CPU-watchdog state dependent on user code.)	Off	Off	$\overline{\text{XRS}}$, GPIO Port A signal, debugger(2), CPU-watchdog

(1) The Exit column lists which signals or under what conditions the low power mode is exited. A low signal, on any of the signals, exits the low power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise, the low-power mode will not be exited and the device will go back into the indicated low power mode.
(2) The JTAG port can still function even if the CPU clock (CLKIN) is turned off.
(3) The WDCLK must be active for the device to go into HALT mode.

The various low-power modes operate as follows:

IDLE Mode: This mode is exited by any enabled interrupt that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.

STANDBY Mode: Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signals will wake the device in the GPIOLPMSEL register. The selected signals are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.

HALT Mode: CPU-watchdog, $\overline{\text{XRS}}$, and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

NOTE

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed. See the System Control and Interrupts chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5) for more details.

6.8 Interrupts

Figure 6-12 shows how the various interrupt sources are multiplexed.

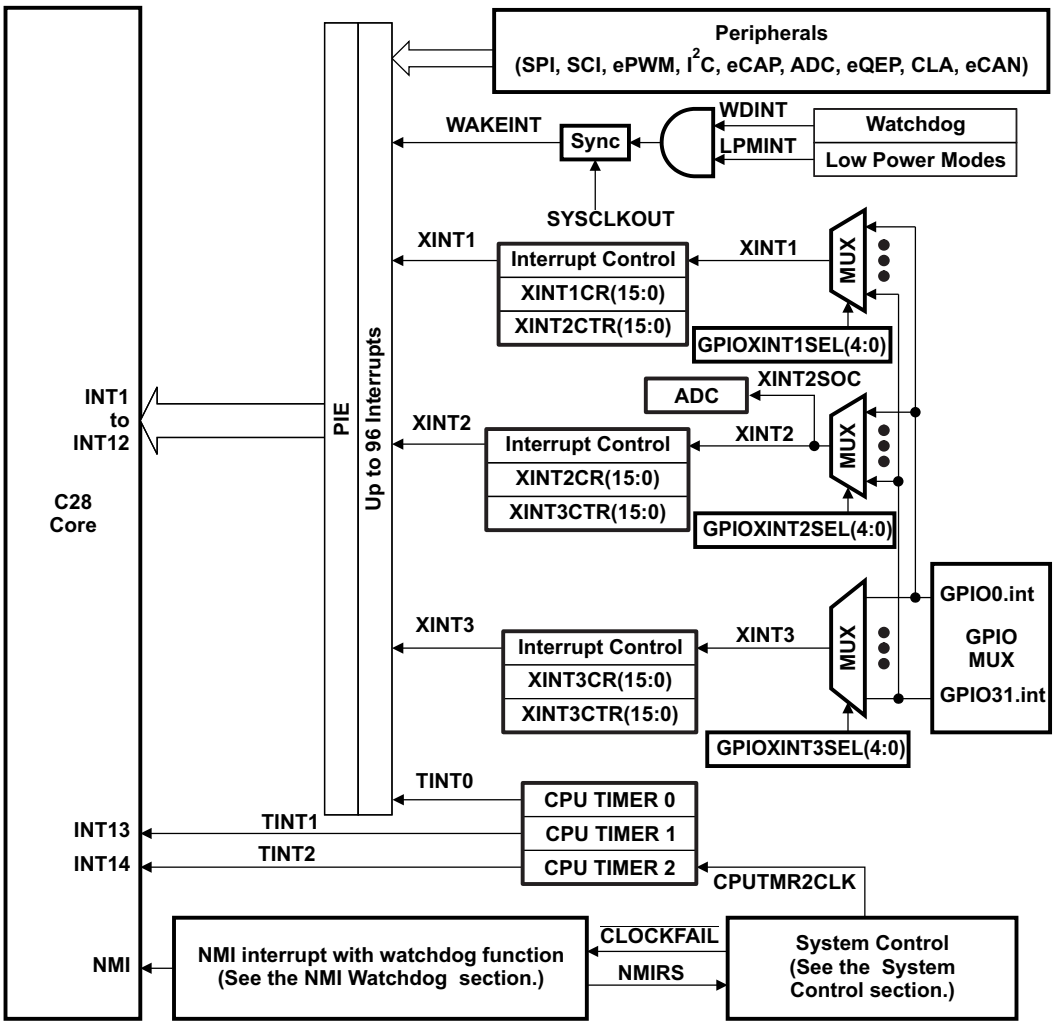


Figure 6-12. External and PIE Interrupt Sources

Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. Table 6-23 shows the interrupts used by 2805x devices.

The TRAP #VectorNumber instruction transfers program control to the interrupt service routine corresponding to the vector specified. TRAP #0 attempts to transfer program control to the address pointed to by the reset vector. The PIE vector table does not, however, include a reset vector. Therefore, TRAP #0 should not be used when the PIE is enabled. Doing so will result in undefined behavior.

When the PIE is enabled, TRAP #1 through TRAP #12 will transfer program control to the interrupt service routine corresponding to the first vector within the PIE group. For example: TRAP #1 fetches the vector from INT1.1, TRAP #2 fetches the vector from INT2.1, and so forth.

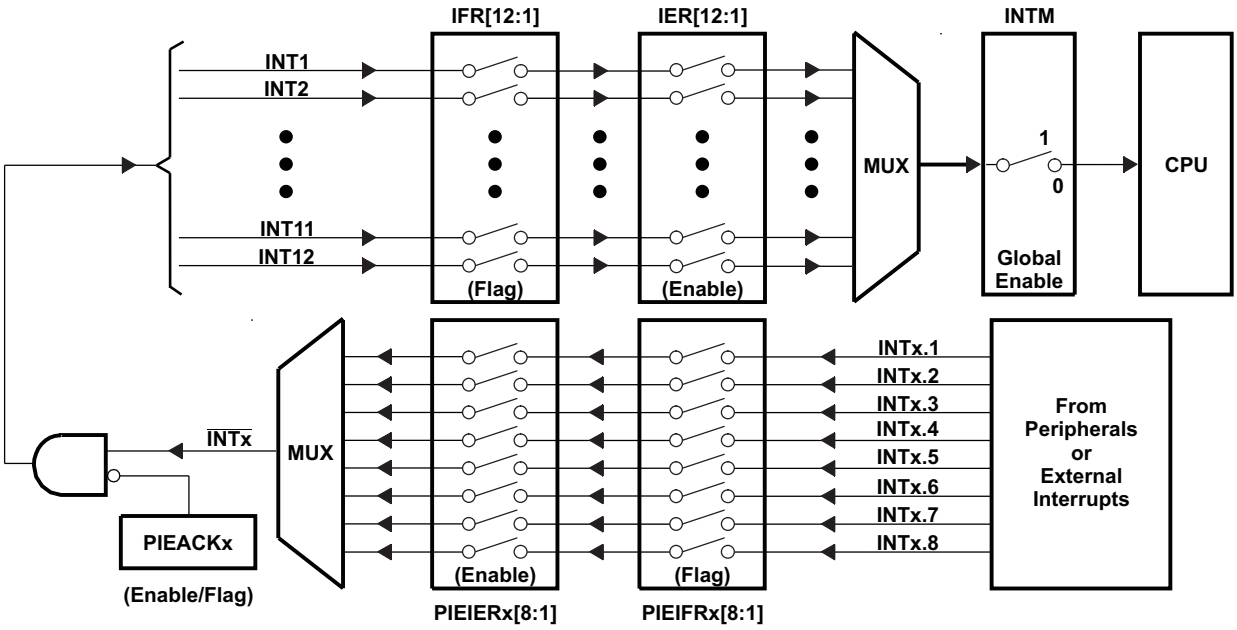


Figure 6-13. Multiplexing of Interrupts Using the PIE Block

Table 6-23. PIE MUXed Peripheral Interrupt Vector Table(1)

	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1.y	WAKEINT (LPM/WD) 0xD4E	TINT0 (TIMER 0) 0xD4C	ADCINT9 (ADC) 0xD4A	XINT2 Ext. int. 2 0xD48	XINT1 Ext. int. 1 0xD46	Reserved – 0xD44	ADCINT2 (ADC) 0xD42	ADCINT1 (ADC) 0xD40
INT2.y	Reserved – 0xD5E	EPWM7_TZINT (ePWM7) 0xD5C	EPWM6_TZINT (ePWM6) 0xD5A	EPWM5_TZINT (ePWM5) 0xD58	EPWM4_TZINT (ePWM4) 0xD56	EPWM3_TZINT (ePWM3) 0xD54	EPWM2_TZINT (ePWM2) 0xD52	EPWM1_TZINT (ePWM1) 0xD50
INT3.y	Reserved – 0xD6E	EPWM7_INT (ePWM7) 0xD6C	EPWM6_INT (ePWM6) 0xD6A	EPWM5_INT (ePWM5) 0xD68	EPWM4_INT (ePWM4) 0xD66	EPWM3_INT (ePWM3) 0xD64	EPWM2_INT (ePWM2) 0xD62	EPWM1_INT (ePWM1) 0xD60
INT4.y	Reserved – 0xD7E	Reserved – 0xD7C	Reserved – 0xD7A	Reserved – 0xD78	Reserved – 0xD76	Reserved – 0xD74	Reserved – 0xD72	ECAP1_INT (eCAP1) 0xD70
INT5.y	Reserved – 0xD8E	Reserved – 0xD8C	Reserved – 0xD8A	Reserved – 0xD88	Reserved – 0xD86	Reserved – 0xD84	Reserved – 0xD82	EQEP1_INT (eQEP1) 0xD80
INT6.y	Reserved – 0xD9E	Reserved – 0xD9C	Reserved – 0xD9A	Reserved – 0xD98	Reserved – 0xD96	Reserved – 0xD94	SPITXINTA (SPI-A) 0xD92	SPIRXINTA (SPI-A) 0xD90
INT7.y	Reserved – 0xDAE	Reserved – 0xDAC	Reserved – 0xDAA	Reserved – 0xDA8	Reserved – 0xDA6	Reserved – 0xDA4	Reserved – 0xDA2	Reserved – 0xDA0
INT8.y	Reserved – 0xDBE	Reserved – 0xDBC	SCITXINTC (SCI-C) 0xDBA	SCIRXINTC (SCI-C) 0xDB8	Reserved – 0xDB6	Reserved – 0xDB4	I2CINT2A (I2C-A) 0xDB2	I2CINT1A (I2C-A) 0xDB0
INT9.y	Reserved – 0xDCE	Reserved – 0xDCC	ECAN1_INTA (CAN-A) 0xDCA	ECAN0_INTA (CAN-A) 0xDC8	SCITXINTB (SCI-B) 0xDC6	SCIRXINTB (SCI-B) 0xDC4	SCITXINTA (SCI-A) 0xDC2	SCIRXINTA (SCI-A) 0xDC0
INT10.y	ADCINT8 (ADC) (ePWM16) 0xDDE	ADCINT7 (ADC) (ePWM15) 0xDDC	ADCINT6 (ADC) (ePWM14) 0xDDA	ADCINT5 (ADC) (ePWM13) 0xDD8	ADCINT4 (ADC) (ePWM12) 0xDD6	ADCINT3 (ADC) (ePWM11) 0xDD4	ADCINT2 (ADC) (ePWM10) 0xDD2	ADCINT1 (ADC) (ePWM9) 0xDD0
INT11.y	CLA1_INT8 (CLA) (ePWM16) 0xDEE	CLA1_INT7 (CLA) (ePWM15) 0xDEC	CLA1_INT6 (CLA) (ePWM14) 0xDEA	CLA1_INT5 (CLA) (ePWM13) 0xDE8	CLA1_INT4 (CLA) (ePWM12) 0xDE6	CLA1_INT3 (CLA) (ePWM11) 0xDE4	CLA1_INT2 (CLA) (ePWM10) 0xDE2	CLA1_INT1 (CLA) (ePWM9) 0xDE0
INT12.y	LUF (CLA) 0xDFE	LVF (CLA) 0xDFC	Reserved – 0xDFA	Reserved – 0xDF8	Reserved – 0xDF6	Reserved – 0xDF4	Reserved – 0xDF2	XINT3 Ext. Int. 3 0xDF0

(1) Out of 96 possible interrupts, some interrupts are not used. These interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR. To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:
- No peripheral within the group is asserting interrupts.
- No peripheral interrupts are assigned to the group (for example, PIE group 7).

Table 6-24. PIE Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION(1)
PIECTRL	0x0CE0	1	PIE, Control Register
PIEACK	0x0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0CFA – 0x0CFF	6	Reserved

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

6.8.1 External Interrupts

Table 6-25. External Interrupt Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XINT1CR	0x00 7070	1	XINT1 configuration register
XINT2CR	0x00 7071	1	XINT2 configuration register
XINT3CR	0x00 7072	1	XINT3 configuration register
XINT1CTR	0x00 7078	1	XINT1 counter register
XINT2CTR	0x00 7079	1	XINT2 counter register
XINT3CTR	0x00 707A	1	XINT3 counter register

Each external interrupt can be enabled, disabled, or qualified using positive, negative, or both positive and negative edge. For more information, see the System Control and Interrupts chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5).

6.8.1.1 External Interrupt Electrical Data/Timing

Table 6-26. External Interrupt Timing Requirements (1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(INT)}$ (2)	Pulse duration, INT input low/high	Synchronous	$1t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-72.
(2) This timing is applicable to any GPIO pin configured for ADCSOC functionality.

Table 6-27. External Interrupt Switching Characteristics (1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch		$t_{w(IQSW)} + 12t_{c(SCO)}$	cycles

(1) For an explanation of the input qualifier parameters, see Table 6-72.

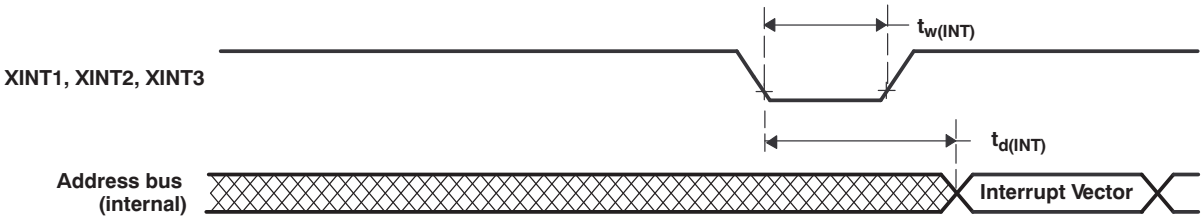


Figure 6-14. External Interrupt Timing

6.9 Peripherals

6.9.1 Control Law Accelerator

6.9.1.1 CLA Device-Specific Information

The CLA extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Utilizing the CLA for time-critical tasks frees up the main CPU to perform other system and communication functions concurently. The following is a list of major features of the CLA.

- Clocked at the same rate as the main CPU (SYSCLKOUT).
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU.
  - Complete bus architecture:
    - Program address bus and program data bus
    - Data address bus, data read bus, and data write bus
  - Independent eight-stage pipeline.
  - 12-bit program counter (MPC)
  - Four 32-bit result registers (MR0–MR3)
  - Two 16-bit auxillary registers (MAR0, MAR1)
  - Status register (MSTF)
- Instruction set includes:
  - IEEE single-precision (32-bit) floating-point math operations
  - Floating-point math with parallel load or store
  - Floating-point multiply with parallel add or subtract
  - 1/X and 1/sqrt(X) estimations
  - Data type conversions.
  - Conditional branch and call
  - Data load and store operations
- The CLA program code can consist of up to eight tasks or interrupt service routines.
  - The start address of each task is specified by the MVECT registers.
  - No limit on task size as long as the tasks fit within the CLA program memory space.
  - One task is serviced at a time through to completion. There is no nesting of tasks.
  - Upon task completion, a task-specific interrupt is flagged within the PIE.
  - When a task finishes, the next highest-priority pending task is automatically started.
- Task trigger mechanisms:
  - C28x CPU via the IACK instruction
  - Task1 to Task7: the corresponding ADC, ePWM, eQEP, or eCAP module interrupt. For example:
    - Task1: ADCINT1 or EPWM1_INT
    - Task2: ADCINT2 or EPWM2_INT
    - Task4: ADCINT4 or EPWM4_INT or EQEPx_INT or ECAPx_INT
    - Task7: ADCINT7 or EPWM7_INT or EQEPx_INT or ECAPx_INT
  - Task8: ADCINT8 or by CPU Timer 0 or EQEPx_INT or ECAPx_INT
- Memory and Shared Peripherals:
  - Two dedicated message RAMs for communication between the CLA and the main CPU.
  - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.
  - The CLA has direct access to the CLA Data ROM that stores the math tables required by the routines in the CLA Math Library.
  - The CLA has direct access to the ADC Result registers, comparator and DAC registers, eCAP, eQEP, and ePWM registers.

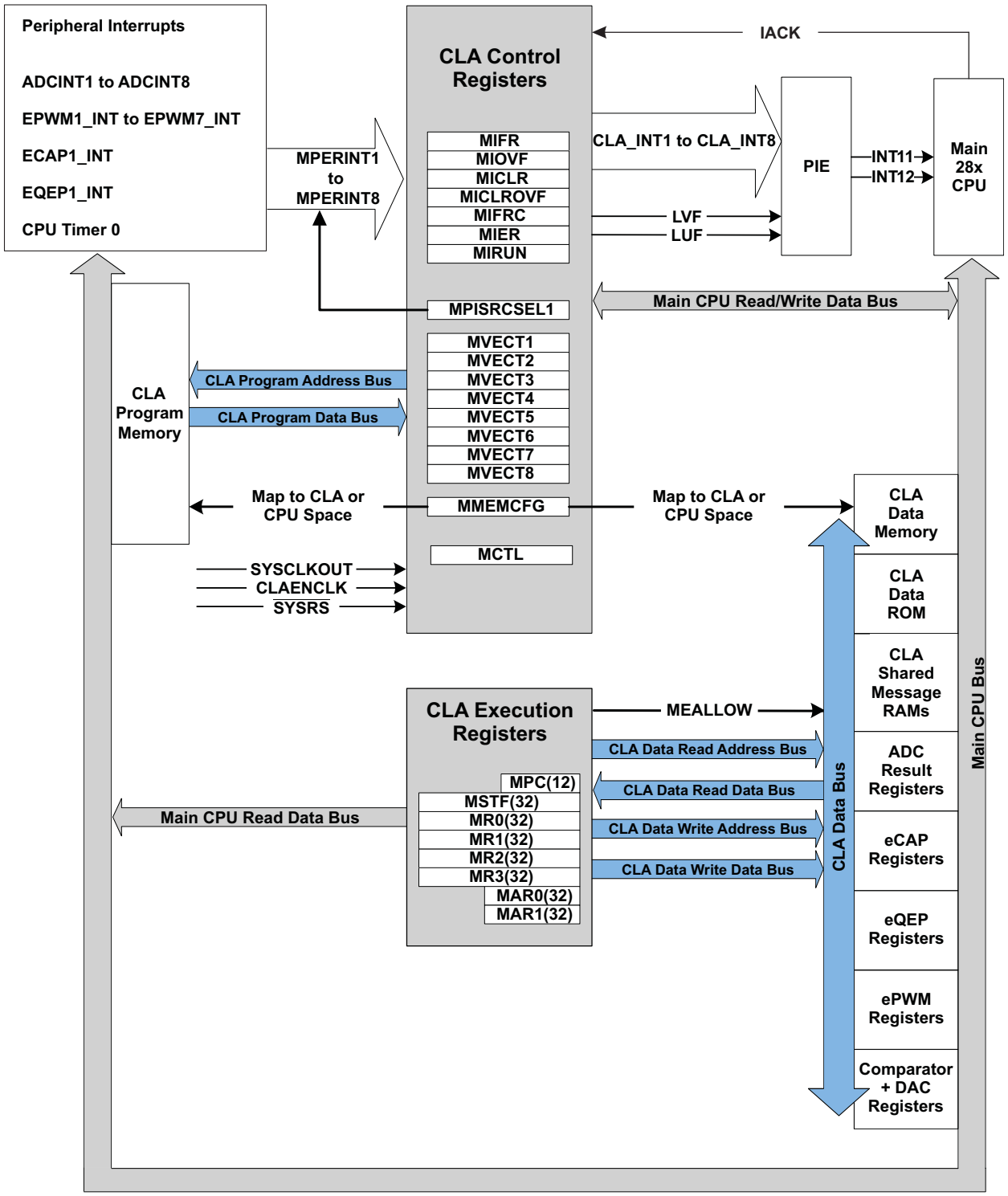


Figure 6-15. CLA Block Diagram

6.9.1.2 CLA Register Descriptions

Table 6-28. CLA Control Registers

REGISTER NAME	CLA1 ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION(1)
MVECT1	0x1400	1	Yes	CLA Interrupt/Task 1 Start Address
MVECT2	0x1401	1	Yes	CLA Interrupt/Task 2 Start Address
MVECT3	0x1402	1	Yes	CLA Interrupt/Task 3 Start Address
MVECT4	0x1403	1	Yes	CLA Interrupt/Task 4 Start Address
MVECT5	0x1404	1	Yes	CLA Interrupt/Task 5 Start Address
MVECT6	0x1405	1	Yes	CLA Interrupt/Task 6 Start Address
MVECT7	0x1406	1	Yes	CLA Interrupt/Task 7 Start Address
MVECT8	0x1407	1	Yes	CLA Interrupt/Task 8 Start Address
MCTL	0x1410	1	Yes	CLA Control Register
MMEMCFG	0x1411	1	Yes	CLA Memory Configure Register
MPISRCSEL1	0x1414	2	Yes	Peripheral Interrupt Source Select Register 1
MIFR	0x1420	1	Yes	Interrupt Flag Register
MIOVF	0x1421	1	Yes	Interrupt Overflow Register
MIFRC	0x1422	1	Yes	Interrupt Force Register
MICLR	0x1423	1	Yes	Interrupt Clear Register
MICLROVF	0x1424	1	Yes	Interrupt Overflow Clear Register
MIER	0x1425	1	Yes	Interrupt Enable Register
MIRUN	0x1426	1	Yes	Interrupt RUN Register
MPC(2)	0x1428	1	–	CLA Program Counter
MAR0(2)	0x142A	1	–	CLA Aux Register 0
MAR1(2)	0x142B	1	–	CLA Aux Register 1
MSTF(2)	0x142E	2	–	CLA STF Register
MR0(2)	0x1430	2	–	CLA R0H Register
MR1(2)	0x1434	2	–	CLA R1H Register
MR2(2)	0x1438	2	–	CLA R2H Register
MR3(2)	0x143C	2	–	CLA R3H Register

(1) All registers in this table are DCSM protected
(2) The main C28x CPU has read only access to this register for debug purposes. The main CPU cannot perform CPU or debugger writes to this register.

Table 6-29. CLA Message RAM

ADDRESS RANGE	SIZE (x16)	DESCRIPTION
0x1480 – 0x14FF	128	CLA to CPU Message RAM
0x1500 – 0x157F	128	CPU to CLA Message RAM

6.9.2 Analog Block

6.9.2.1 Analog-to-Digital Converter

6.9.2.1.1 ADC Device-Specific Information

The core of the ADC contains a single 12-bit converter fed by two sample-and-hold circuits. The sample-and-hold circuits can be sampled simultaneously or sequentially. These, in turn, are fed by a total of up to 16 analog input channels. The converter can be configured to run with an internal bandgap reference to create true-voltage based conversions or with a pair of external voltage references (V_{REFHI}/V_{REFLO}) to create ratiometric-based conversions.

Contrary to previous ADC types, this ADC is not sequencer-based. The user can easily create a series of conversions from a single trigger. However, the basic principle of operation is centered around the configurations of individual conversions, called SOCs, or Start-Of-Conversions.

Functions of the ADC module include:

- 12-bit ADC core with built-in dual sample-and-hold (S/H)
- Simultaneous sampling or sequential sampling modes
- Full range analog input: 0 V to 3.3 V fixed, or V_{REFHI}/V_{REFLO} ratiometric. The digital value of the input analog voltage is derived by:
  - Internal Reference (V_{REFLO} = V_{SSA}. V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes.)

$$\text{Digital Value} = 0, \quad \text{when input} \le 0\ \text{V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{3.3}, \quad \text{when } 0\ \text{V} < \text{input} < 3.3\ \text{V}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \ge 3.3\ \text{V}$$

  - External Reference (V_{REFHI}/V_{REFLO} connected to external references. V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes.)

$$\text{Digital Value} = 0, \quad \text{when input} \le 0\ \text{V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{V_{REFHI} - V_{REFLO}}, \quad \text{when } 0\ \text{V} < \text{input} < V_{REFHI}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \ge V_{REFHI}$$

- Up to 16-channel, multiplexed inputs
- 16 SOCs, configurable for trigger, sample window, and channel
- 16 result registers (individually addressable) to store conversion values
- Multiple trigger sources
  - S/W – software immediate start
  - ePWM 1–7
  - GPIO XINT2
  - CPU Timer 0, CPU Timer 1, CPU Timer 2
  - ADCINT1, ADCINT2
- 9 flexible PIE interrupts, can configure interrupt request after any conversion

Table 6-30. ADC Configuration and Control Registers

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCCTL1	0x7100	1	Yes	Control 1 Register
ADCCTL2	0x7101	1	Yes	Control 2 Register
ADCINTFLG	0x7104	1	No	Interrupt Flag Register
ADCINTFLGCLR	0x7105	1	No	Interrupt Flag Clear Register
ADCINTOVF	0x7106	1	No	Interrupt Overflow Register
ADCINTOVFCLR	0x7107	1	No	Interrupt Overflow Clear Register
INTSEL1N2	0x7108	1	Yes	Interrupt 1 and 2 Selection Register
INTSEL3N4	0x7109	1	Yes	Interrupt 3 and 4 Selection Register
INTSEL5N6	0x710A	1	Yes	Interrupt 5 and 6 Selection Register
INTSEL7N8	0x710B	1	Yes	Interrupt 7 and 8 Selection Register
INTSEL9N10	0x710C	1	Yes	Interrupt 9 Selection Register (reserved Interrupt 10 Selection)
SOCPRICTL	0x7110	1	Yes	SOC Priority Control Register
ADCSAMPLEMODE	0x7112	1	Yes	Sampling Mode Register
ADCINTSOCSEL1	0x7114	1	Yes	Interrupt SOC Selection 1 Register (for 8 channels)
ADCINTSOCSEL2	0x7115	1	Yes	Interrupt SOC Selection 2 Register (for 8 channels)
ADCSOCFLG1	0x7118	1	No	SOC Flag 1 Register (for 16 channels)
ADCSOCFRC1	0x711A	1	No	SOC Force 1 Register (for 16 channels)
ADCSOCOVF1	0x711C	1	No	SOC Overflow 1 Register (for 16 channels)
ADCSOCOVFCLR1	0x711E	1	No	SOC Overflow Clear 1 Register (for 16 channels)
ADCSOC0CTL to ADCSOC15CTL	0x7120 – 0x712F	1	Yes	SOC0 Control Register to SOC15 Control Register
ADCREFTRIM	0x7140	1	Yes	Reference Trim Register
ADCOFFTRIM	0x7141	1	Yes	Offset Trim Register
ADCREV	0x714F	1	No	Revision Register

Table 6-31. ADC Result Registers (Mapped to PF0)

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCRESULT0 to ADCRESULT15	0xB00 – 0xB0F	1	No	ADC Result 0 Register to ADC Result 15 Register

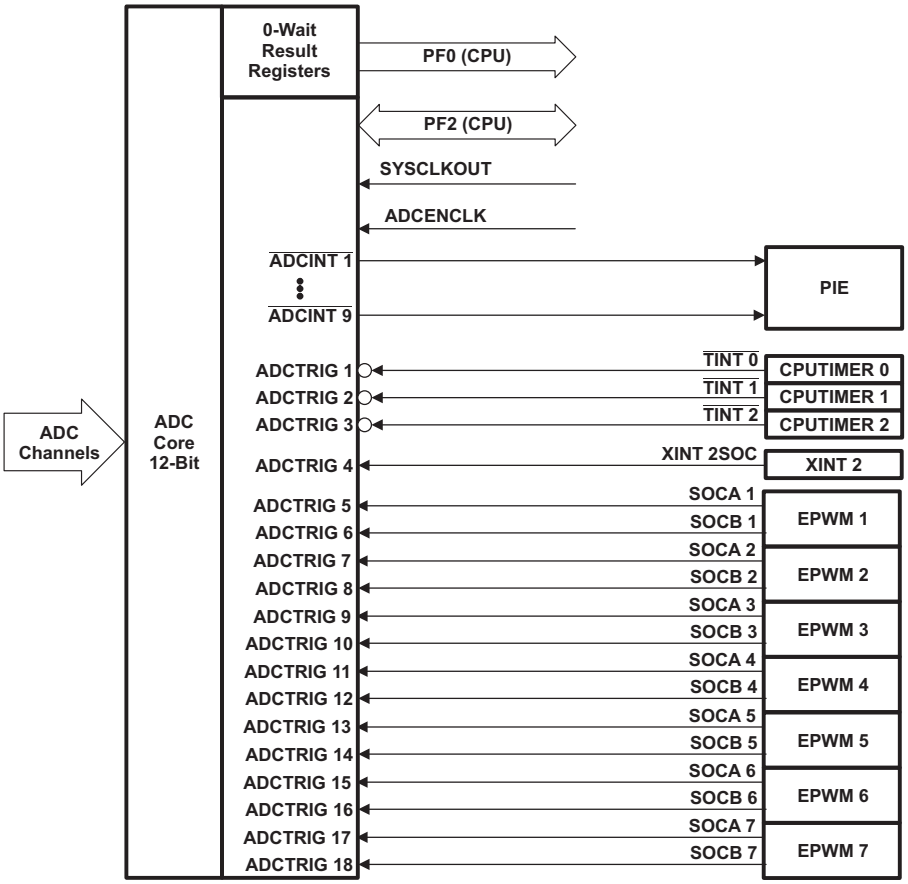


Figure 6-16. ADC Connections

ADC Connections if the ADC is Not Used

TI recommends that the connections for the analog power pins be kept, even if the ADC is not used. Following is a summary of how the ADC pins should be connected, if the ADC is not used in an application:

- V_{DDA} – Connect to V_{DDIO}
- V_{SSA} – Connect to V_{SS}
- V_{REFLO} – Connect to V_{SS}
- ADCINAn, ADCINBn, V_{REFHI} – Connect to V_{SSA}

When the ADC module is used in an application, unused ADC input pins should be connected to analog ground (V_{SSA}).

When the ADC is not used, be sure that the clock to the ADC module is not turned on to realize power savings.

6.9.2.1.2 ADC Electrical Data/Timing

Table 6-32. ADC Electrical Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
DC SPECIFICATIONS					
Resolution		12			Bits
ADC clock		0.5		60	MHz
Sample Window (see Table 6-33)	28055, 28054, 28053, 28052	10		63	ADC Clocks
	28051, 28050	24		63	
ACCURACY					
INL (Integral nonlinearity) (1)		–4		4.5	LSB
DNL (Differential nonlinearity), no missing codes		–1		1.5	LSB
Offset error (2)	Executing a single self-recalibration (3)	–20	0	20	LSB
	Executing periodic self-recalibration (4)	–4	0	4	
Overall gain error with internal reference		–60		60	LSB
Overall gain error with external reference		–40		40	LSB
Channel-to-channel offset variation		–4		4	LSB
Channel-to-channel gain variation		–4		4	LSB
ADC temperature coefficient with internal reference			–50		ppm/°C
ADC temperature coefficient with external reference			–20		ppm/°C
V_{REFLO}			–100		µA
V_{REFHI}			100		µA
ANALOG INPUT					
Analog input voltage with internal reference		0		3.3	V
Analog input voltage with external reference		V_{REFLO}		V_{REFHI}	V
V_{REFLO} input voltage		V_{SSA}		0.66	V
V_{REFHI} input voltage (5)		2.64		V_{DDA}	V
	with $V_{REFLO} = V_{SSA}$	1.98		V_{DDA}	
Input capacitance			5		pF
Input leakage current			±2		µA

(1) INL will degrade when the ADC input voltage goes above V_{DDA}.
(2) 1 LSB has the weighted value of full-scale range (FSR)/4096. FSR is 3.3 V with internal reference and V_{REFHI} - V_{REFLO} for external reference.
(3) For more details, see the *TMS320F28055, TMS320F28054, TMS320F28053, TMS320F28052, TMS320F28051, TMS320F28050 Piccolo MCU Silicon Errata* (SPRZ362).
(4) Periodic self-recalibration will remove system-level and temperature dependencies on the ADC zero offset error. This can be performed as needed in the application without sacrificing an ADC channel by using the procedure listed in the "ADC Zero Offset Calibration" section in the Analog-to-Digital Converter and Comparator chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5).
(5) V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes.

Table 6-33. ACQPS Values (1)

	OVERLAP MODE	NONOVERLAP MODE
Non-PGA	{9, 10, 23, 36, 49, 62}	{15, 16, 28, 29, 41, 42, 54, 55}
PGA	{23, 36, 49, 62}	{15, 16, 28, 29, 41, 42, 54, 55}

(1) ACQPS = 6 can be used for the first sample if it is thrown away.

Table 6-34. ADC Power Modes

ADC OPERATING MODE	CONDITIONS	I_{DDA}	UNITS
Mode A – Operating Mode	ADC Clock Enabled Bandgap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 1) ADC Powered Up (ADCPWDN = 1)	13	mA
Mode B – Quick Wake Mode	ADC Clock Enabled Bandgap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 1) ADC Powered Up (ADCPWDN = 0)	4	mA
Mode C – Comparator-Only Mode	ADC Clock Enabled Bandgap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 0) ADC Powered Up (ADCPWDN = 0)	1.5	mA
Mode D – Off Mode	ADC Clock Enabled Bandgap On (ADCBGPWD = 0) Reference On (ADCREFPWD = 0) ADC Powered Up (ADCPWDN = 0)	0.075	mA

6.9.2.1.2.1 External ADC Start-of-Conversion Electrical Data/Timing

Table 6-35. External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{\text{ADCSOCxO}}$ low	$32t_{c(HCO)}$		cycles

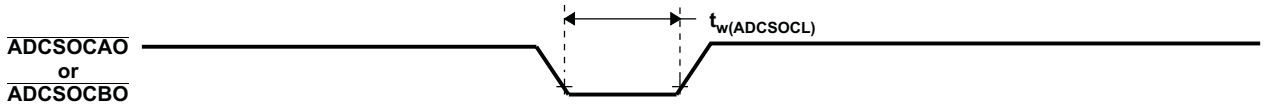


Figure 6-17. $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ Timing

6.9.2.1.2.2 Internal Temperature Sensor

Table 6-36. Temperature Sensor Coefficient(1)

PARAMETER(2)		MIN	TYP	MAX	UNIT
T_{SLOPE}	Degrees C of temperature movement per measured ADC LSB change of the temperature sensor		0.18(3)(4)		°C/LSB
T_{OFFSET}	ADC output at 0°C of the temperature sensor		1750		LSB

(1) The accuracy of the temperature sensor for sensing absolute temperature (temperature in degrees) is not specified. The primary use of the temperature sensor should be to compensate the internal oscillator for temperature drift (this operation is assured as per Table 5-7).
(2) The temperature sensor slope and offset are given in terms of ADC LSBs using the internal reference of the ADC. Values must be adjusted accordingly in external reference mode to the external reference voltage.
(3) ADC temperature coeffieicient is accounted for in this specification
(4) Output of the temperature sensor (in terms of LSBs) is sign-consistent with the direction of the temperature movement. Increasing temperatures will give increasing ADC values relative to an initial value; decreasing temperatures will give decreasing ADC values relative to an initial value.

6.9.2.1.2.3 ADC Power-Up Control Bit Timing

Table 6-37. ADC Power-Up Delays

PARAMETER(1)		MIN	MAX	UNIT
$t_{d(PWD)}$	Delay time for the ADC to be stable after power up		1	ms

(1) Timings maintain compatibility to the ADC module. The 2805x ADC supports driving all 3 bits at the same time $t_{d(PWD)}$ ms before first conversion.

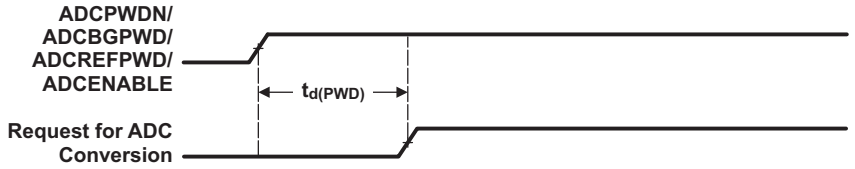
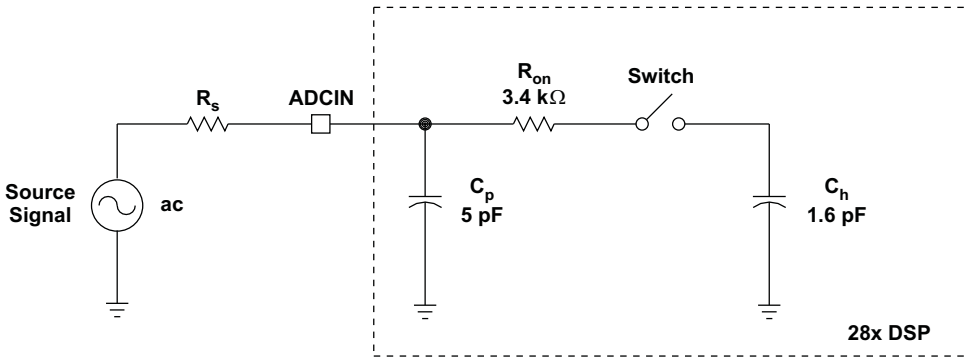


Figure 6-18. ADC Conversion Timing



Typical Values of the Input Circuit Components:

Switch Resistance (R_{on}): 3.4 kΩ
Sampling Capacitor (C_h): 1.6 pF
Parasitic Capacitance (C_p): 5 pF
Source Resistance (R_s): 50 Ω

Figure 6-19. ADC Input Impedance Model

6.9.2.1.2.4 ADC Sequential and Simultaneous Timings

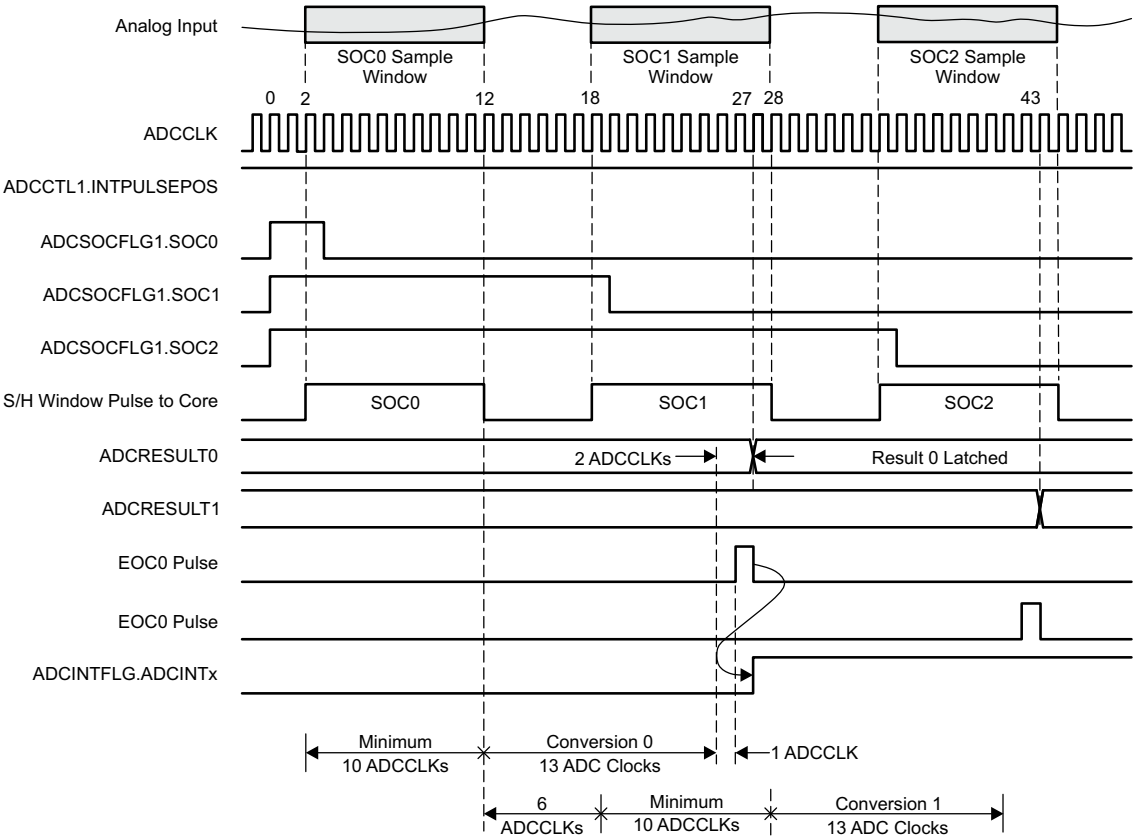


Figure 6-20. Timing Example for Sequential Mode / Late Interrupt Pulse

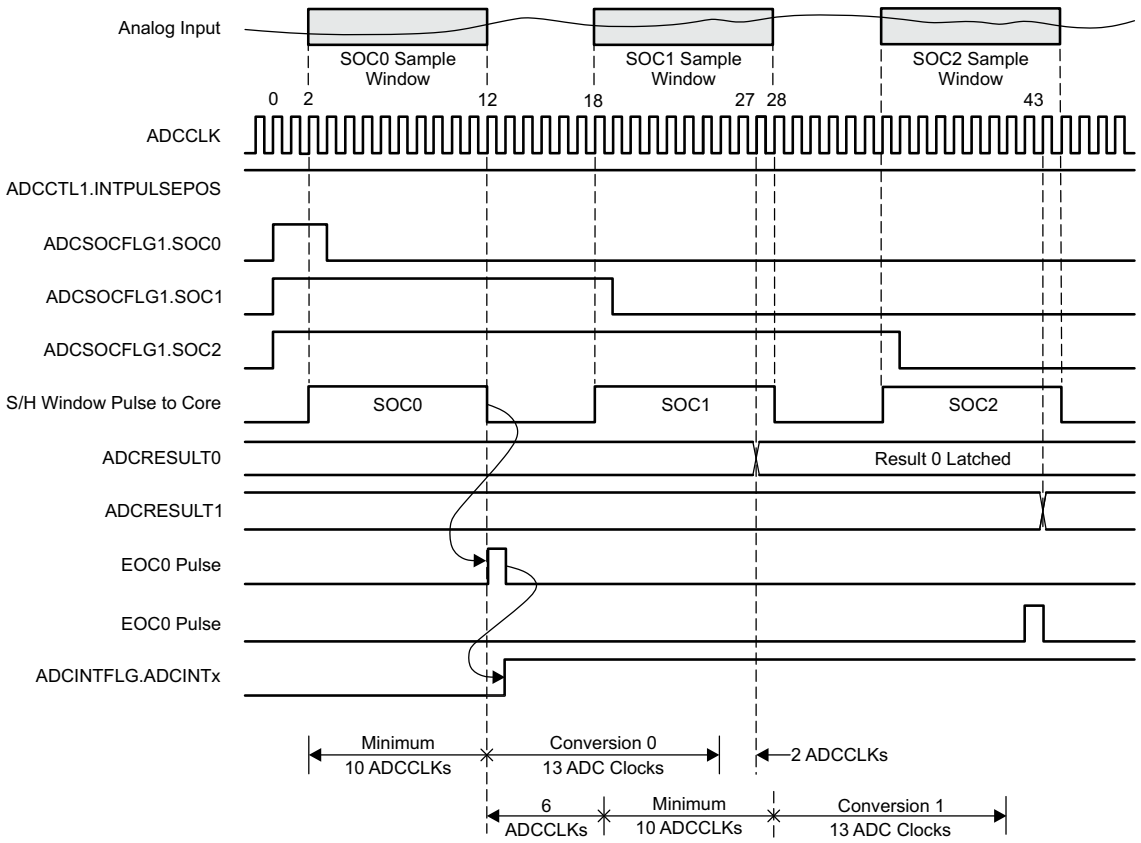


Figure 6-21. Timing Example for Sequential Mode / Early Interrupt Pulse

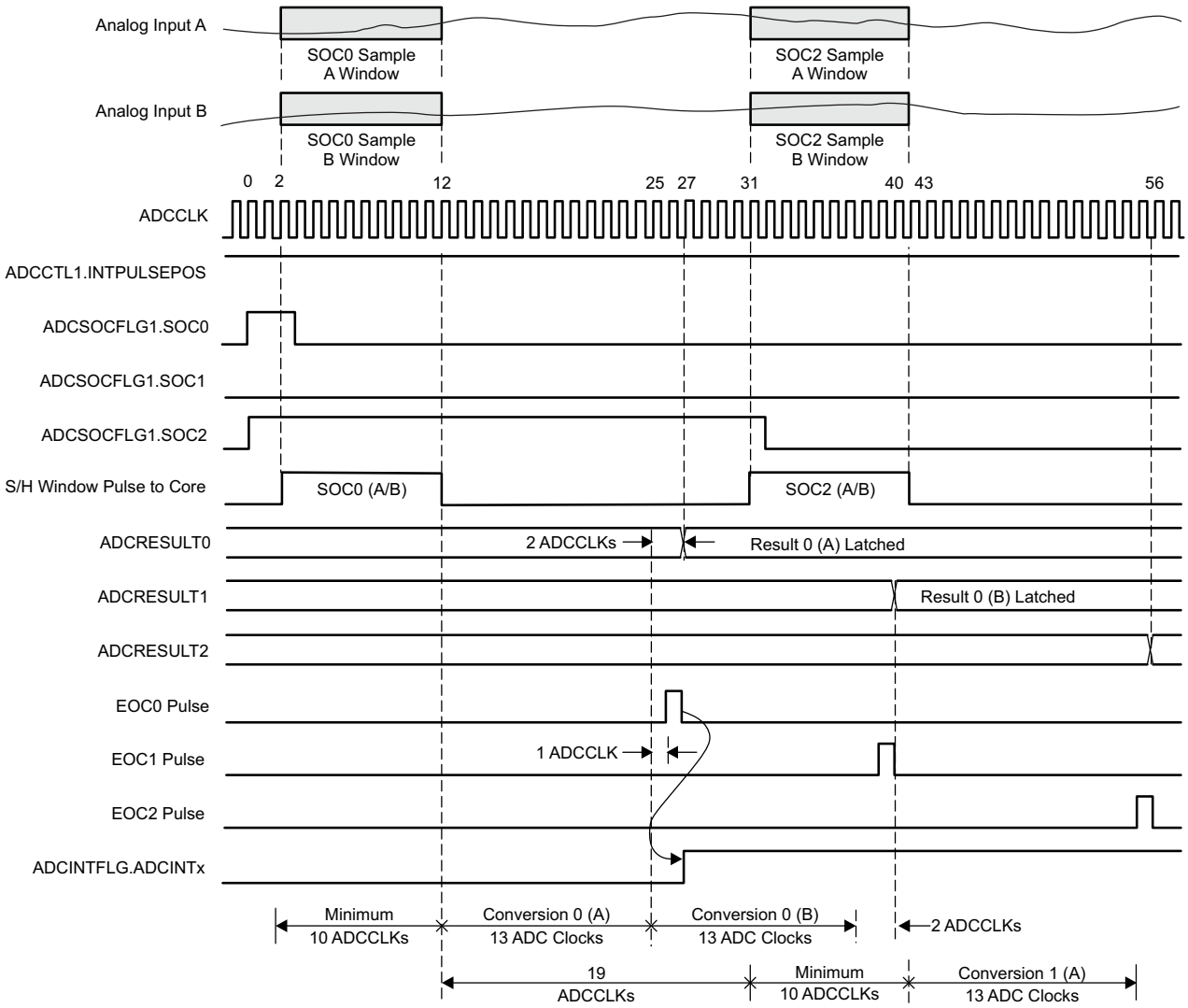


Figure 6-22. Timing Example for Simultaneous Mode / Late Interrupt Pulse

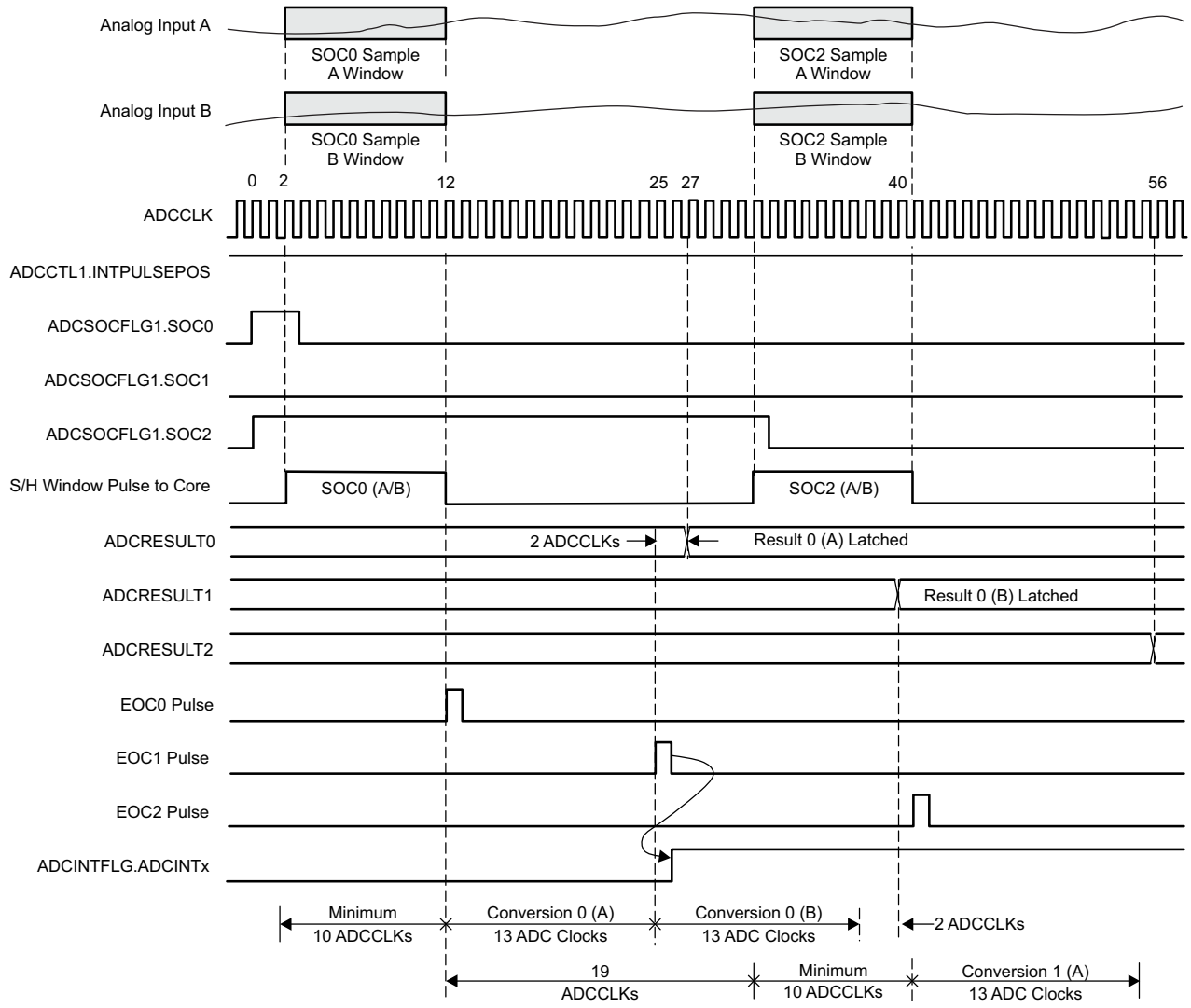


Figure 6-23. Timing Example for Simultaneous Mode / Early Interrupt Pulse

6.9.2.2 Analog Front End

6.9.2.2.1 AFE Device-Specific Information

The AFE contains up to seven comparators with up to three integrated DACs, one VREFOUT-buffered DAC, up to four PGAs, and up to four digital filters. Figure 6-24 and Figure 6-25 show the AFE.

The comparator output signal filtering is achieved using the Digital Filter present on selective input line and qualifies the output of the COMP/DAC subsystem (see Figure 6-27). The filtered or unfiltered output of the COMP/DAC subsystem can be configured to be an input to the Digital Compare submodule of the ePWM peripheral. **Note:** The Analog inputs are brought in through the AFE subsystem rather than through an AIO Mux, which is not present.

The ADCINSWITCH register is used to control ADC inputs dynamically and the setting of this register is separate from the AFE and Digital Filter initialization.

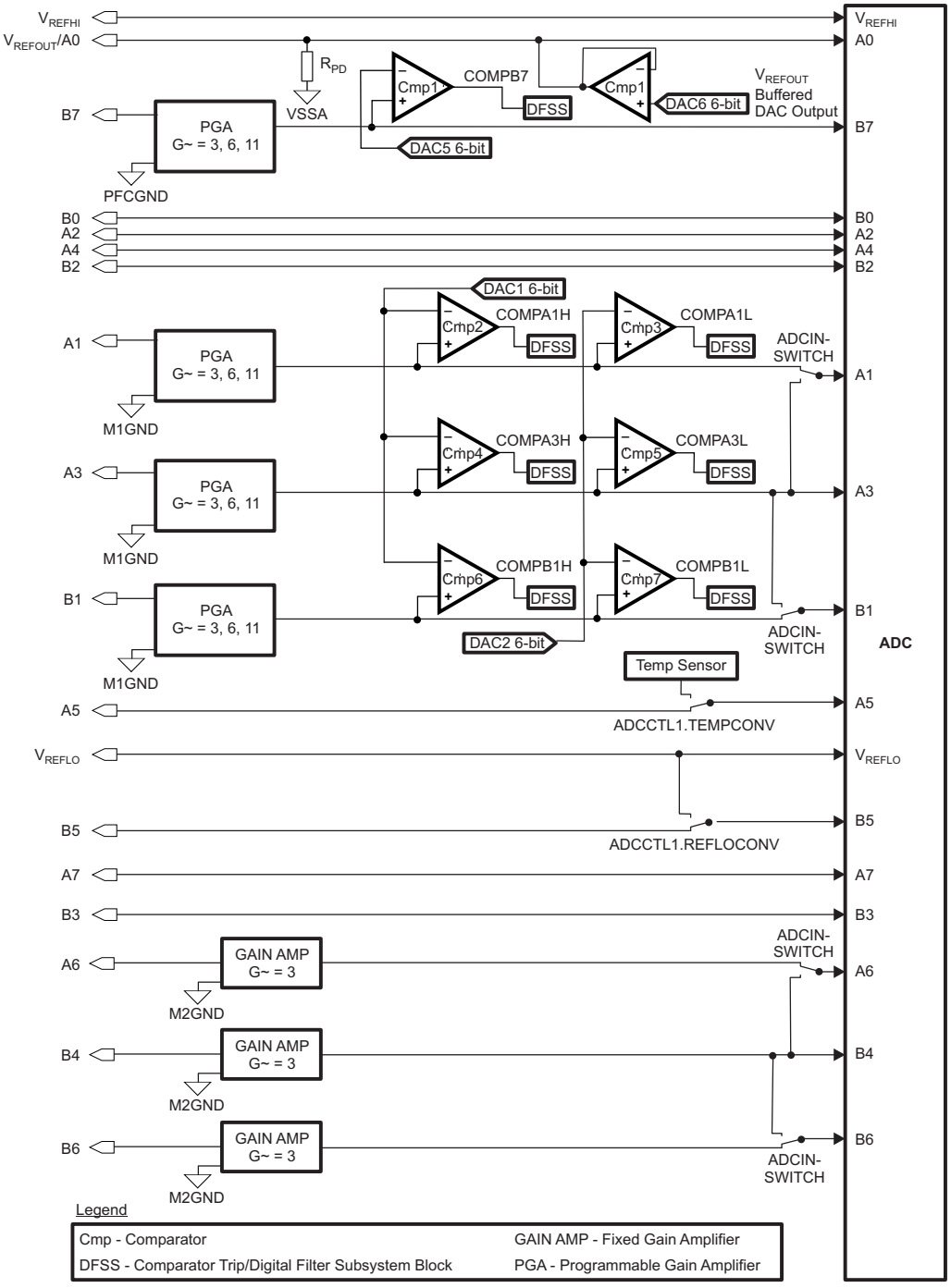


Figure 6-24. 28055, 28054, 28053, 28052, and 28051 Analog Front End

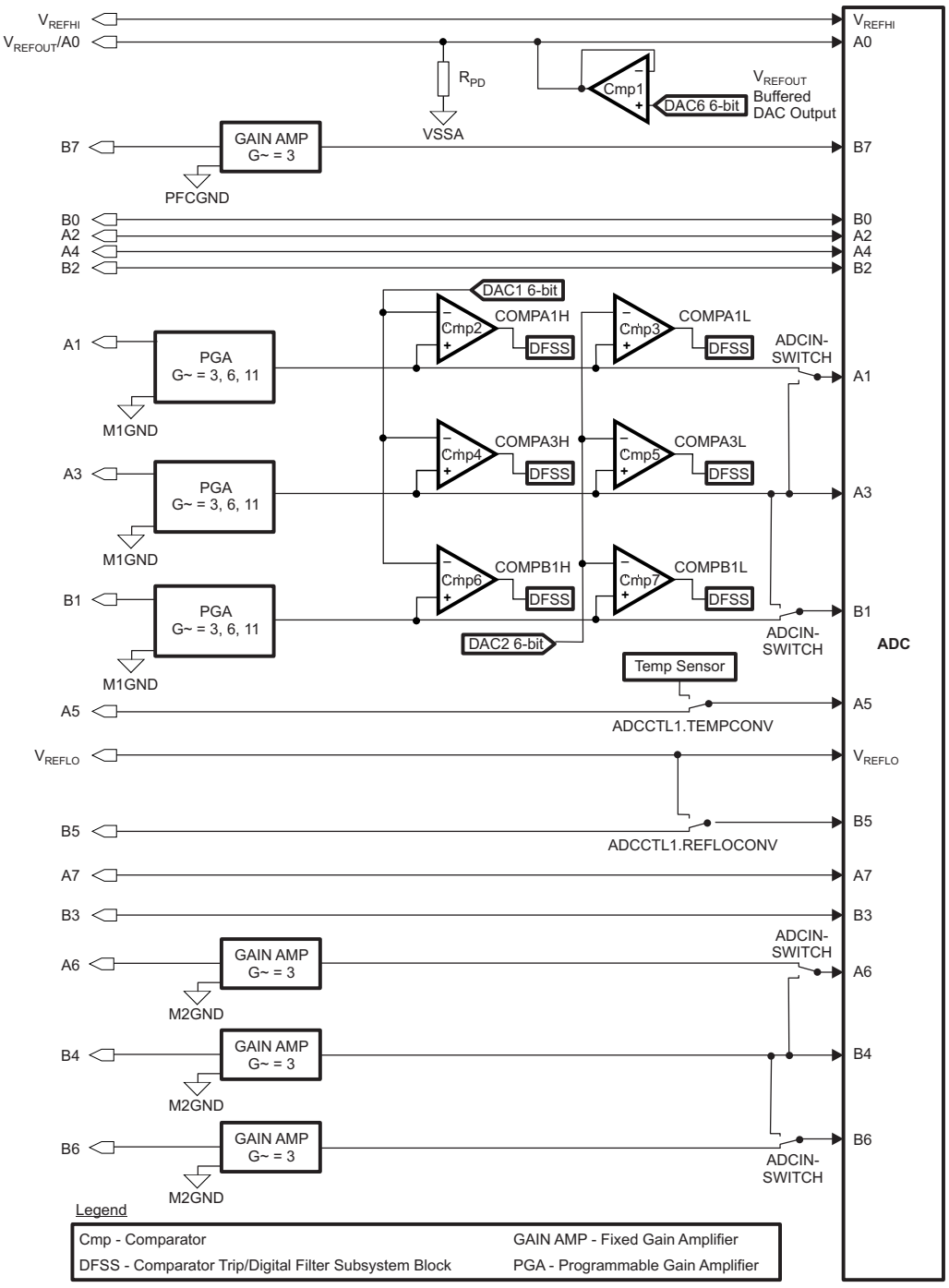


Figure 6-25. 28050 Analog Front End

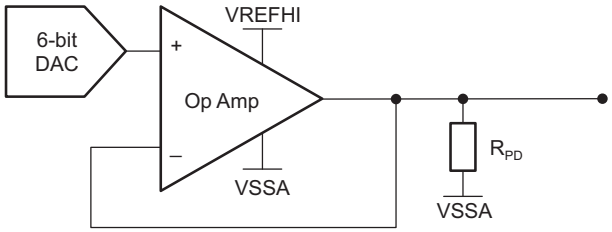


Figure 6-26. V_{REFOUT}

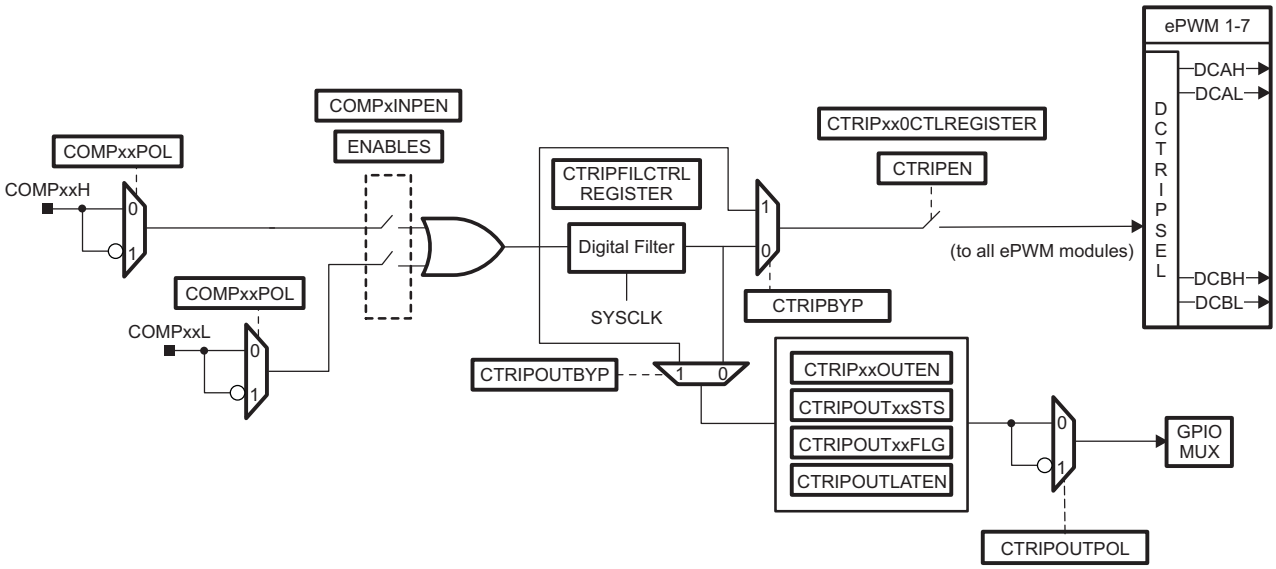


Figure 6-27. Comparator Trip/Digital Filter Subsystem

6.9.2.2.2 AFE Register Descriptions

Table 6-38. DAC Control Registers

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
DAC1CTL	0x6400	1	Yes	DAC1 Control Register
DAC2CTL	0x6401	1	Yes	DAC2 Control Register
DAC5CTL	0x6404	1	Yes	DAC5 Control Register
VREFOUTCTL	0x6405	1	Yes	VREFOUT DAC Control Register

Table 6-39. DAC, PGA, Comparator, and Filter Enable Registers

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
DACEN	0x6410	1	Yes	DAC Enables Register
VREFOUTEN	0x6411	1	Yes	VREFOUT Enable Register
PGAEN	0x6412	1	Yes	Programmable Gain Amplifier Enable Register
COMPEN	0x6413	1	Yes	Comparator Enable Register
AMPM1_GAIN	0x6414	1	Yes	Motor Unit 1 PGA Gain Controls Register
AMP_PFC_GAIN	0x6416	1	Yes	PFC PGA Gain Controls Register

Table 6-40. SWITCH Registers

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCINSWITCH	0x6421	1	Yes	ADC Input-Select Switch Control Register
Reserved	0x6422 – 0x6428	7	Yes	Reserved
COMPHYSTCTL	0x6429	1	Yes	Comparator Hysteresis Control Register

Table 6-41. Digital Filter and Comparator Control Registers

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
CTRIPA1ICTL	0x6430	1	Yes	CTRIPA1 Filter Input and Function Control Register
CTRIPA1FILCTL	0x6431	1	Yes	CTRIPA1 Filter Parameters Register
CTRIPA1FILCLKCTL	0x6432	1	Yes	CTRIPA1 Filter Sample Clock Control Register
Reserved	0x6433	1	Yes	Reserved
CTRIPA3ICTL	0x6434	1	Yes	CTRIPA3 Filter Input and Function Control Register
CTRIPA3FILCTL	0x6435	1	Yes	CTRIPA3 Filter Parameters Register
CTRIPA3FILCLKCTL	0x6436	1	Yes	CTRIPA3 Filter Sample Clock Control Register
Reserved	0x6437	1	Yes	Reserved
CTRIPB1ICTL	0x6438	1	Yes	CTRIPB1 Filter Input and Function Control Register
CTRIPB1FILCTL	0x6439	1	Yes	CTRIPB1 Filter Parameters Register
CTRIPB1FILCLKCTL	0x643A	1	Yes	CTRIPB1 Filter Sample Clock Control Register
Reserved	0x643B	1	Yes	Reserved
Reserved	0x643C	1	Yes	Reserved
CTRIPM1OCTL	0x643D	1	Yes	CTRIPM1 CTRIP Filter Output Control Register
CTRIPM1STS	0x643E	1	Yes	CTRIPM1 CTRIPxx Outputs Status Register
CTRIPM1FLGCLR	0x643F	1	Yes	CTRIPM1 CTRIPxx Flag Clear Register
Reserved	0x6440 – 0x645F	16	Yes	Reserved
Reserved	0x6460 – 0x646F	16	Yes	Reserved

Table 6-41. Digital Filter and Comparator Control Registers (continued)

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
CTRIPB7ICTL	0x6470	1	Yes	CTRIPB7 Filter Input and Function Control Register
CTRIPB7FILCTL	0x6471	1	Yes	CTRIPB7 Filter Parameters Register
CTRIPB7FILCLKCTL	0x6472	1	Yes	CTRIPB7 Filter Sample Clock Control Register
Reserved	0x6473 – 0x647B	9	Yes	Reserved
Reserved	0x647C	1	Yes	Reserved
CTRIPPFCOCTL	0x647D	1	Yes	CTRIPPFC CTRIPxx Outputs Status Register
CTRIPPFCSTS	0x647E	1	Yes	CTRIPPFC CTRIPxx Flag Clear Register
CTRIPPFCFLGCLR	0x647F	1	Yes	CTRIPPFC COMP Test Control Register

Table 6-42. LOCK Registers

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
LOCKCTRIP	0x64F0	1	Yes	Lock Register for CTRIP Filters Register
Reserved	0x64F1	1	Yes	Reserved
LOCKDAC	0x64F2	1	Yes	Lock Register for DACs Register
Reserved	0x64F3	1	Yes	Reserved
LOCKAMPCOMP	0x64F4	1	Yes	Lock Register for Amplifiers and Comparators Register
Reserved	0x64F5	1	Yes	Reserved
LOCKSWITCH	0x64F6	1	Yes	Lock Register for Switches Register

6.9.2.2.3 PGA Electrical Data/Timing

Table 6-43. Op-Amp Linear Output and ADC Sampling Time Across Gain Settings

INTERNAL RESISTOR RATIO	EQUIVALENT GAIN FROM INPUT TO OUTPUT	LINEAR OUTPUT RANGE OF OP-AMP	MINIMUM ADC SAMPLING TIME TO ACHIEVE SETTLING ACCURACY
10	11	0.6 V to V_{DDA} – 0.6 V	384 ns (ACQPS = 23)
5	6	0.6 V to V_{DDA} – 0.6 V	384 ns (ACQPS = 23)
2	3	0.6 V to V_{DDA} – 0.6 V	384 ns (ACQPS = 23)

Table 6-44. PGA Gain Stage: DC Accuracy Across Gain Settings

INTERNAL RESISTOR RATIO	EQUIVALENT GAIN FROM INPUT TO OUTPUT	COMPENSATED GAIN-ERROR ACROSS TEMPERATURE AND SUPPLY VARIATIONS	COMPENSATED INPUT OFFSET-ERROR ACROSS TEMPERATURE AND SUPPLY VARIATIONS IN mV
10	11	< ±2.5%	< ±8 mV
5	6	< ±1.5%	< ±8 mV
2	3	< ±1.0%	< ±8 mV

6.9.2.2.4 Comparator Block Electrical Data/Timing

Table 6-45. Electrical Characteristics of the Comparator/DAC

PARAMETER	MIN	TYP	MAX	UNITS
Comparator				
Comparator Input Range		V_{SSA} – V_{DDA}		V
Comparator response time to PWM Trip Zone (Async)		65		ns
Comparator large step response time to PWM Trip Zone (Async)		95		ns
DAC				
DAC Output Range		V_{DDA} / 2^6 – V_{DDA}		V
DAC resolution		6		bits
DAC Gain		–1.5		%
DAC Offset		10		mV
Monotonic		Yes		
INL		0.2		LSB

6.9.2.2.5 V_{REFOUT} Buffered DAC Electrical Data

Table 6-46. Electrical Characteristics of V_{REFOUT} Buffered DAC

PARAMETER	MIN	TYP	MAX	UNITS
V_{REFOUT} Programmable Range	6		56	LSB
V_{REFOUT} resolution		6		bits
V_{REFOUT} Gain		–1.5		%
V_{REFOUT} Offset		10		mV
Monotonic		Yes		
INL		±0.2		LSB
Load	3			kΩ
			100	pF
R_{PD}		20		kΩ

6.9.3 Detailed Descriptions

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs one-half LSB before the first code transition. The full-scale point is defined as level one-half LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

Zero Offset

Zero error is the difference between the ideal input voltage and the actual input voltage that just causes a transition from an output code of zero to an output code of one.

Gain Error

The first code transition should occur at an analog value one-half LSB above negative full scale. The last transition should occur at an analog value one and one-half LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion

Signal-to-noise ratio + distortion (SINAD) is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, $N = \frac{(SINAD - 1.76)}{6.02}$ it is possible to get a measure of performance expressed as N, the effective number of bits (ENOB). Thus, the ENOB for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of the first nine harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range

Spurious free dynamic range (SFDR) is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

6.9.4 Serial Peripheral Interface

6.9.4.1 SPI Device-Specific Information

The device includes the four-pin SPI module. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO if the SPI module is not used.

- Two operational modes: master and slave

  Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \qquad \text{when SPIBRR} = 3 \text{ to } 127$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \qquad \text{when SPIBRR} = 0, 1, 2$$

- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

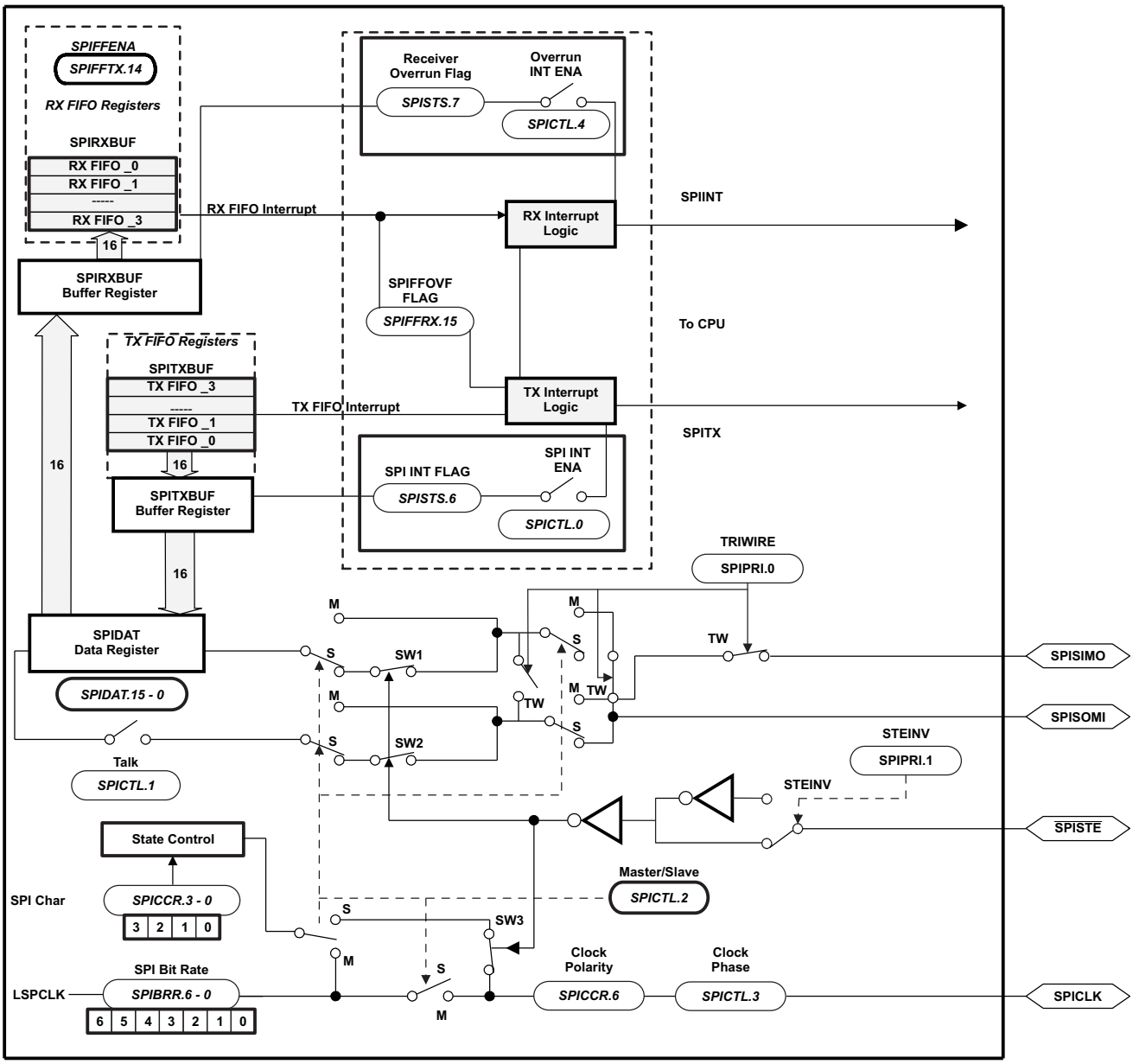
NOTE

All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 4-level transmit/receive FIFO
- Delayed transmit control
- Bi-directional 3-wire SPI mode support
- Audio data receive support via $\overline{\text{SPISTE}}$ inversion

Figure 6-28 is a block diagram of the SPI in slave mode.



A. $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

Figure 6-28. SPI Module Block Diagram (Slave Mode)

6.9.4.2 SPI Register Descriptions

The SPI port operation is configured and controlled by the registers listed in Table 6-47.

Table 6-47. SPI-A Registers

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION(1)
SPICCR	0x7040	1	No	SPI-A Configuration Control Register
SPICTL	0x7041	1	No	SPI-A Operation Control Register
SPISTS	0x7042	1	No	SPI-A Status Register
SPIBRR	0x7044	1	No	SPI-A Baud Rate Register
SPIRXEMU	0x7046	1	No	SPI-A Receive Emulation Buffer Register
SPIRXBUF	0x7047	1	No	SPI-A Serial Input Buffer Register
SPITXBUF	0x7048	1	No	SPI-A Serial Output Buffer Register
SPIDAT	0x7049	1	No	SPI-A Serial Data Register
SPIFFTX	0x704A	1	No	SPI-A FIFO Transmit Register
SPIFFRX	0x704B	1	No	SPI-A FIFO Receive Register
SPIFFCT	0x704C	1	No	SPI-A FIFO Control Register
SPIPRI	0x704F	1	No	SPI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

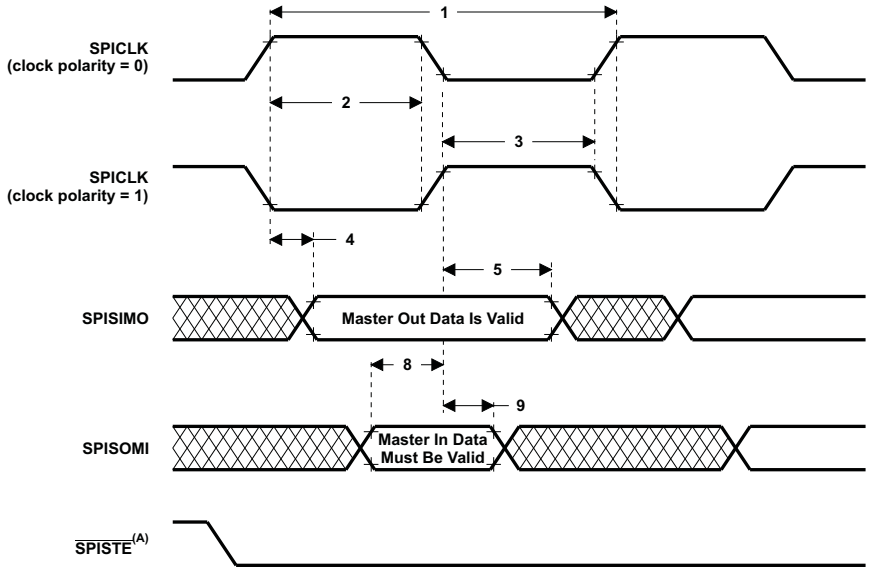
6.9.4.3 SPI Master Mode Electrical Data/Timing

Table 6-48 lists the master mode timing (clock phase = 0) and Table 6-49 lists the timing (clock phase = 1). Figure 6-29 and Figure 6-30 show the timing waveforms.

Table 6-48. SPI Master Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$	$0.5_{tc(SPC)M}$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5_{tc(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)		10		10	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)		10		10	
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$		
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	26		26		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	26		26		
9	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.25t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$		ns
	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.25t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$		

(1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR +1)
(3) $t_{c(LCO)}$ = LSPCLK cycle time
(4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 15-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
(5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).



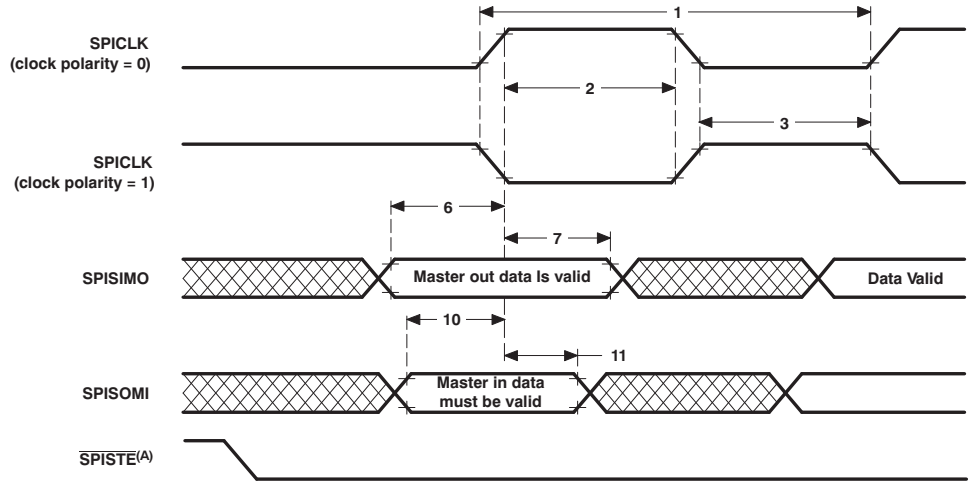
A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit, except that $\overline{\text{SPISTE}}$ stays active between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-29. SPI Master Mode External Timing (Clock Phase = 0)

Table 6-49. SPI Master Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)(5)

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} - 0.5t_{c\ (LCO)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$	ns
	$t_{w(SPCL))M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} - 0.5t_{c\ (LCO)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LCO}$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M}$	$0.5_{tc(SPC)M} + 0.5t_{c(LCO)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$	
6	$t_{su(SIMO-SPCH)M}$	Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		ns
	$t_{su(SIMO-SPCL)M}$	Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		
7	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		
10	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	26		26		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	26		26		
11	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$0.25t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 10$		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$0.25_{tc(SPC)M} - 10$		$0.5_{tc(SPC)M} - 10$		

(1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 15-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit, except that $\overline{\text{SPISTE}}$ stays active between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-30. SPI Master Mode External Timing (Clock Phase = 1)

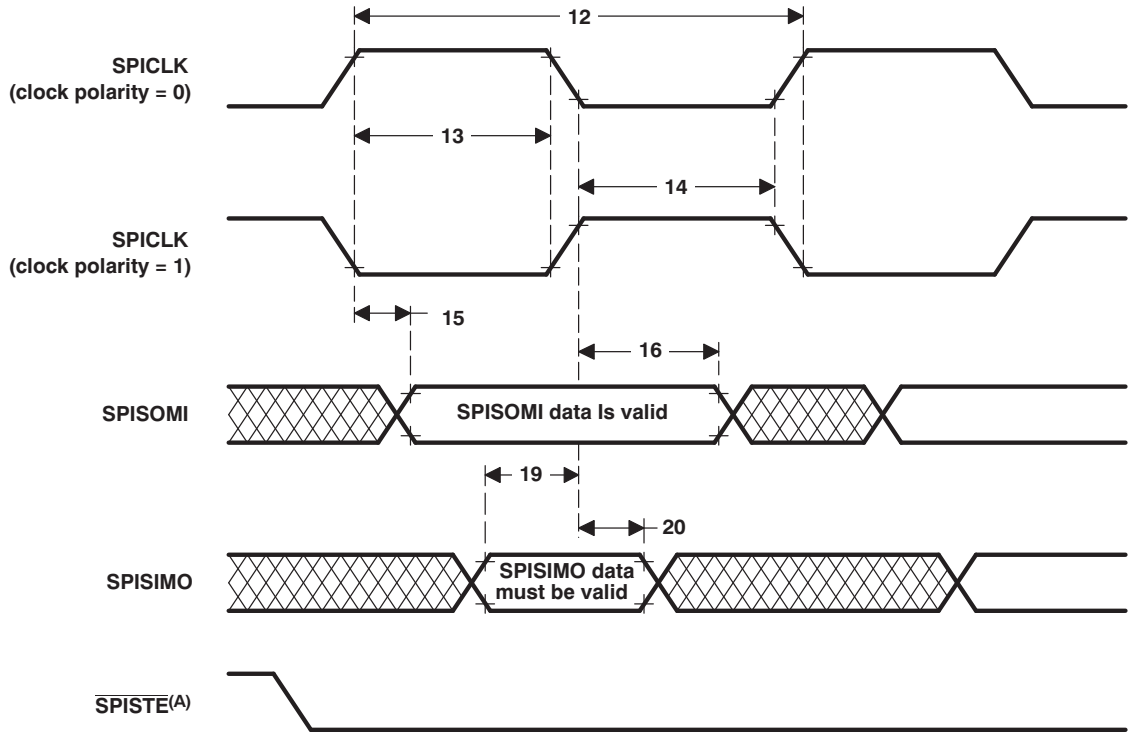
6.9.4.4 SPI Slave Mode Electrical Data/Timing

Table 6-50 lists the slave mode external timing (clock phase = 0) and Table 6-51 (clock phase = 1). Figure 6-31 and Figure 6-32 show the timing waveforms.

Table 6-50. SPI Slave Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(LCO)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	
15	$t_{d(SPCH-SOMI)S}$	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)		21	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPICLK low to SPISOMI valid (clock polarity = 1)		21	
16	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.75t_{c(SPC)S}$		
19	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	26		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	26		
20	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$		ns
	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$		

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 15-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



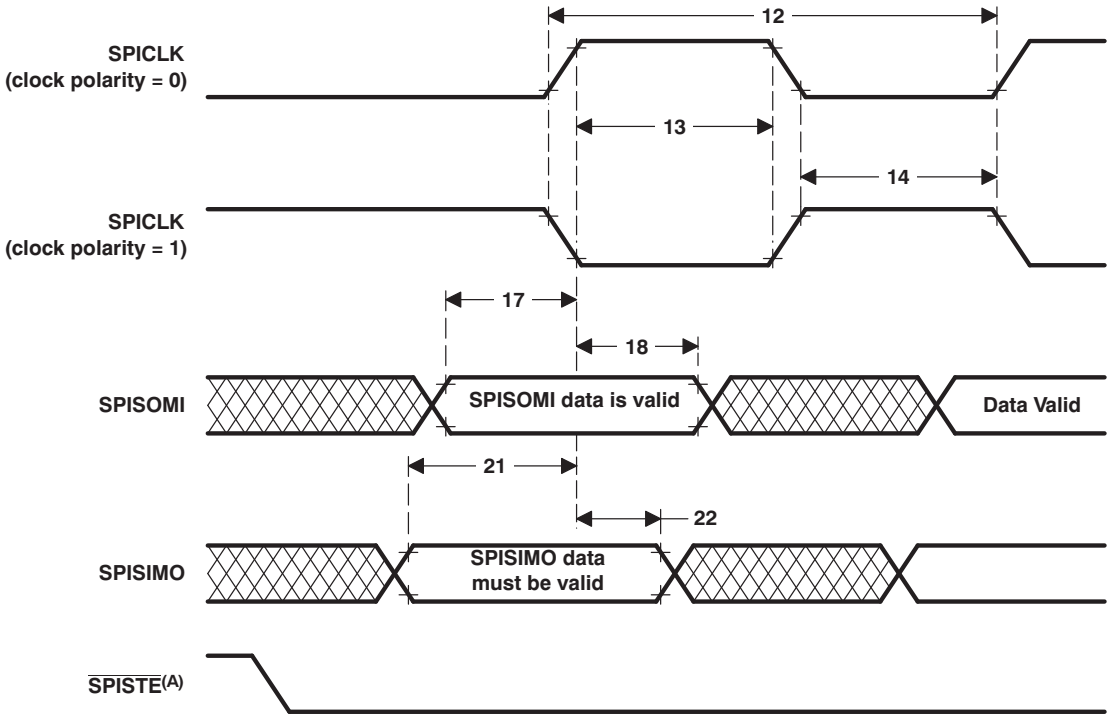
A. In the slave mode, the $\overline{SPISTE}$ signal should be asserted low at least $0.5t_{c(SPC)}$ (minimum) before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-31. SPI Slave Mode External Timing (Clock Phase = 0)

Table 6-51. SPI Slave Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_{c(LCO)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)\ S}$	
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)\ S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$	$0.5t_{c(SPC)S}$	
17	$t_{su(SOMI-SPCH)S}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$0.125t_{c(SPC)S}$		ns
	$t_{su(SOMI-SPCL)S}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$0.125t_{c(SPC)S}$		
18	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$0.75t_{c(SPC)\ S}$		
21	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	26		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	26		
22	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 10$		ns
	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 10$		

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 15-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



A. In the slave mode, the $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$ before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-32. SPI Slave Mode External Timing (Clock Phase = 1)

6.9.5 Serial Communications Interface

6.9.5.1 SCI Device-Specific Information

The 2805x devices include three SCI modules (SCI-A, SCI-B, SCI-C). Each SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

    NOTE: Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \qquad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \qquad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format

NOTE

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic
- 4-level transmit/receive FIFO

Figure 6-33 shows the SCI module block diagram.

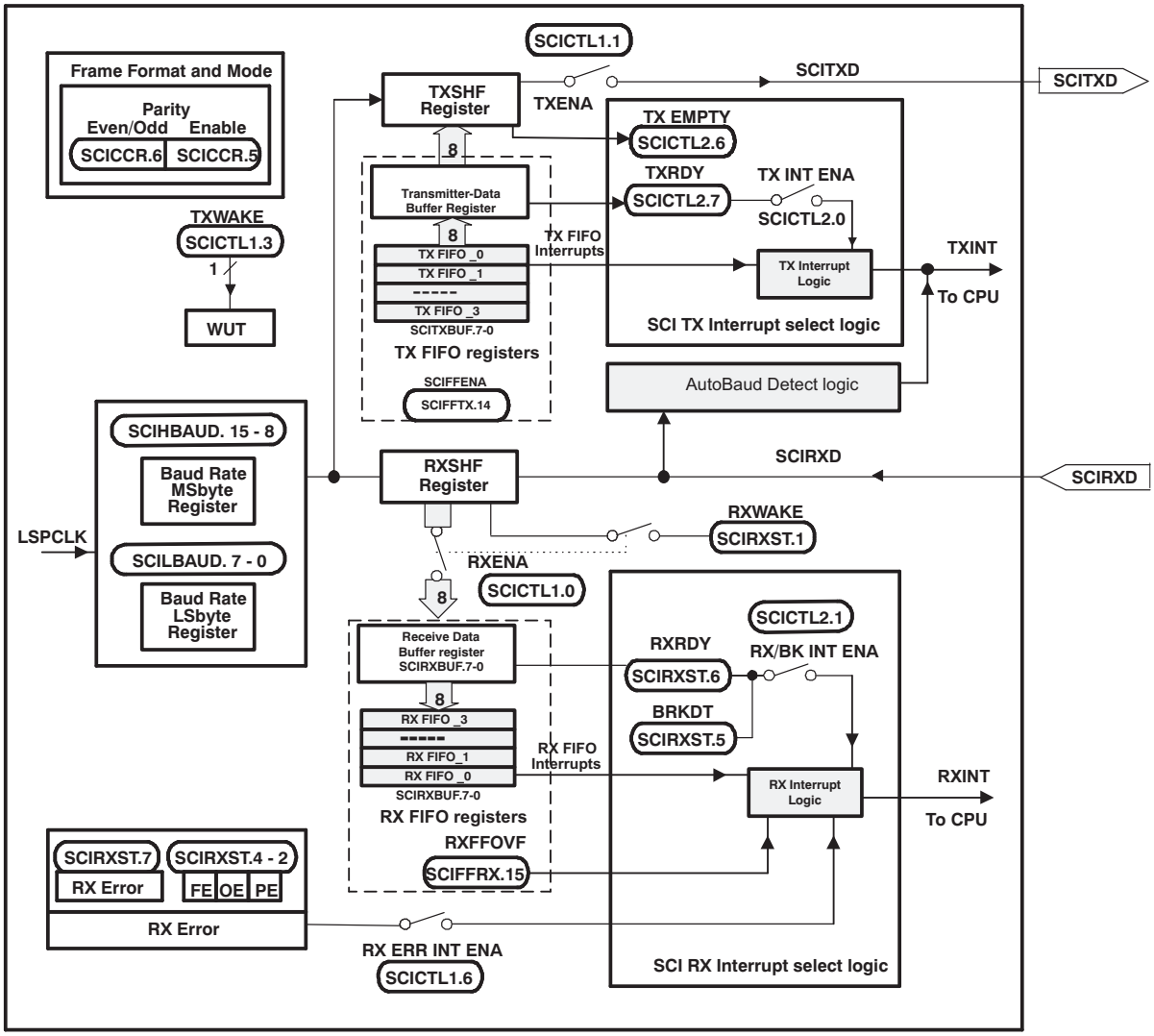


Figure 6-33. SCI Module Block Diagram

6.9.5.2 SCI Register Descriptions

The SCI port operation is configured and controlled by the registers listed in Table 6-52.

Table 6-52. SCI-A Registers(1)

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
SCICCRA	0x7050	1	No	SCI-A Communications Control Register
SCICTL1A	0x7051	1	No	SCI-A Control Register 1
SCIHBAUDA	0x7052	1	No	SCI-A Baud Register, High Bits
SCILBAUDA	0x7053	1	No	SCI-A Baud Register, Low Bits
SCICTL2A	0x7054	1	No	SCI-A Control Register 2
SCIRXSTA	0x7055	1	No	SCI-A Receive Status Register
SCIRXEMUA	0x7056	1	No	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x7057	1	No	SCI-A Receive Data Buffer Register
SCITXBUFA	0x7059	1	No	SCI-A Transmit Data Buffer Register
SCIFFTXA(2)	0x705A	1	No	SCI-A FIFO Transmit Register
SCIFFRXA(2)	0x705B	1	No	SCI-A FIFO Receive Register
SCIFFCTA(2)	0x705C	1	No	SCI-A FIFO Control Register
SCIPRIA	0x705F	1	No	SCI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

6.9.6 Enhanced Controller Area Network

6.9.6.1 eCAN Device-Specific Information

The CAN module (eCAN-A) has the following features:

- Fully compliant with CAN protocol, version 2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit time stamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A "dummy" acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

NOTE

For a SYSCLKOUT of 60 MHz, the smallest bit rate possible is 4.6875 kbps.

The F2805x CAN has passed the conformance test per ISO/DIS 16845. Contact TI for test report and exceptions.

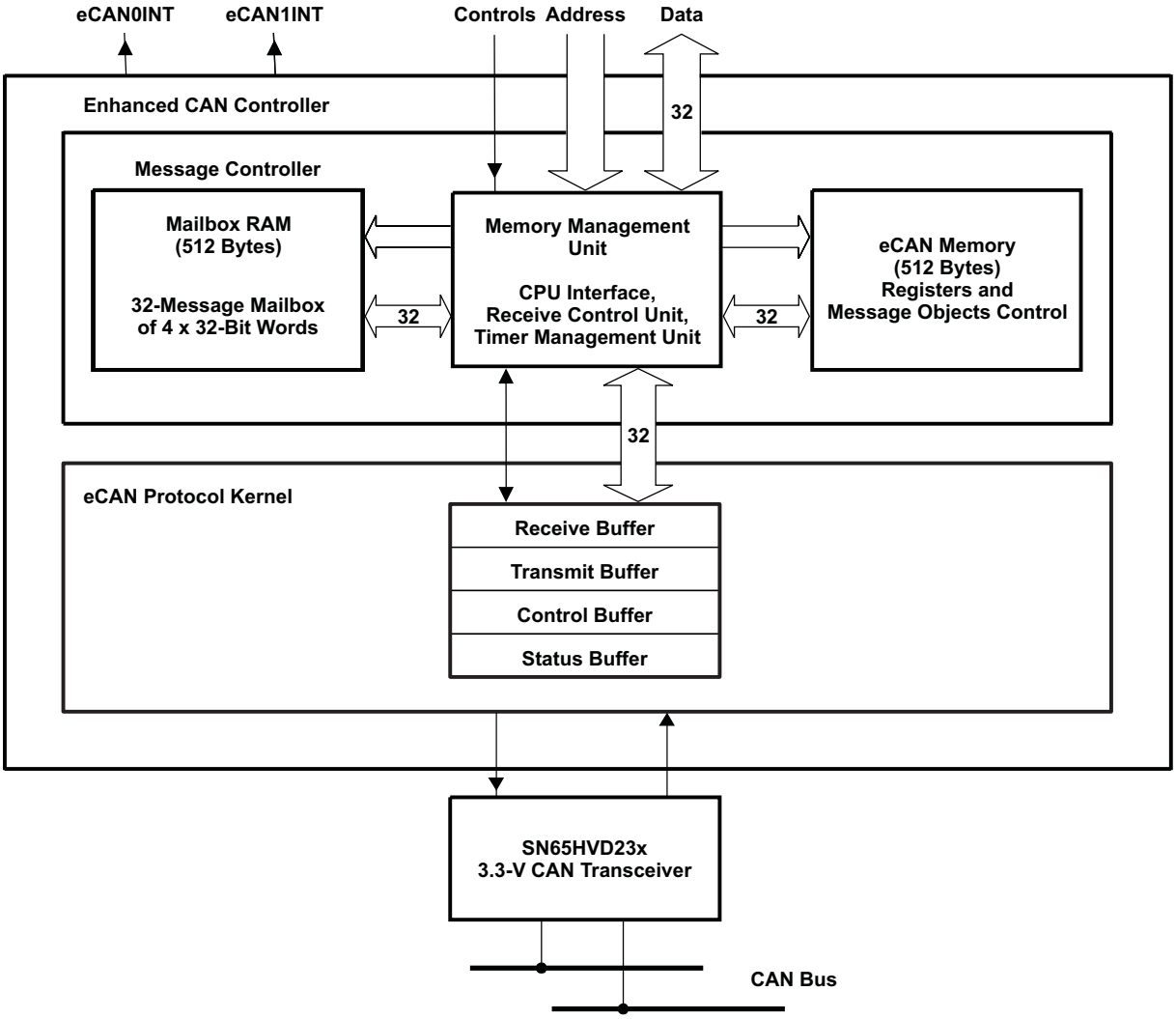


Figure 6-34. eCAN Block Diagram and Interface Circuit

Table 6-53. 3.3-V eCAN Transceivers

PART NUMBER	SUPPLY VOLTAGE	LOW-POWER MODE	SLOPE CONTROL	VREF	OTHER	T_A
SN65HVD230	3.3 V	Standby	Adjustable	Yes	–	–40°C to 85°C
SN65HVD230Q	3.3 V	Standby	Adjustable	Yes	–	–40°C to 125°C
SN65HVD231	3.3 V	Sleep	Adjustable	Yes	–	–40°C to 85°C
SN65HVD231Q	3.3 V	Sleep	Adjustable	Yes	–	–40°C to 125°C
SN65HVD232	3.3 V	None	None	None	–	–40°C to 85°C
SN65HVD232Q	3.3 V	None	None	None	–	–40°C to 125°C
SN65HVD233	3.3 V	Standby	Adjustable	None	Diagnostic Loopback	–40°C to 125°C
SN65HVD234	3.3 V	Standby and Sleep	Adjustable	None	–	–40°C to 125°C
SN65HVD235	3.3 V	Standby	Adjustable	None	Autobaud Loopback	–40°C to 125°C
ISO1050	3–5.5 V	None	None	None	Built-in Isolation Low Prop Delay Thermal Shutdown Failsafe Operation Dominant Time-Out	–55°C to 105°C

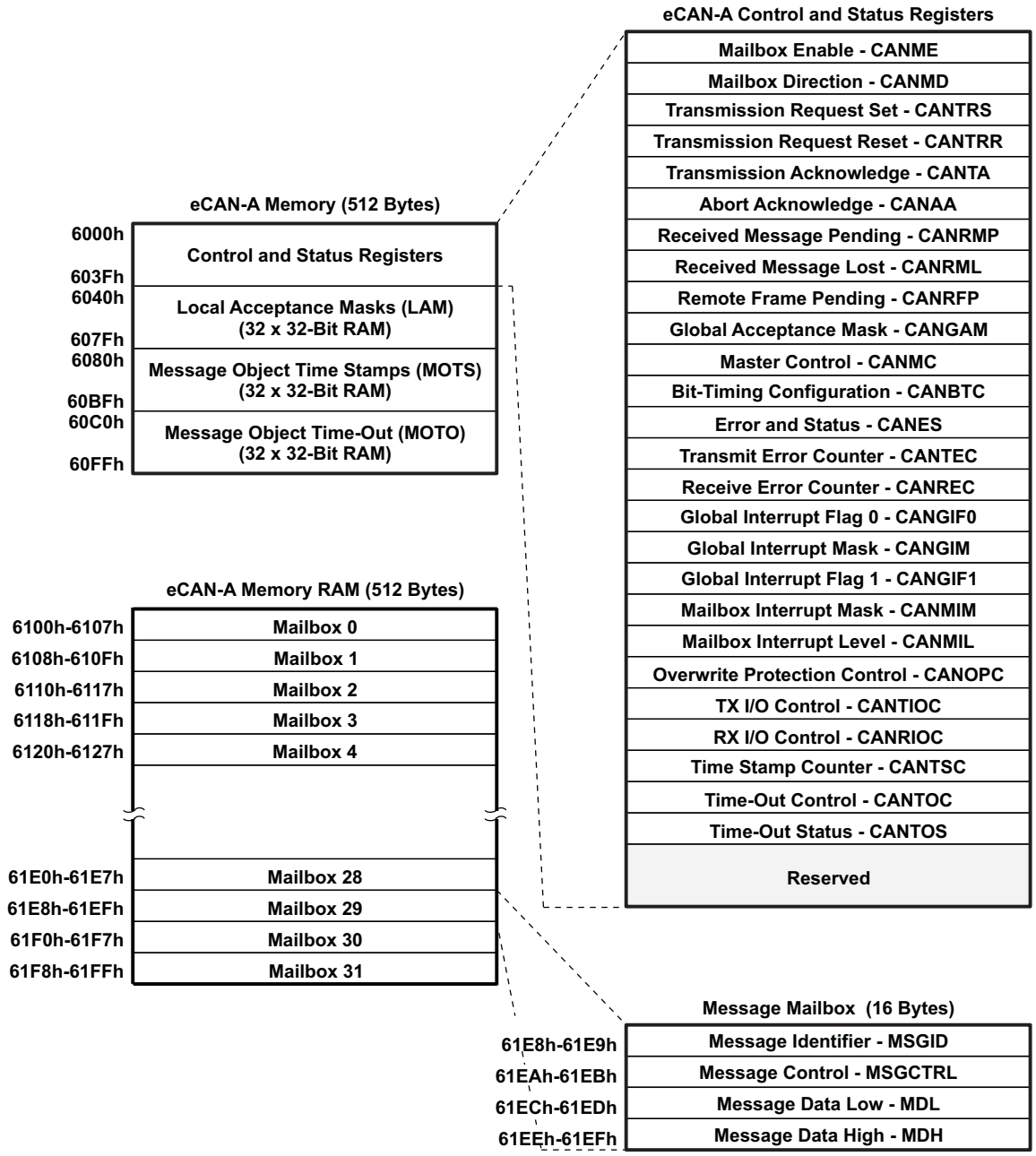


Figure 6-35. eCAN-A Memory Map

NOTE

If the eCAN module is not used in an application, the RAM available (LAM, MOTS, MOTO, and mailbox RAM) can be used as general-purpose RAM. The CAN module clock should be enabled if the eCAN RAM (LAM, MOTS, MOTO, and mailbox RAM) is used as general-purpose RAM.

6.9.6.2 eCAN Register Descriptions

The CAN registers listed in Table 6-54 are used by the CPU to configure and control the CAN controller and the message objects. eCAN control registers only support 32-bit read/write operations. Mailbox RAM can be accessed as 16 bits or 32 bits. 32-bit accesses are aligned to an even boundary.

Table 6-54. CAN Register Map(1)

REGISTER NAME	eCAN-A ADDRESS	SIZE (x32)	DESCRIPTION
CANME	0x6000	1	Mailbox enable
CANMD	0x6002	1	Mailbox direction
CANTRS	0x6004	1	Transmit request set
CANTRR	0x6006	1	Transmit request reset
CANTA	0x6008	1	Transmission acknowledge
CANAA	0x600A	1	Abort acknowledge
CANRMP	0x600C	1	Receive message pending
CANRML	0x600E	1	Receive message lost
CANRFP	0x6010	1	Remote frame pending
CANGAM	0x6012	1	Global acceptance mask
CANMC	0x6014	1	Master control
CANBTC	0x6016	1	Bit-timing configuration
CANES	0x6018	1	Error and status
CANTEC	0x601A	1	Transmit error counter
CANREC	0x601C	1	Receive error counter
CANGIF0	0x601E	1	Global interrupt flag 0
CANGIM	0x6020	1	Global interrupt mask
CANGIF1	0x6022	1	Global interrupt flag 1
CANMIM	0x6024	1	Mailbox interrupt mask
CANMIL	0x6026	1	Mailbox interrupt level
CANOPC	0x6028	1	Overwrite protection control
CANTIOC	0x602A	1	TX I/O control
CANRIOC	0x602C	1	RX I/O control
CANTSC	0x602E	1	Time stamp counter (Reserved in SCC mode)
CANTOC	0x6030	1	Time-out control (Reserved in SCC mode)
CANTOS	0x6032	1	Time-out status (Reserved in SCC mode)

(1) These registers are mapped to Peripheral Frame 1.

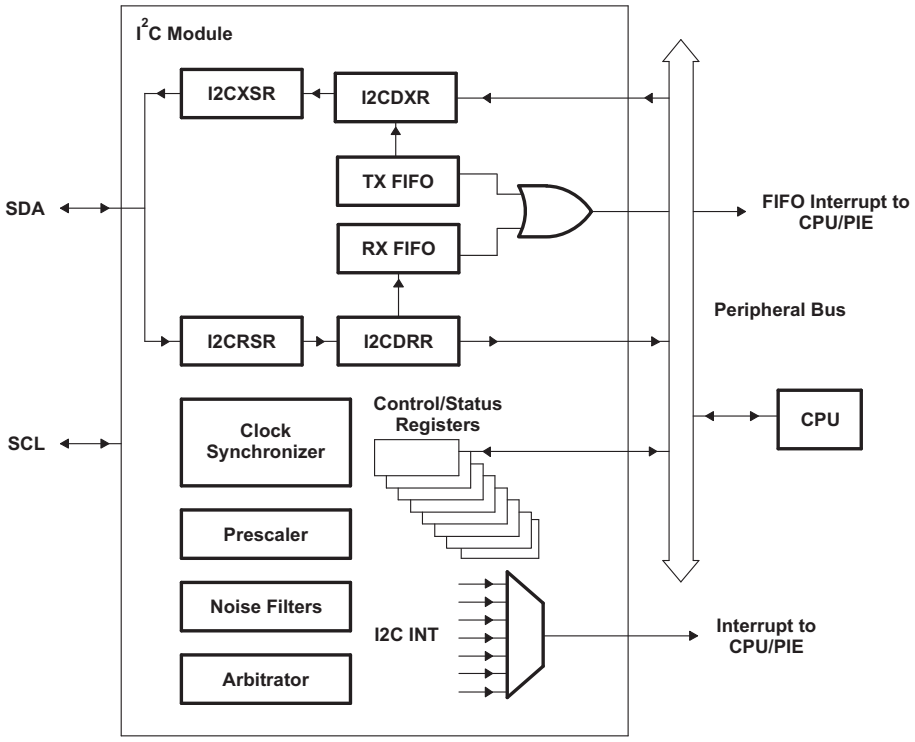
6.9.7 Inter-Integrated Circuit

6.9.7.1 I²C Device-Specific Information

The device contains one I²C serial port. Figure 6-36 shows how the I²C peripheral module interfaces within the device.

The I²C module has the following features:

- Compliance with the Philips Semiconductors I²C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (I²C Fast-mode rate)
- One 4-word receive FIFO and one 4-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode



A. The I²C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I²C port are also at the SYSCLKOUT rate.

B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I²C port for low power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 6-36. I²C Peripheral Module Interfaces

6.9.7.2 I²C Register Descriptions

The registers in Table 6-55 configure and control the I²C port operation.

Table 6-55. I2C-A Registers

NAME	ADDRESS	EALLOW PROTECTED	DESCRIPTION
I2COAR	0x7900	No	I²C own address register
I2CIER	0x7901	No	I²C interrupt enable register
I2CSTR	0x7902	No	I²C status register
I2CCLKL	0x7903	No	I²C clock low-time divider register
I2CCLKH	0x7904	No	I²C clock high-time divider register
I2CCNT	0x7905	No	I²C data count register
I2CDRR	0x7906	No	I²C data receive register
I2CSAR	0x7907	No	I²C slave address register
I2CDXR	0x7908	No	I²C data transmit register
I2CMDR	0x7909	No	I²C mode register
I2CISRC	0x790A	No	I²C interrupt source register
I2CPSC	0x790C	No	I²C prescaler register
I2CFFTX	0x7920	No	I²C FIFO transmit register
I2CFFRX	0x7921	No	I²C FIFO receive register
I2CRSR	–	No	I²C receive shift register (not accessible to the CPU)
I2CXSR	–	No	I²C transmit shift register (not accessible to the CPU)

6.9.7.3 I²C Electrical Data/Timing

Table 6-56. I²C Timing

		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	I²C clock module frequency is between 7 MHz and 12 MHz and I²C prescaler and clock divider registers are configured appropriately		400	kHz
v_{il}	Low level input voltage			0.3 V_{DDIO}	V
V_{ih}	High level input voltage		0.7 V_{DDIO}		V
V_{hys}	Input hysteresis		0.05 V_{DDIO}		V
V_{ol}	Low level output voltage	3 mA sink current	0	0.4	V
t_{LOW}	Low period of SCL clock	I²C clock module frequency is between 7 MHz and 12 MHz and I²C prescaler and clock divider registers are configured appropriately	1.3		µs
t_{HIGH}	High period of SCL clock	I²C clock module frequency is between 7 MHz and 12 MHz and I²C prescaler and clock divider registers are configured appropriately	0.6		µs
I_I	Input current with an input voltage between 0.1 V_{DDIO} and 0.9 V_{DDIO} MAX		–10	10	µA

6.9.8 Enhanced Pulse Width Modulator

6.9.8.1 ePWM Device-Specific Information

The devices contain up to seven enhanced PWM modules (ePWM1–ePWM7). Figure 6-37 shows a block diagram of multiple ePWM modules. Figure 6-38 shows the signal interconnections with the ePWM. See the Enhanced Pulse Width Modulator (ePWM) Module chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5) for more details.

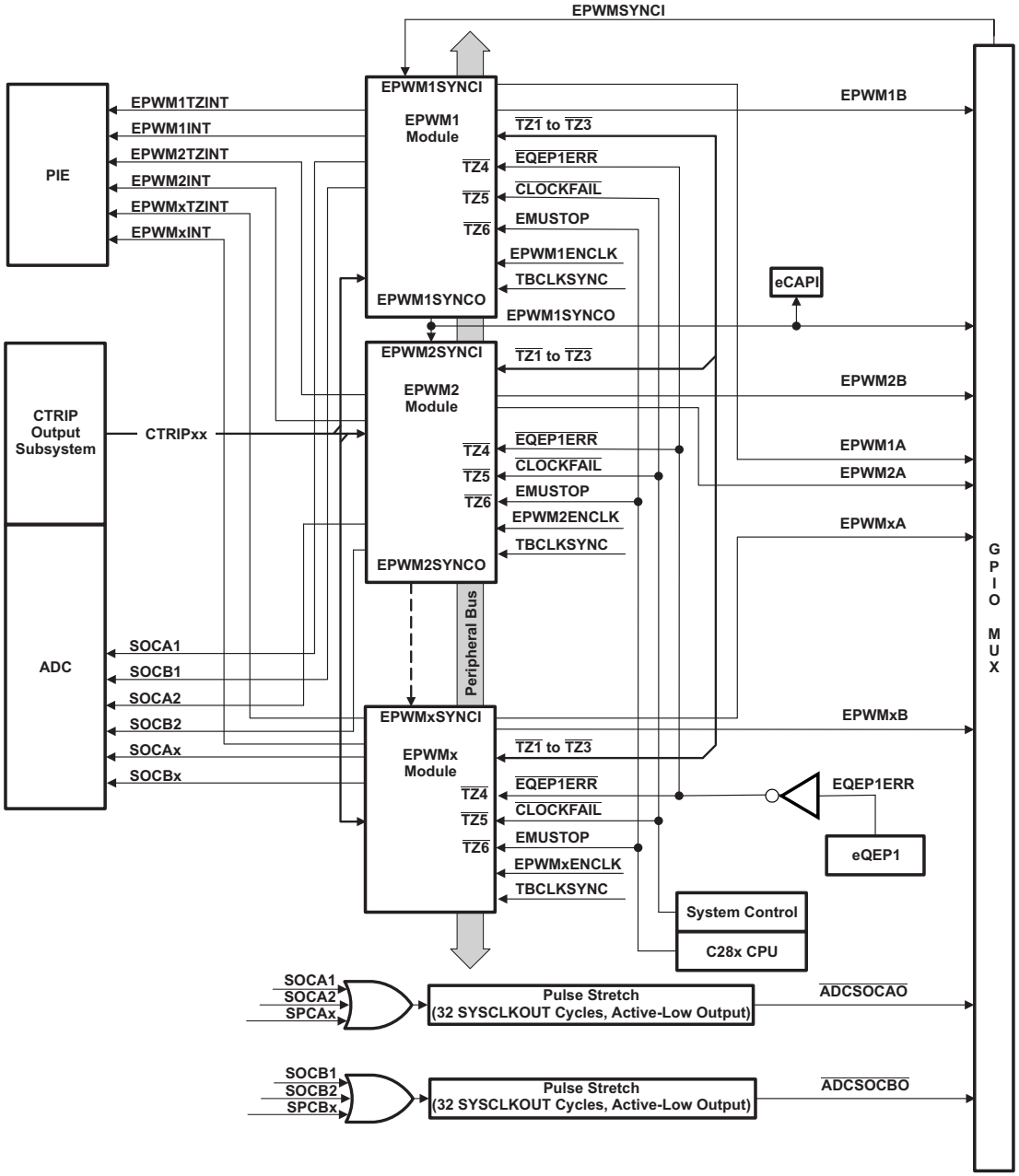
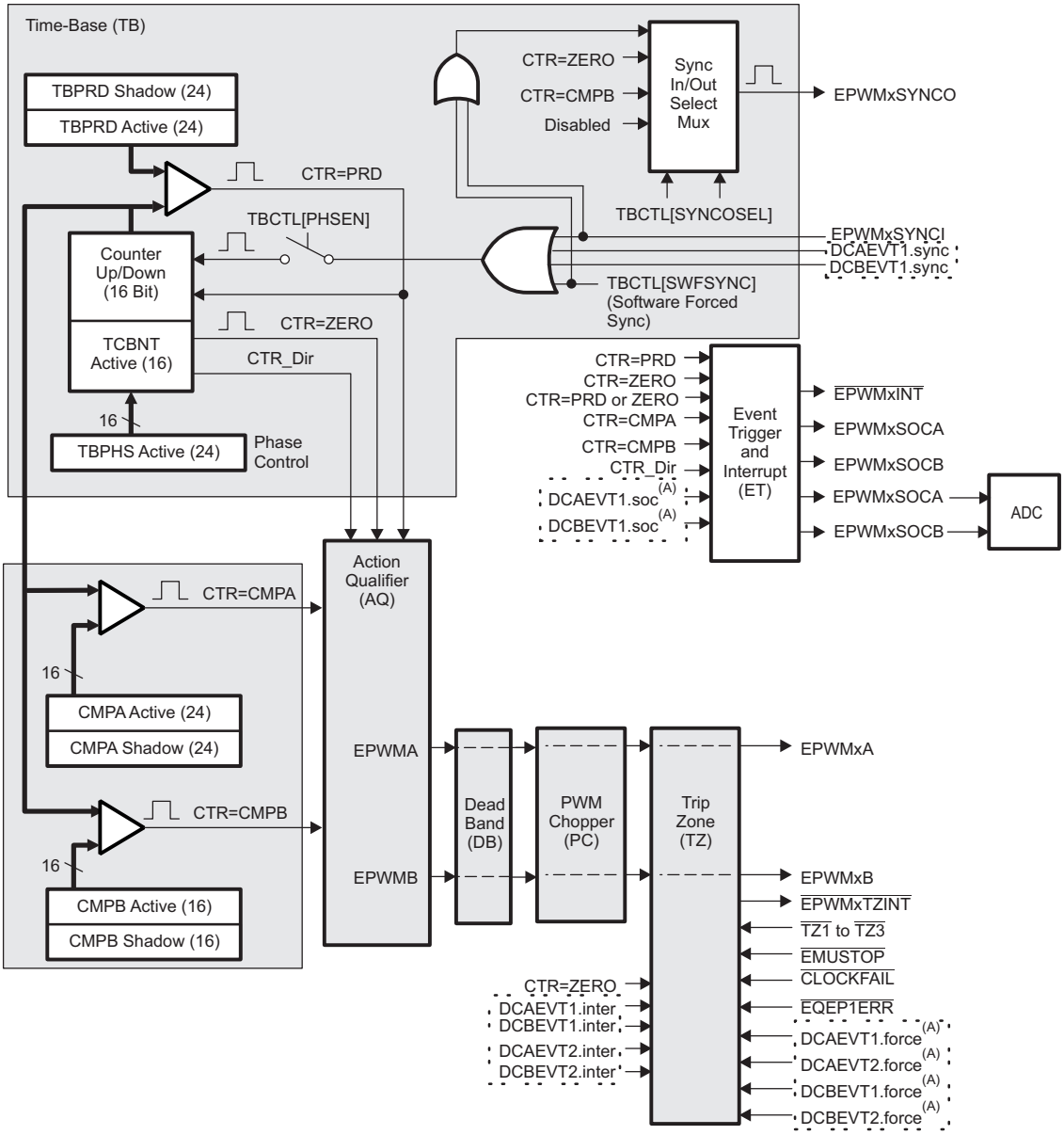


Figure 6-37. ePWM



A. These events are generated by the Type 1 ePWM digital compare (DC) submodule based on the levels of the COMPxOUT and $\overline{TZ}$ signals.

Figure 6-38. ePWM Sub-Modules Showing Critical Internal Signal Interconnections

6.9.8.2 ePWM Register Descriptions

Table 6-57 and Table 6-58 show the complete ePWM register set per module.

Table 6-57. ePWM1–ePWM4 Control and Status Registers

NAME	ePWM1	ePWM2	ePWM3	ePWM4	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6800	0x6840	0x6880	0x68C0	1 / 0	Time Base Control Register
TBSTS	0x6801	0x6841	0x6881	0x68C1	1 / 0	Time Base Status Register
Reserved	0x6802	0x6842	0x6882	0x68C2	1 / 0	Reserved
TBPHS	0x6803	0x6843	0x6883	0x68C3	1 / 0	Time Base Phase Register
TBCTR	0x6804	0x6844	0x6884	0x68C4	1 / 0	Time Base Counter Register
TBPRD	0x6805	0x6845	0x6885	0x68C5	1 / 1	Time Base Period Register Set
Reserved	0x6806	0x6846	0x6886	0x68C6	1 / 1	Reserved
CMPCTL	0x6807	0x6847	0x6887	0x68C7	1 / 0	Counter Compare Control Register
Reserved	0x6808	0x6848	0x6888	0x68C8	1 / 1	Reserved
CMPA	0x6809	0x6849	0x6889	0x68C9	1 / 1	Counter Compare A Register Set
CMPB	0x680A	0x684A	0x688A	0x68CA	1 / 1	Counter Compare B Register Set
AQCTLA	0x680B	0x684B	0x688B	0x68CB	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x680C	0x684C	0x688C	0x68CC	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x680D	0x684D	0x688D	0x68CD	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x680E	0x684E	0x688E	0x68CE	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x680F	0x684F	0x688F	0x68CF	1 / 1	Dead-Band Generator Control Register
DBRED	0x6810	0x6850	0x6890	0x68D0	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6811	0x6851	0x6891	0x68D1	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6812	0x6852	0x6892	0x68D2	1 / 0	Trip Zone Select Register(1)
TZDCSEL	0x6813	0x6853	0x6893	0x98D3	1 / 0	Trip Zone Digital Compare Register
TZCTL	0x6814	0x6854	0x6894	0x68D4	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6815	0x6855	0x6895	0x68D5	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6816	0x6856	0x6896	0x68D6	1 / 0	Trip Zone Flag Register (1)
TZCLR	0x6817	0x6857	0x6897	0x68D7	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6818	0x6858	0x6898	0x68D8	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6819	0x6859	0x6899	0x68D9	1 / 0	Event Trigger Selection Register
ETPS	0x681A	0x685A	0x689A	0x68DA	1 / 0	Event Trigger Prescale Register
ETFLG	0x681B	0x685B	0x689B	0x68DB	1 / 0	Event Trigger Flag Register
ETCLR	0x681C	0x685C	0x689C	0x68DC	1 / 0	Event Trigger Clear Register

(1) Registers that are EALLOW protected.

Table 6-57. ePWM1–ePWM4 Control and Status Registers (continued)

NAME	ePWM1	ePWM2	ePWM3	ePWM4	SIZE (x16) / #SHADOW	DESCRIPTION
ETFRC	0x681D	0x685D	0x689D	0x68DD	1 / 0	Event Trigger Force Register
PCCTL	0x681E	0x685E	0x689E	0x68DE	1 / 0	PWM Chopper Control Register
Reserved	0x6820	0x6860	0x68A0	0x68E0	1 / 0	Reserved
Reserved	0x6821	-	-	-	1 / 0	Reserved
Reserved	0x6826	-	-	-	1 / 0	Reserved
Reserved	0x6828	0x6868	0x68A8	0x68E8	1 / 0	Reserved
Reserved	0x682A	0x686A	0x68AA	0x68EA	1 / W(2)	Reserved
TBPRDM	0x682B	0x686B	0x68AB	0x68EB	1 / W(2)	Time Base Period Register Mirror
Reserved	0x682C	0x686C	0x68AC	0x68EC	1 / W(2)	Reserved
CMPAM	0x682D	0x686D	0x68AD	0x68ED	1 / W(2)	Compare A Register Mirror
DCTRIPSEL	0x6830	0x6870	0x68B0	0x68F0	1 / 0	Digital Compare Trip Select Register (1)
DCACTL	0x6831	0x6871	0x68B1	0x68F1	1 / 0	Digital Compare A Control Register(1)
DCBCTL	0x6832	0x6872	0x68B2	0x68F2	1 / 0	Digital Compare B Control Register(1)
DCFCTL	0x6833	0x6873	0x68B3	0x68F3	1 / 0	Digital Compare Filter Control Register(1)
DCCAPCT	0x6834	0x6874	0x68B4	0x68F4	1 / 0	Digital Compare Capture Control Register(3)
DCFOFFSET	0x6835	0x6875	0x68B5	0x68F5	1 / 1	Digital Compare Filter Offset Register
DCFOFFSETCNT	0x6836	0x6876	0x68B6	0x68F6	1 / 0	Digital Compare Filter Offset Counter Register
DCFWINDOW	0x6837	0x6877	0x68B7	0x68F7	1 / 0	Digital Compare Filter Window Register
DCFWINDOWCNT	0x6838	0x6878	0x68B8	0x68F8	1 / 0	Digital Compare Filter Window Counter Register
DCCAP	0x6839	0x6879	0x68B9	0x68F9	1 / 1	Digital Compare Counter Capture Register

(2) W = Write to shadow register
(3) Registers that are EALLOW protected.

Table 6-58. ePWM5–ePWM7 Control and Status Registers

NAME	ePWM5	ePWM6	ePWM7	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6900	0x6940	0x6980	1 / 0	Time Base Control Register
TBSTS	0x6901	0x6941	0x6981	1 / 0	Time Base Status Register
Reserved	0x6902	0x6942	0x6982	1 / 0	Reserved
TBPHS	0x6903	0x6943	0x6983	1 / 0	Time Base Phase Register
TBCTR	0x6904	0x6944	0x6984	1 / 0	Time Base Counter Register
TBPRD	0x6905	0x6945	0x6985	1 / 1	Time Base Period Register Set
Reserved	0x6906	0x6946	0x6986	1 / 1	Reserved
CMPCTL	0x6907	0x6947	0x6987	1 / 0	Counter Compare Control Register
Reserved	0x6908	0x6948	0x6988	1 / 1	Reserved
CMPA	0x6909	0x6949	0x6989	1 / 1	Counter Compare A Register Set
CMPB	0x690A	0x694A	0x698A	1 / 1	Counter Compare B Register Set
AQCTLA	0x690B	0x694B	0x698B	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x690C	0x694C	0x698C	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x690D	0x694D	0x698D	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x690E	0x694E	0x698E	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x690F	0x694F	0x698F	1 / 1	Dead-Band Generator Control Register
DBRED	0x6910	0x6950	0x6990	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6911	0x6951	0x6991	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6912	0x6952	0x6992	1 / 0	Trip Zone Select Register(1)
TZDCSEL	0x6913	0x6953	0x6993	1 / 0	Trip Zone Digital Compare Register
TZCTL	0x6914	0x6954	0x6994	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6915	0x6955	0x6995	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6916	0x6956	0x6996	1 / 0	Trip Zone Flag Register (1)
TZCLR	0x6917	0x6957	0x6997	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6918	0x6958	0x6998	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6919	0x6959	0x6999	1 / 0	Event Trigger Selection Register
ETPS	0x691A	0x695A	0x699A	1 / 0	Event Trigger Prescale Register
ETFLG	0x691B	0x695B	0x699B	1 / 0	Event Trigger Flag Register
ETCLR	0x691C	0x695C	0x699C	1 / 0	Event Trigger Clear Register
ETFRC	0x691D	0x695D	0x699D	1 / 0	Event Trigger Force Register
PCCTL	0x691E	0x695E	0x699E	1 / 0	PWM Chopper Control Register
Reserved	0x6920	0x6960	0x69A0	1 / 0	Reserved
Reserved	-	-	-	1 / 0	Reserved
Reserved	-	-	-	1 / 0	Reserved
Reserved	0x6928	0x6968	0x69A8	1 / 0	Reserved
Reserved	0x692A	0x696A	0x69AA	1 / W(2)	Reserved
TBPRDM	0x692B	0x696B	0x69AB	1 / W(2)	Time Base Period Register Mirror
Reserved	0x692C	0x696C	0x69AC	1 / W(2)	Reserved
CMPAM	0x692D	0x696D	0x69AD	1 / W(2)	Compare A Register Mirror
DCTRIPSEL	0x6930	0x6970	0x69B0	1 / 0	Digital Compare Trip Select Register (1)
DCACTL	0x6931	0x6971	0x69B1	1 / 0	Digital Compare A Control Register(1)
DCBCTL	0x6932	0x6972	0x69B2	1 / 0	Digital Compare B Control Register(1)
DCFCTL	0x6933	0x6973	0x69B3	1 / 0	Digital Compare Filter Control Register(1)
DCCAPCT	0x6934	0x6974	0x69B4	1 / 0	Digital Compare Capture Control Register(1)

(1) Registers that are EALLOW protected.
(2) W = Write to shadow register

Table 6-58. ePWM5–ePWM7 Control and Status Registers (continued)

NAME	ePWM5	ePWM6	ePWM7	SIZE (x16) / #SHADOW	DESCRIPTION
DCFOFFSET	0x6935	0x6975	0x69B5	1 / 1	Digital Compare Filter Offset Register
DCFOFFSETCNT	0x6936	0x6976	0x69B6	1 / 0	Digital Compare Filter Offset Counter Register
DCFWINDOW	0x6937	0x6977	0x69B7	1 / 0	Digital Compare Filter Window Register
DCFWINDOWCNT	0x6938	0x6978	0x69B8	1 / 0	Digital Compare Filter Window Counter Register
DCCAP	0x6939	0x6979	0x69B9	1 / 1	Digital Compare Counter Capture Register

6.9.8.3 ePWM Electrical Data/Timing

PWM refers to PWM outputs on ePWM1–ePWM7. Table 6-59 shows the PWM timing requirements and Table 6-60, switching characteristics.

Table 6-59. ePWM Timing Requirements (1)

			MIN	MAX	UNIT
$t_{w(SYCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-72.

Table 6-60. ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

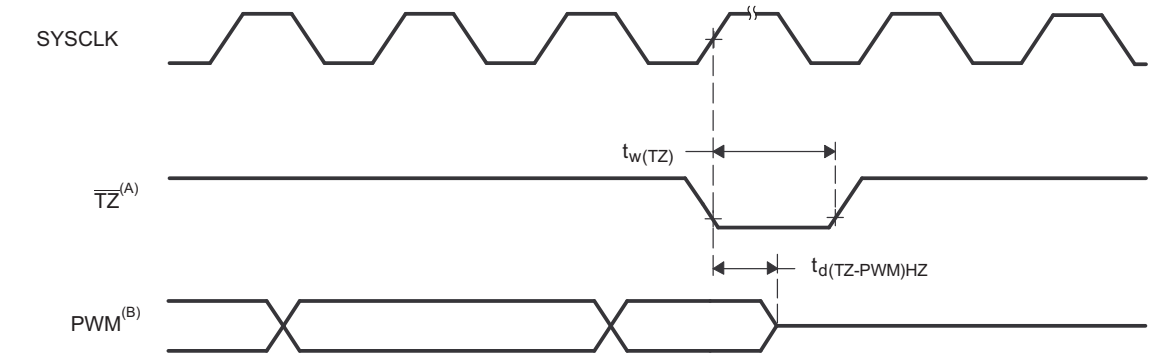
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		33.33		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SCO)}$		cycles
$t_{d(PWM)tza}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low	no pin load		25	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20	ns

6.9.8.3.1 Trip-Zone Input Timing

Table 6-61. Trip-Zone Input Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZ}x$ input low	Asynchronous	$2t_{c(TBCLK)}$		cycles
		Synchronous	$2t_{c(TBCLK)}$		cycles
		With input qualifier	$2t_{c(TBCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-72.



A. $\overline{TZ}$ - $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, $\overline{TZ4}$, $\overline{TZ5}$, $\overline{TZ6}$

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-39. PWM Hi-Z Characteristics

6.9.9 Enhanced Capture Module

6.9.9.1 eCAP Module Device-Specific Information

The device contains an enhanced capture module (eCAP1). Figure 6-40 shows a functional block diagram of a module.

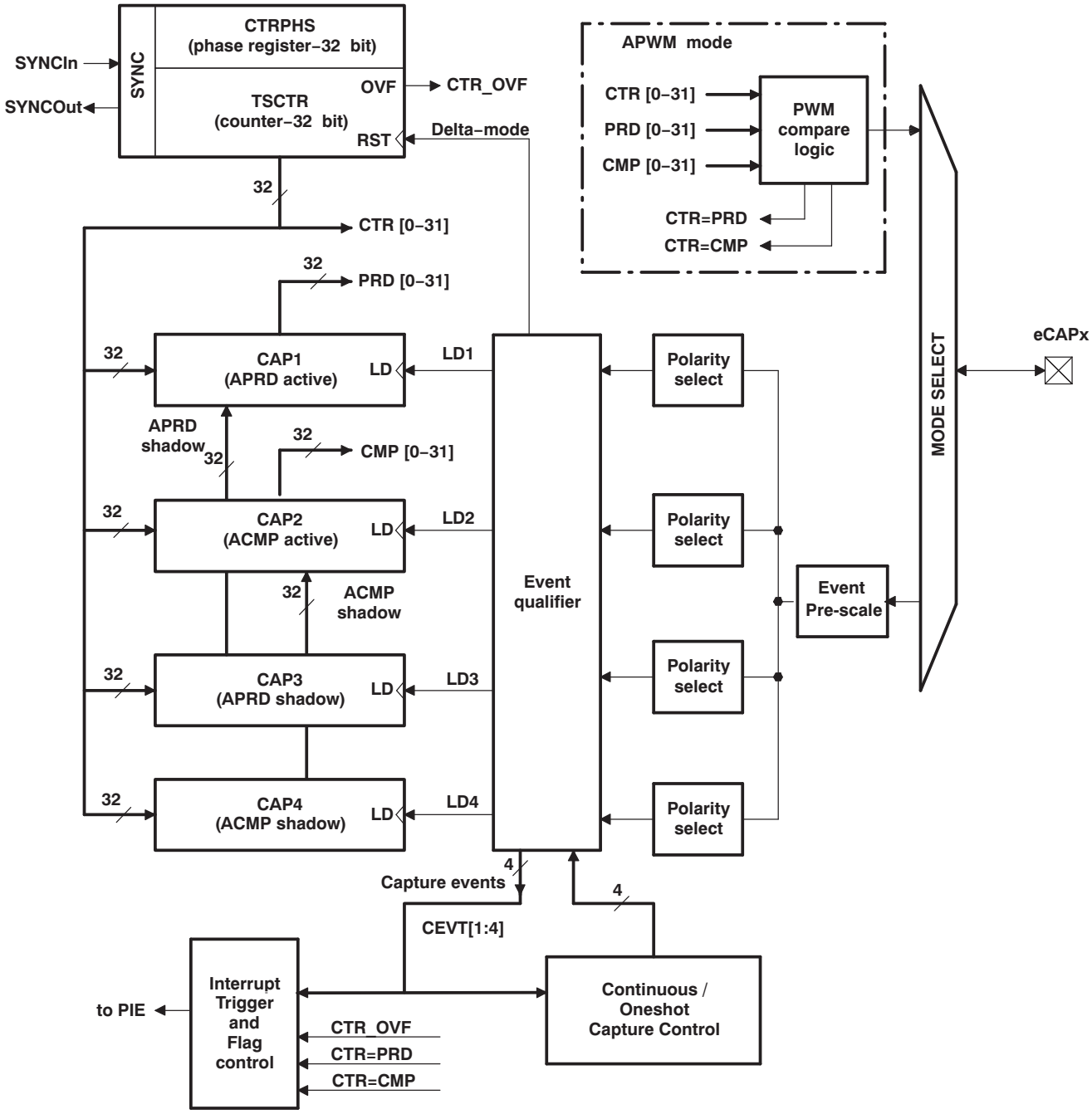


Figure 6-40. eCAP Functional Block Diagram

The eCAP module is clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1 ENCLK) in the PCLKCR1 register turn off the eCAP module individually (for low power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

6.9.9.2 eCAP Module Register Descriptions

Table 6-62 shows the eCAP Control and Status Registers.

Table 6-62. eCAP Control and Status Registers

NAME	eCAP1	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
TSCTR	0x6A00	2		Time-Stamp Counter
CTRPHS	0x6A02	2		Counter Phase Offset Value Register
CAP1	0x6A04	2		Capture 1 Register
CAP2	0x6A06	2		Capture 2 Register
CAP3	0x6A08	2		Capture 3 Register
CAP4	0x6A0A	2		Capture 4 Register
Reserved	0x6A0C – 0x6A12	8		Reserved
ECCTL1	0x6A14	1		Capture Control Register 1
ECCTL2	0x6A15	1		Capture Control Register 2
ECEINT	0x6A16	1		Capture Interrupt Enable Register
ECFLG	0x6A17	1		Capture Interrupt Flag Register
ECCLR	0x6A18	1		Capture Interrupt Clear Register
ECFRC	0x6A19	1		Capture Interrupt Force Register
Reserved	0x6A1A – 0x6A1F	6		Reserved

6.9.9.3 eCAP Module Electrical Data/Timing

Table 6-63 shows the eCAP timing requirement and Table 6-64 shows the eCAP switching characteristics.

Table 6-63. eCAP Timing Requirement(1)

			MIN	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-72.

Table 6-64. eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20		ns

6.9.10 Enhanced Quadrature Encoder Pulse

6.9.10.1 eQEP Device-Specific Information

The device contains one eQEP module. Figure 6-41 shows the eQEP functional block diagram.

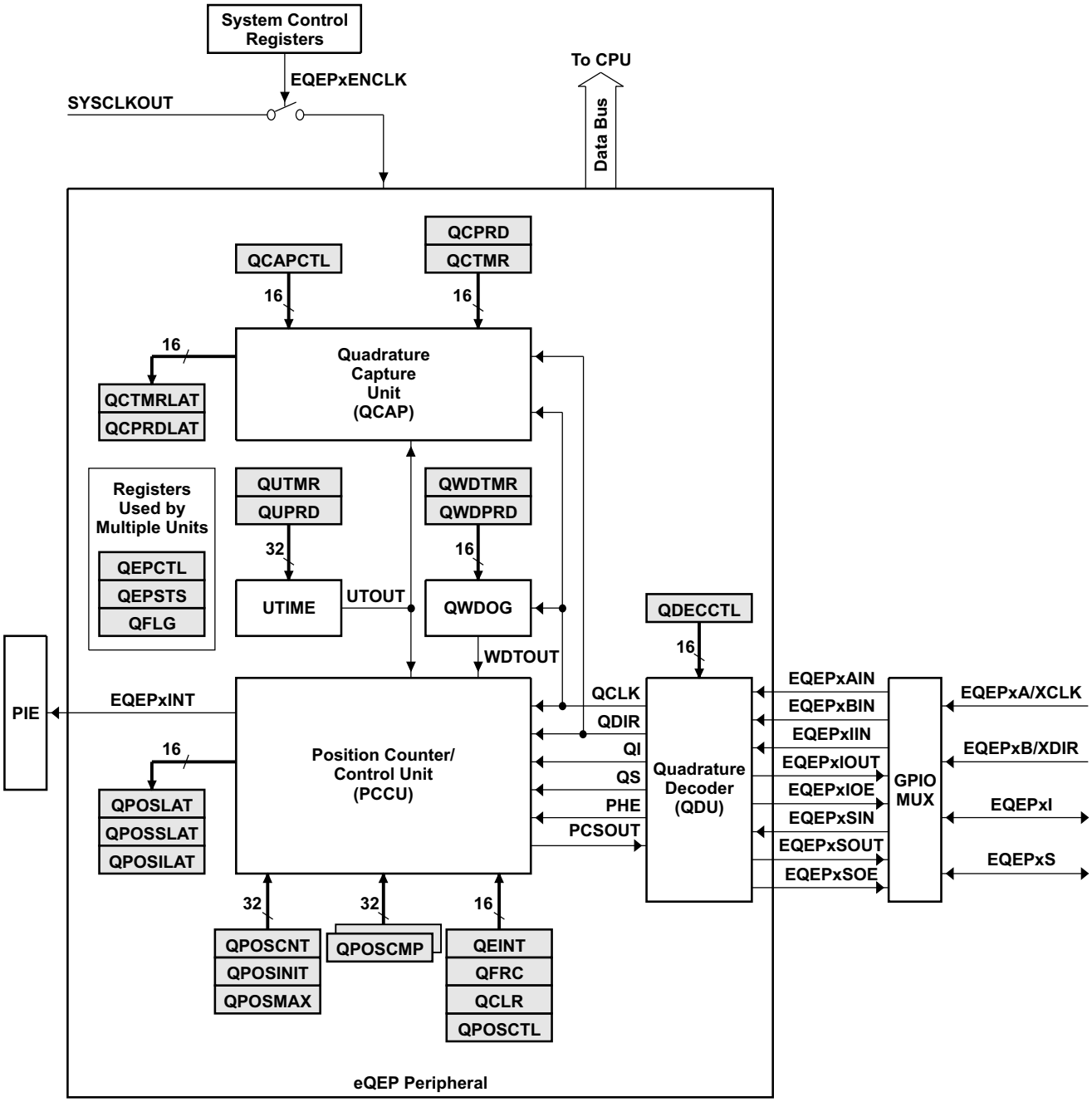


Figure 6-41. eQEP Functional Block Diagram

6.9.10.2 eQEP Register Descriptions

Table 6-65 shows the eQEP Control and Status Registers.

Table 6-65. eQEP Control and Status Registers

NAME	eQEP1 ADDRESS	eQEP1 SIZE(x16)/ #SHADOW	REGISTER DESCRIPTION
QPOSCNT	0x6B00	2/0	eQEP Position Counter
QPOSINIT	0x6B02	2/0	eQEP Initialization Position Count
QPOSMAX	0x6B04	2/0	eQEP Maximum Position Count
QPOSCMP	0x6B06	2/1	eQEP Position-compare
QPOSILAT	0x6B08	2/0	eQEP Index Position Latch
QPOSSLAT	0x6B0A	2/0	eQEP Strobe Position Latch
QPOSLAT	0x6B0C	2/0	eQEP Position Latch
QUTMR	0x6B0E	2/0	eQEP Unit Timer
QUPRD	0x6B10	2/0	eQEP Unit Period Register
QWDTMR	0x6B12	1/0	eQEP Watchdog Timer
QWDPRD	0x6B13	1/0	eQEP Watchdog Period Register
QDECCTL	0x6B14	1/0	eQEP Decoder Control Register
QEPCTL	0x6B15	1/0	eQEP Control Register
QCAPCTL	0x6B16	1/0	eQEP Capture Control Register
QPOSCTL	0x6B17	1/0	eQEP Position-compare Control Register
QEINT	0x6B18	1/0	eQEP Interrupt Enable Register
QFLG	0x6B19	1/0	eQEP Interrupt Flag Register
QCLR	0x6B1A	1/0	eQEP Interrupt Clear Register
QFRC	0x6B1B	1/0	eQEP Interrupt Force Register
QEPSTS	0x6B1C	1/0	eQEP Status Register
QCTMR	0x6B1D	1/0	eQEP Capture Timer
QCPRD	0x6B1E	1/0	eQEP Capture Period Register
QCTMRLAT	0x6B1F	1/0	eQEP Capture Timer Latch
QCPRDLAT	0x6B20	1/0	eQEP Capture Period Latch
Reserved	0x6B21 – 0x6B3F	31/0	

6.9.10.3 eQEP Electrical Data/Timing

Table 6-66 shows the eQEP timing requirement and Table 6-67 shows the eQEP switching characteristics.

Table 6-66. eQEP Timing Requirements(1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2[1t_{c(SCO)} + t_{w(IQSW)}]$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-72.

Table 6-67. eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$4t_{c(SCO)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$6t_{c(SCO)}$	cycles

6.9.11 JTAG Port

6.9.11.1 JTAG Port Device-Specific Information

On the 2805x device, the JTAG port is reduced to 5 pins ($\overline{\text{TRST}}$, TCK, TDI, TMS, TDO). TCK, TDI, TMS and TDO pins are also GPIO pins. The $\overline{\text{TRST}}$ signal selects either JTAG or GPIO operating mode for the pins in Figure 6-42. During emulation/debug, the GPIO function of these pins are not available. If the GPIO38/TCK/XCLKIN pin is used to provide an external clock, an alternate clock source should be used to clock the device during emulation/debug since this pin will be needed for the TCK function.

NOTE

In 2805x devices, the JTAG pins may also be used as GPIO pins. Care should be taken in the board design to ensure that the circuitry connected to these pins do not affect the emulation capabilities of the JTAG pin function. Any circuitry connected to these pins should not prevent the emulator from driving (or being driven by) the JTAG pins for successful debug.

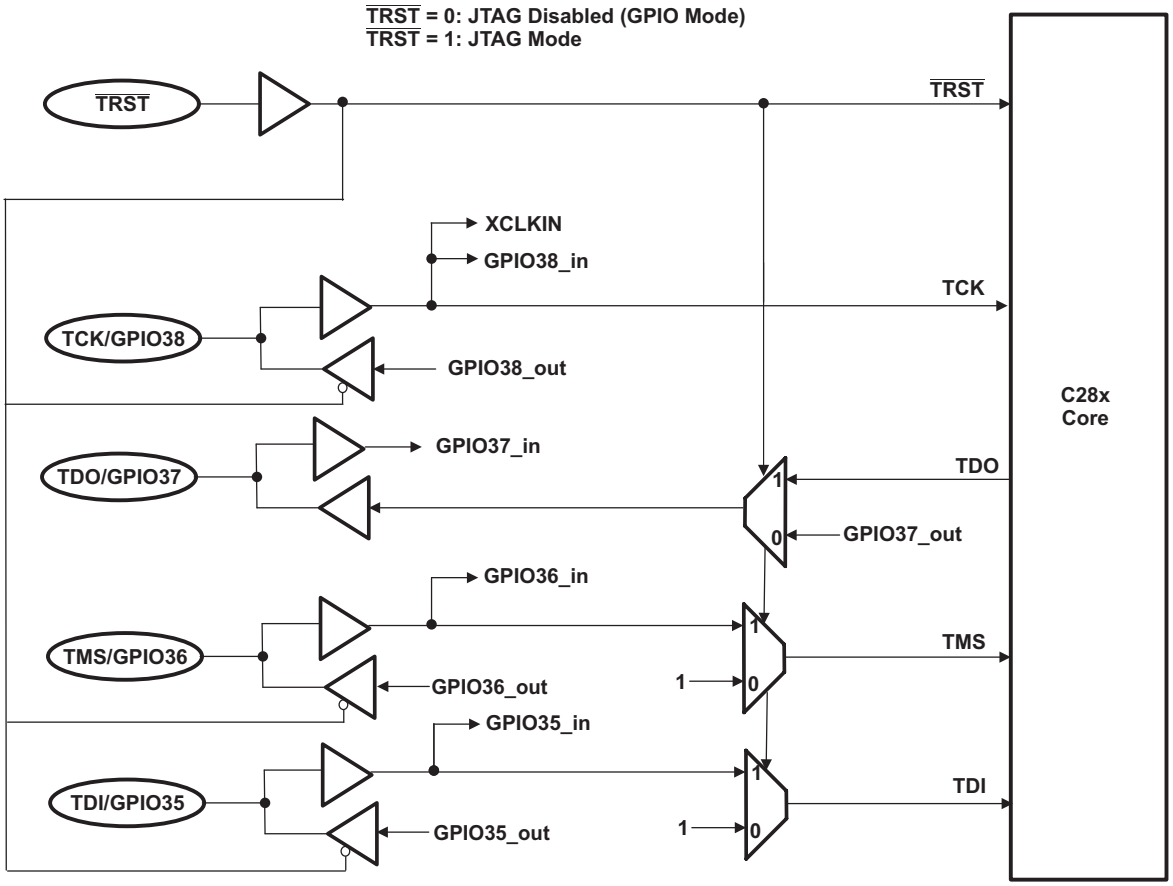


Figure 6-42. JTAG/GPIO Multiplexing

6.9.12 General-Purpose Input/Output

6.9.12.1 GPIO Device-Specific Information

The GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging I/O capability.

Table 6-68. GPIOA MUX(1) (2)

	DEFAULT AT RESET PRIMARY I/O FUNCTION	PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2	PERIPHERAL SELECTION 3
GPAMUX1 REGISTER BITS	(GPAMUX1 BITS = 00)	(GPAMUX1 BITS = 01)	(GPAMUX1 BITS = 10)	(GPAMUX1 BITS = 11)
1-0	GPIO0	EPWM1A (O)	Reserved	Reserved
3-2	GPIO1	EPWM1B (O)	Reserved	CTRIPM1OUT (O)
5-4	GPIO2	EPWM2A (O)	Reserved	Reserved
7-6	GPIO3	EPWM2B (O)	SPISOMIA (I/O)	Reserved
9-8	GPIO4	EPWM3A (O)	Reserved	Reserved
11-10	GPIO5	EPWM3B (O)	SPISIMOA (I/O)	ECAP1 (I/O)
13-12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15-14	GPIO7	EPWM4B (O)	SCIRXDA (I)	Reserved
17-16	GPIO8	EPWM5A (O)	Reserved	$\overline{\text{ADCSOCAO}}$ (O)
19-18	GPIO9	EPWM5B (O)	SCITXDB (O)	Reserved
21-20	GPIO10	EPWM6A (O)	Reserved	$\overline{\text{ADCSOCBO}}$ (O)
23-22	GPIO11	EPWM6B (O)	SCIRXDB (I)	Reserved
25-24	GPIO12	$\overline{\text{TZ1}}$ (I)/ CTRIPM1OUT (O)	SCITXDA (O)	Reserved
27-26	GPIO13	$\overline{\text{TZ2}}$ (I)	Reserved	Reserved
29-28	GPIO14	$\overline{\text{TZ3}}$ (I)/ CTRIPPFCOUT (O)	SCITXDB (O)	Reserved
31-30	GPIO15	$\overline{\text{TZ1}}$ (I)/ CTRIPM1OUT (O)	SCIRXDB (I)	Reserved

(1) The word reserved means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should the Reserved GPxMUX1/2 register setting be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.
(2) I = Input, O = Output, OC = Open Collector, OD = Open Drain

Table 6-68. GPIOA MUX[1] [2] (continued)

	DEFAULT AT RESET PRIMARY I/O FUNCTION	PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2	PERIPHERAL SELECTION 3
GPAMUX2 REGISTER BITS	(GPAMUX2 BITS = 00)	(GPAMUX2 BITS = 01)	(GPAMUX2 BITS = 10)	(GPAMUX2 BITS = 11)
1-0	GPIO16	SPISIMOA (I/O)	EQEP1S (I/O)	$\overline{\text{TZ2}}$ (I)
3-2	GPIO17	SPISOMIA (I/O)	EQEP1I (I/O)	$\overline{\text{TZ3}}$ (I)/ CTRIPPFCOUT (O)
5-4	GPIO18	SPICLKA (I/O)	SCITXDB (O)	XCLKOUT (O)
7-6	GPIO19/XCLKIN	$\overline{\text{SPISTEA}}$ (I/O)	SCIRXDB (I)	ECAP1 (I/O)
9-8	GPIO20	EQEP1A (I)	EPWM7A (O)	CTRIPM1OUT (O)
11-10	GPIO21	EQEP1B (I)	EPWM7B (O)	Reserved
13-12	GPIO22	EQEP1S (I/O)	Reserved	SCITXDB (O)
15-14	GPIO23	EQEP1I (I/O)	Reserved	SCIRXDB (I)
17-16	GPIO24	ECAP1 (I/O)	EPWM7A (O)	Reserved
19-18	GPIO25	Reserved	Reserved	Reserved
21-20	GPIO26	Reserved	SCIRXDC (O)	Reserved
23-22	GPIO27	Reserved	SCITXDC (O)	Reserved
25-24	GPIO28	SCIRXDA (I)	SDAA (I/OC)	$\overline{\text{TZ2}}$ (I)
27-26	GPIO29	SCITXDA (O)	SCLA (I/OC)	$\overline{\text{TZ3}}$ (I)/ CTRIPPFCOUT (O)
29-28	GPIO30	CANRXA (I)	SCIRXDB (I)	EPWM7A (O)
31-30	GPIO31	CANTXA (O)	SCITXDB (I)	EPWM7B (O)

Table 6-69. GPIOB MUX[1]

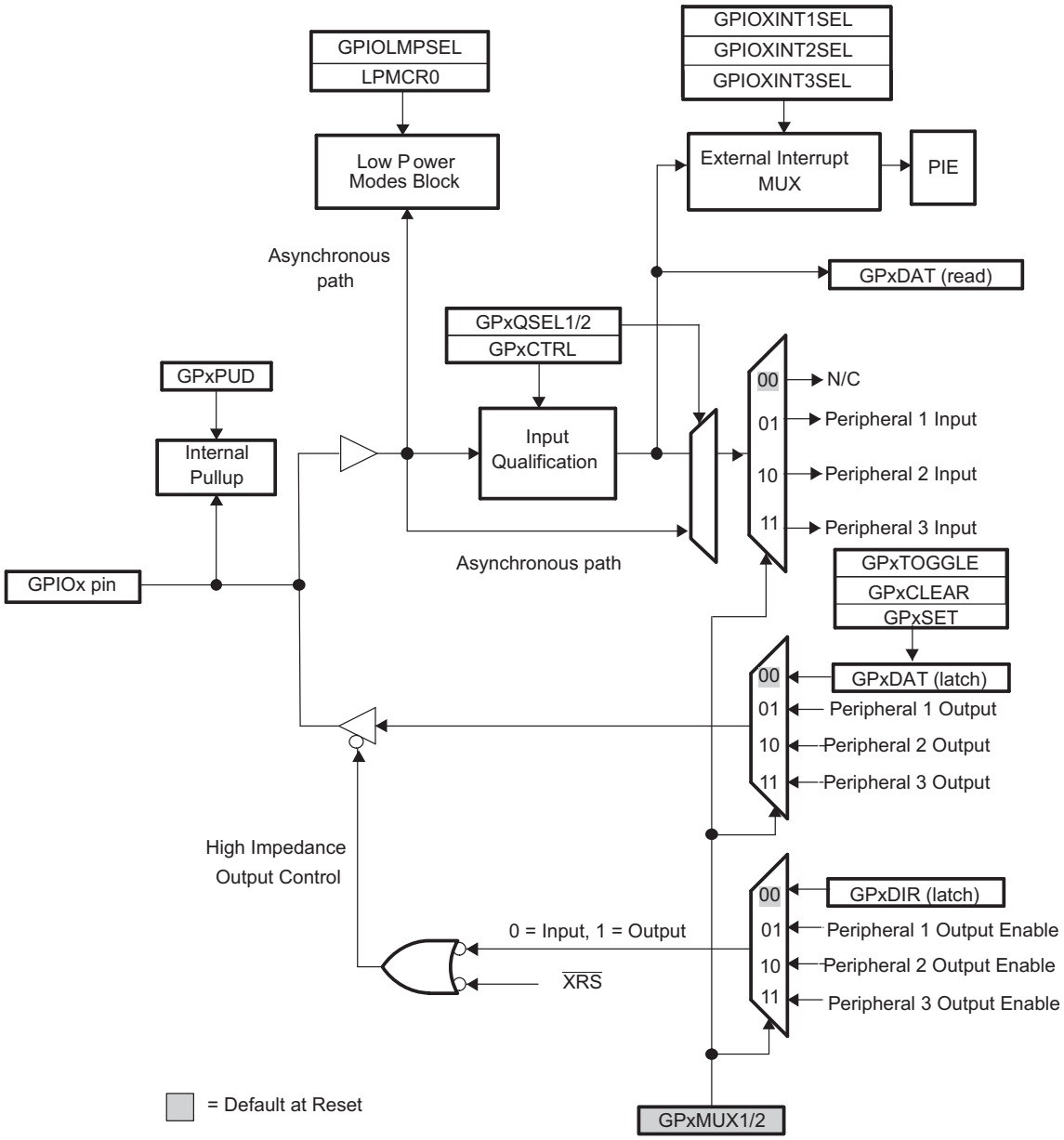
	DEFAULT AT RESET PRIMARY I/O FUNCTION	PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2	PERIPHERAL SELECTION 3
GPBMUX1 REGISTER BITS	(GPBMUX1 BITS = 00)	(GPBMUX1 BITS = 01)	(GPBMUX1 BITS = 10)	(GPBMUX1 BITS = 11)
1-0	GPIO32	SDAA (I/OC)	EPWMSYNCI (I)	EQEP1S (I/O)
3-2	GPIO33	SCLA (I/OC)	EPWMSYNCO (O)	EQEP1I (I/O)
5-4	GPIO34	Reserved	Reserved	CTRIPPFCOUT (O)
7-6	GPIO35 (TDI)	Reserved	Reserved	Reserved
9-8	GPIO36 (TMS)	Reserved	Reserved	Reserved
11-10	GPIO37 (TDO)	Reserved	Reserved	Reserved
13-12	GPIO38/XCLKIN (TCK)	Reserved	Reserved	Reserved
15-14	GPIO39	Reserved	SCIRXDC (I)	CTRIPPFCOUT (O)
17-16	GPIO40	EPWM7A (O)	Reserved	Reserved
19-18	Reserved	Reserved	Reserved	Reserved
21-20	GPIO42	Reserved	Reserved	CTRIPM1OUT (O)
23-22	Reserved	Reserved	Reserved	Reserved
25-24	Reserved	Reserved	Reserved	Reserved
27-26	Reserved	Reserved	Reserved	Reserved
29-28	Reserved	Reserved	Reserved	Reserved
31-30	Reserved	Reserved	Reserved	Reserved

(1) I = Input, O = Output, OC = Open Collector, OD = Open Drain

The user can select the type of input qualification for each GPIO pin via the GPxQSEL1/2 registers from four choices:

- Synchronization to SYSCLKOUT Only (GPxQSEL1/2 = 0, 0): This mode is the default mode of all GPIO pins at reset and this mode simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2 = 0, 1 and 1, 0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.
- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. The sampling period specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in Figure 6-45 (for 6 sample mode).
- No Synchronization (GPxQSEL1/2 = 1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multi-level multiplexing that is required on the device, there may be cases where a peripheral input signal can be mapped to more then one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.



A. x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected.

B. GPxDAT latch/read are accessed at the same memory location.

C. This diagram is a generic GPIO MUX block diagram. Not all options may be applicable for all GPIO pins. See the Systems Control and Interrupts chapter of the *TMS320x2805x Piccolo Technical Reference Manual* (SPRUHE5) for pin-specific variations.

Figure 6-43. GPIO Multiplexing

6.9.12.2 GPIO Register Descriptions

The device supports 42 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). Table 6-70 shows the GPIO register mapping.

Table 6-70. GPIO Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pull Up Disable Register (GPIO0 to 31)
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 44)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 44)
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 44)
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 44)
GPBPUD	0x6F9C	2	GPIO B Pull Up Disable Register (GPIO32 to 44)
Reserved	0x6FB6	2	Reserved
Reserved	0x6FBA	2	Reserved
GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO A Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO A Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO A Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO A Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO B Data Register (GPIO32 to 44)
GPBSET	0x6FCA	2	GPIO B Data Set Register (GPIO32 to 44)
GPBCLEAR	0x6FCC	2	GPIO B Data Clear Register (GPIO32 to 44)
GPBTOGGLE	0x6FCE	2	GPIO B Data Toggle Register (GPIO32 to 44)
Reserved	0x6FD8	2	Reserved
Reserved	0x6FDA	2	Reserved
Reserved	0x6FDC	2	Reserved
Reserved	0x6FDE	2	Reserved
GPIO INTERRUPT AND LOW POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT3SEL	0x6FE2	1	XINT3 GPIO Input Select Register (GPIO0 to 31)
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)

NOTE

There is a two-SYSCLKOUT cycle delay from when the write to the GPxMUXn and GPxQSELn registers occurs to when the action is valid.

6.9.12.3 GPIO Electrical Data/Timing

6.9.12.3.1 GPIO - Output Timing

Table 6-71. General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		13(1)	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		13(1)	ns
t_{fGPO}	Toggling frequency			15	MHz

(1) Rise time and fall time vary with electrical loading on I/O pins. Values given in Table 6-71 are applicable for a 40-pF load on I/O pins.

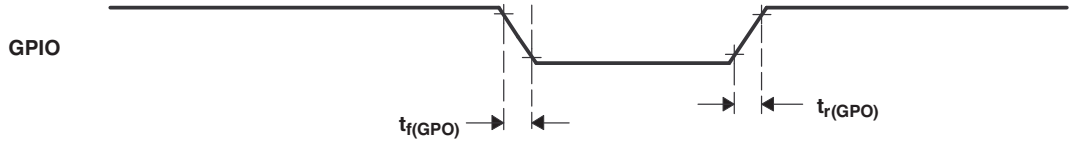


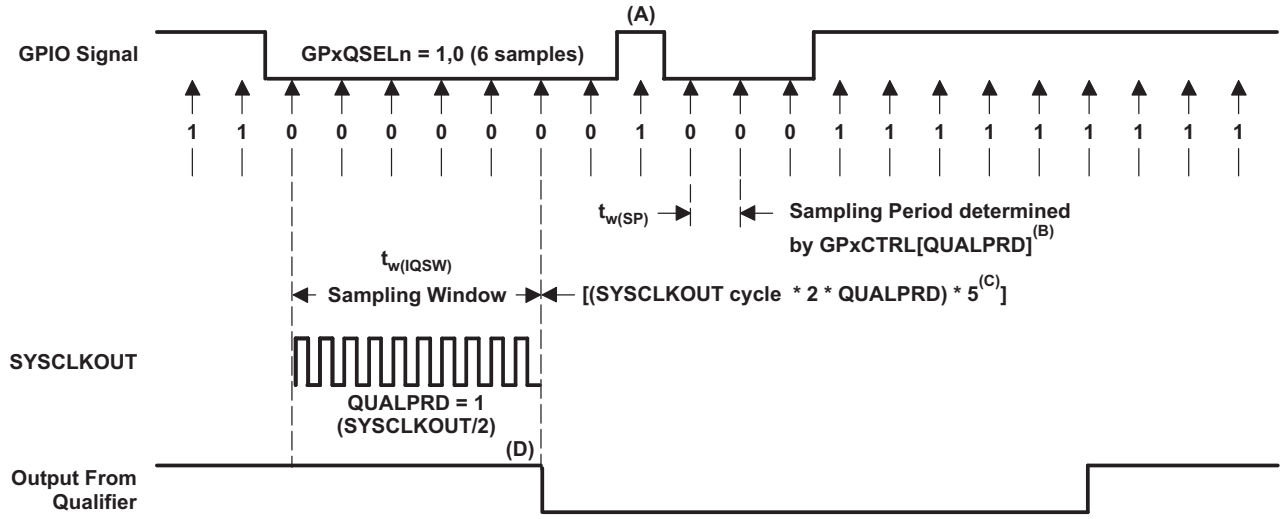
Figure 6-44. General-Purpose Output Timing

6.9.12.3.2 GPIO - Input Timing

Table 6-72. General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SCO)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SCO)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SCO)}$		cycles
		With input qualifier	$t_{w(IQSW)}$ + $t_{w(SP)}$ + $1t_{c(SCO)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. The QUALPRD bit field value can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLKOUT cycle. For any other value "n", the qualification sampling period in 2n SYSCLKOUT cycles (that is, at every 2n SYSCLKOUT cycles, the GPIO pin will be sampled).

B. The qualification period selected via the GPxCTRL register applies to groups of 8 GPIO pins.

C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.

D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLKOUT cycles. This condition would ensure 5 sampling periods for detection to occur. Since external signals are driven asynchronously, an 13-SYSCLKOUT-wide pulse ensures reliable recognition.

Figure 6-45. Sampling Mode

6.9.12.3.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLKOUT.

Sampling frequency = SYSCLKOUT/(2 * QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLKOUT, if QUALPRD = 0

Sampling period = SYSCLKOUT cycle x 2 x QUALPRD, if QUALPRD ≠ 0

In the above equations, SYSCLKOUT cycle indicates the time period of SYSCLKOUT.

Sampling period = SYSCLKOUT cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. The number of samples is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 5, if QUALPRD = 0

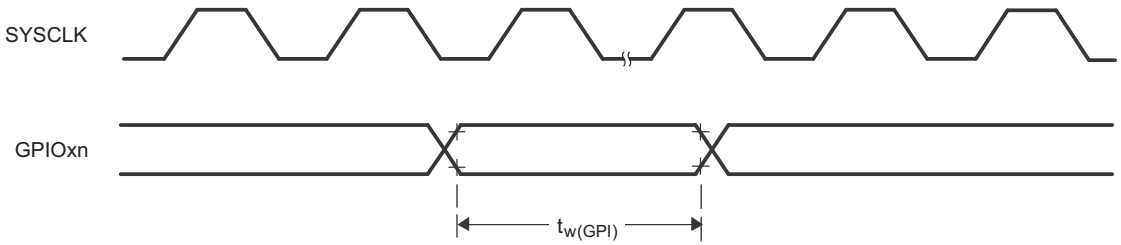


Figure 6-46. General-Purpose Input Timing

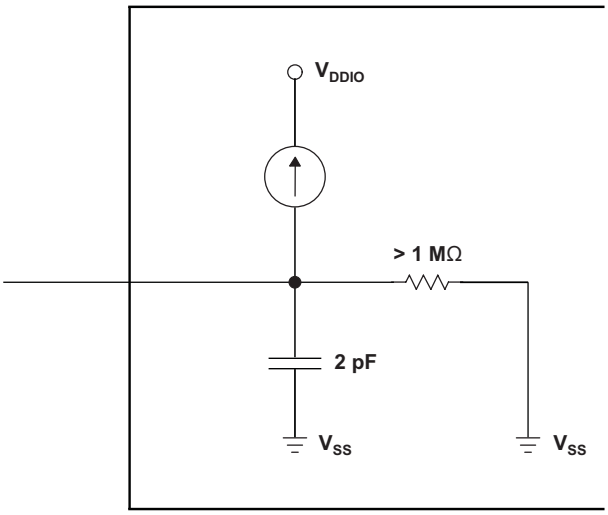


Figure 6-47. Input Resistance Model for a GPIO Pin With an Internal Pull-up

6.9.12.3.4 Low-Power Mode Wakeup Timing

Table 6-73 shows the timing requirements, Table 6-74 shows the switching characteristics, and Figure 6-48 shows the timing diagram for IDLE mode.

Table 6-73. IDLE Mode Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SCO)}$		cycles
		With input qualifier	$5t_{c(SCO)} + t_{w(IQSW)}$		

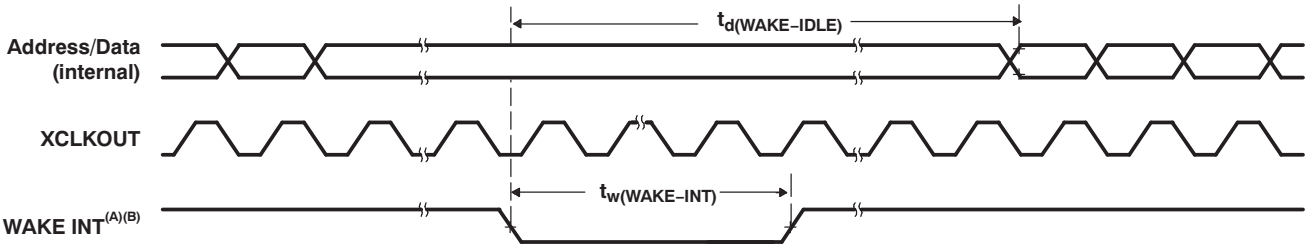
(1) For an explanation of the input qualifier parameters, see Table 6-72.

Table 6-74. IDLE Mode Switching Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume (2)				cycles
	• Wake-up from Flash – Flash module in active state	Without input qualifier		$20t_{c(SCO)}$	cycles
		With input qualifier		$20t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from Flash – Flash module in sleep state	Without input qualifier		$1050t_{c(SCO)}$	cycles
		With input qualifier		$1050t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from SARAM	Without input qualifier		$20t_{c(SCO)}$	cycles
		With input qualifier		$20t_{c(SCO)} + t_{w(IQSW)}$	

(1) For an explanation of the input qualifier parameters, see Table 6-72.
(2) This delay time is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake-up) signal involves additional latency.



A. WAKE INT can be any enabled interrupt, $\overline{\text{WDINT}}$ or $\overline{\text{XRS}}$. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
B. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 6-48. IDLE Entry and Exit Timing

Table 6-75. STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualification	$3t_{c(OSCCLK)}$		cycles
		With input qualification(1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

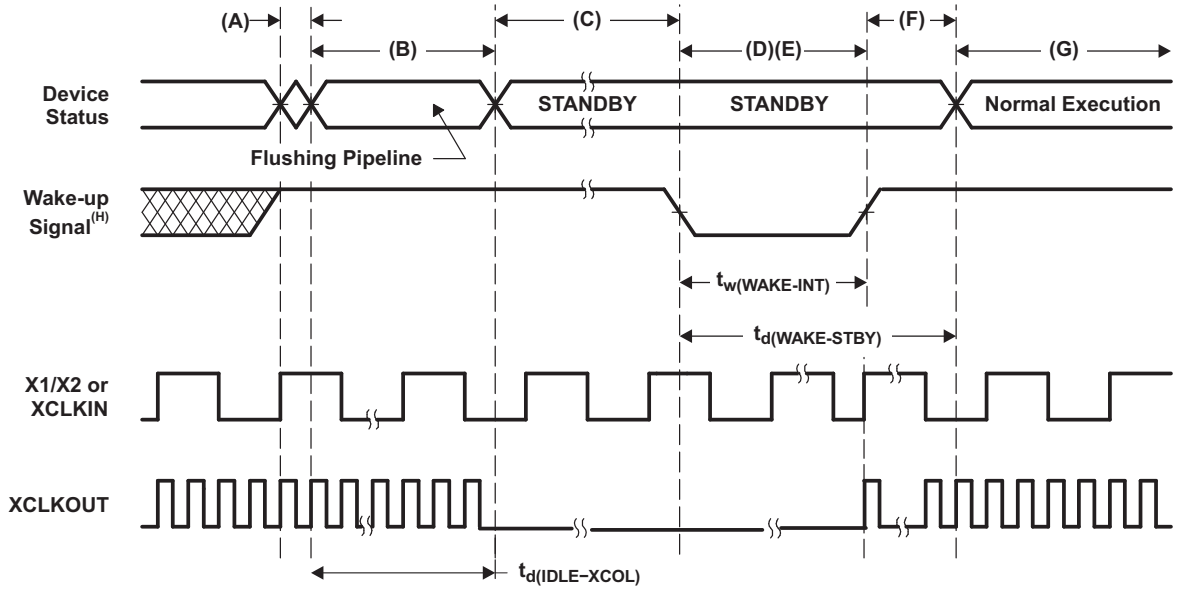
(1) QUALSTDBY is a 6-bit field in the LPMCR0 register.

Table 6-76. STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low		$32t_{c(SCO)}$	$45t_{c(SCO)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)				cycles
	• Wake up from flash – Flash module in active state	Without input qualifier		$100t_{c(SCO)}$	cycles
		With input qualifier		$100t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from flash – Flash module in sleep state	Without input qualifier		$1125t_{c(SCO)}$	cycles
		With input qualifier		$1125t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from SARAM	Without input qualifier		$100t_{c(SCO)}$	cycles
		With input qualifier		$100t_{c(SCO)} + t_{w(WAKE-INT)}$	

(1) This delay time is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up signal) involves additional latency.



A. IDLE instruction is executed to put the device into STANDBY mode.

B. The PLL block responds to the STANDBY signal. SYSCLKOUT is held for the number of cycles indicated below before being turned off:
   - 16 cycles, when DIVSEL = 00 or 01
   - 32 cycles, when DIVSEL = 10
   - 64 cycles, when DIVSEL = 11

   This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. The external wake-up signal is driven active.

E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.

F. After a latency period, the STANDBY mode is exited.

G. Normal execution resumes. The device will respond to the interrupt (if enabled).

H. From the time the IDLE instruction is executed to place the device into low-power mode, wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 6-49. STANDBY Entry and Exit Timing Diagram

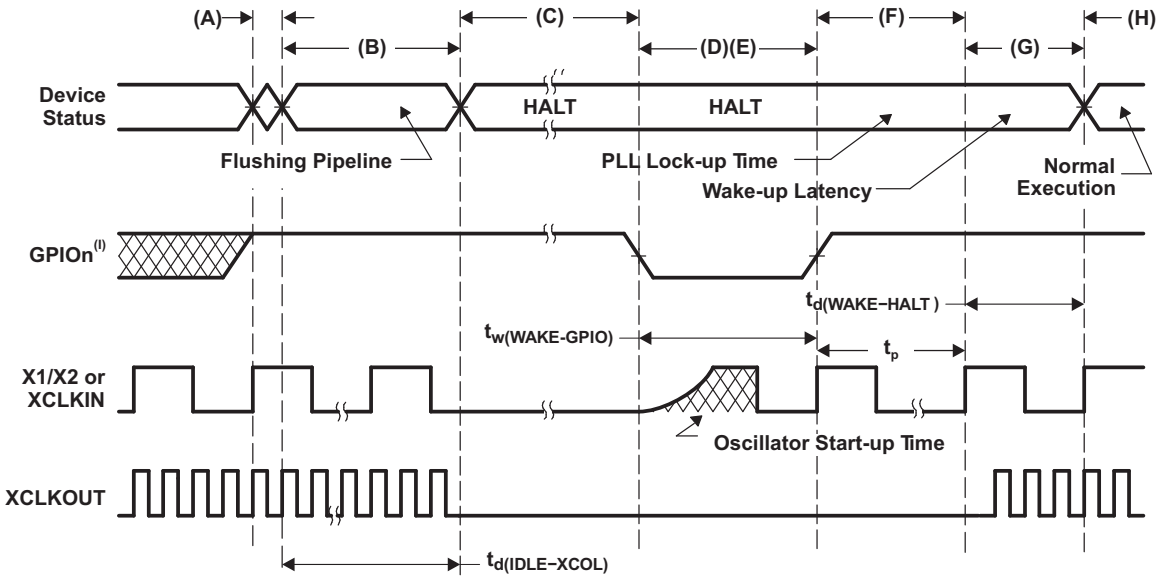
Table 6-77. HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal	$t_{oscst} + 2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wakeup signal	$t_{oscst} + 8t_{c(OSCCLK)}$		cycles

Table 6-78. HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low	$32t_{c(SCO)}$	$45t_{c(SCO)}$	cycles
t_p	PLL lock-up time		1	ms
$t_{d(WAKE-HALT)}$	Delay time, PLL lock to program execution resume • Wake up from flash – Flash module in sleep state		$1125t_{c(SCO)}$	cycles
	• Wake up from SARAM		$35t_{c(SCO)}$	cycles



A. IDLE instruction is executed to put the device into HALT mode.

B. The PLL block responds to the HALT signal. SYSCLKOUT is held for the number of cycles indicated below before oscillator is turned off and the CLKIN to the core is stopped:
   - 16 cycles, when DIVSEL = 00 or 01
   - 32 cycles, when DIVSEL = 10
   - 64 cycles, when DIVSEL = 11

   This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes absolute minimum power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT mode. Keeping INTOSC1, INTOSC2, and the watchdog alive in HALT mode is done by writing to the appropriate bits in the CLKCTL register. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized, which enables the provision of a clean clock signal during the PLL lock sequence. Since the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.

E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.

F. Once the oscillator has stabilized, the PLL lock sequence is initiated, which takes 1 ms.

G. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after a latency. The HALT mode is now exited.

H. Normal operation resumes.

I. From the time the IDLE instruction is executed to place the device into low-power mode, wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 6-50. HALT Wake-Up Using GPIOn

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x generation of MCUs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of 2805x-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - Cycle Accurate Simulator
- Application algorithms
- Sample applications code

Hardware Development Tools

- Development and evaluation boards
- JTAG-based emulators – XDS510™ class, XDS560™ emulator, XDS100
- Flash programming tools
- Power supply
- Documentation and cables

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

7.1.1.1 Getting Started

This section gives a brief overview of the steps to take when first developing for a C28x device. For more detail on each of these steps, see the following:

- *Getting Started With TMS320C28x Digital Signal Controllers* (SPRAAM0).
- C2000 Getting Started Website (http://www.ti.com/c2000getstarted)
- TMS320F28x MCU Development and Experimenter's Kits (http://www.ti.com/f28xkits)

7.1.2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320 MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F28055). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

- **TMX** Experimental device that is not necessarily representative of the final device's electrical specifications
- **TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
- **TMS** Fully qualified production device

Support tool development evolutionary flow:

- **TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing
- **TMDS** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PN) and temperature range (for example, T). Figure 7-1 provides a legend for reading the complete device name for any family member.

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F28055, TMS320F28054, TMS320F28053, TMS320F28052, TMS320F28051, TMS320F28050 Piccolo MCU Silicon Errata* (SPRZ362).

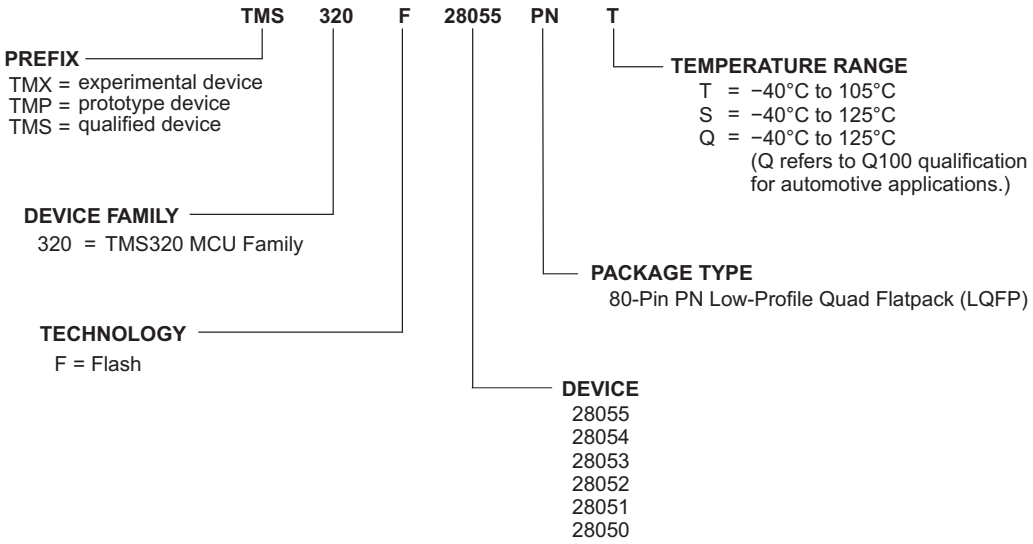


Figure 7-1. Device Nomenclature

7.2 Documentation Support

Extensive documentation supports all of the TMS320 MCU family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications.

The following documents can be downloaded from the TI website (www.ti.com):

Data Manual and Errata

SPRS797 **TMS320F28055, TMS320F28054, TMS320F28053, TMS320F28052, TMS320F28051, TMS320F28050 Piccolo Microcontrollers Data Manual** contains the pinout, signal descriptions, as well as electrical and timing specifications for the 2805x devices.

SPRZ362 **TMS320F28055, TMS320F28054, TMS320F28053, TMS320F28052, TMS320F28051, TMS320F28050 Piccolo MCU Silicon Errata** describes known advisories on silicon and provides workarounds.

InstaSPIN Technical Reference Manuals

SPRUHJ1 **InstaSPIN-FOC™ and InstaSPIN-MOTION™ User's Guide** describes the InstaSPIN-FOC and InstaSPIN-MOTION devices.

SPRUHW0 **TMS320F28054F, TMS320F28052F InstaSPIN-FOC™ Software Technical Reference Manual** describes TMS320F28054F and TMS320F28052F InstaSPIN-FOC software.

SPRUHW1 **TMS320F28054M, TMS320F28052M InstaSPIN-MOTION™ Software Technical Reference Manual** describes TMS320F28054M and TMS320F28052M InstaSPIN-MOTION software.

Technical Reference Manual

SPRUHE5 **TMS320x2805x Piccolo Technical Reference Manual** details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the 2805x microcontrollers.

CPU User's Guides

SPRU430 **TMS320C28x CPU and Instruction Set Reference Guide** describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

Peripheral Guides

SPRU566 **TMS320x28xx, 28xxx DSP Peripheral Reference Guide** describes the peripheral reference guides of the 28x digital signal processors (DSPs).

Tools Guides

SPRU513 **TMS320C28x Assembly Language Tools v6.2.4 User's Guide** describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514 **TMS320C28x Optimizing C/C++ Compiler v6.2.4 User's Guide** describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 digital signal processor (DSP) assembly language source code for the TMS320C28x device.

SPRU608 **TMS320C28x Instruction Set Simulator Technical Overview** describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x core.

Application Reports

SZZA021 **Semiconductor Packing Methodology** describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

7.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TMS320F28055	Click here	Click here	Click here	Click here	Click here
TMS320F28054	Click here	Click here	Click here	Click here	Click here
TMS320F28053	Click here	Click here	Click here	Click here	Click here
TMS320F28052	Click here	Click here	Click here	Click here	Click here
TMS320F28051	Click here	Click here	Click here	Click here	Click here
TMS320F28050	Click here	Click here	Click here	Click here	Click here

7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.5 Trademarks

Piccolo, InstaSPIN-MOTION, InstaSPIN-FOC, InstaSPIN, TMS320C2000, DSP/BIOS, Code Composer Studio, XDS510, XDS560, TMS320, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28050PNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28050PNQ TMS320	Samples
TMS320F28050PNS	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28050PNS TMS320	Samples
TMS320F28050PNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28050PNT TMS320	Samples
TMS320F28051PNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28051PNQ TMS320	Samples
TMS320F28051PNS	ACTIVE	LQFP	PN	80		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28051PNS TMS320	Samples
TMS320F28051PNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28051PNT TMS320	Samples
TMS320F28052FPNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28052FPNQ TMS320	Samples
TMS320F28052FPNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28052FPNT TMS320	Samples
TMS320F28052MPNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28052MPNQ TMS320	Samples
TMS320F28052MPNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28052MPNT TMS320	Samples
TMS320F28052PNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28052PNQ TMS320	Samples
TMS320F28052PNS	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28052PNS TMS320	Samples
TMS320F28052PNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28052PNT TMS320	Samples
TMS320F28053PNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28053PNQ TMS320	Samples
TMS320F28053PNS	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28053PNS TMS320	Samples
TMS320F28053PNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28053PNT TMS320	Samples
TMS320F28054FPNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28054FPNQ TMS320	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28054FPNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28054FPNT TMS320	Samples
TMS320F28054MPNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28054MPNQ TMS320	Samples
TMS320F28054MPNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28054MPNT TMS320	Samples
TMS320F28054PNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28054PNQ TMS320	Samples
TMS320F28054PNS	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28054PNS TMS320	Samples
TMS320F28054PNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28054PNT TMS320	Samples
TMS320F28055PNQ	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28055PNQ TMS320	Samples
TMS320F28055PNS	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	F28055PNS TMS320	Samples
TMS320F28055PNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	F28055PNT TMS320	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

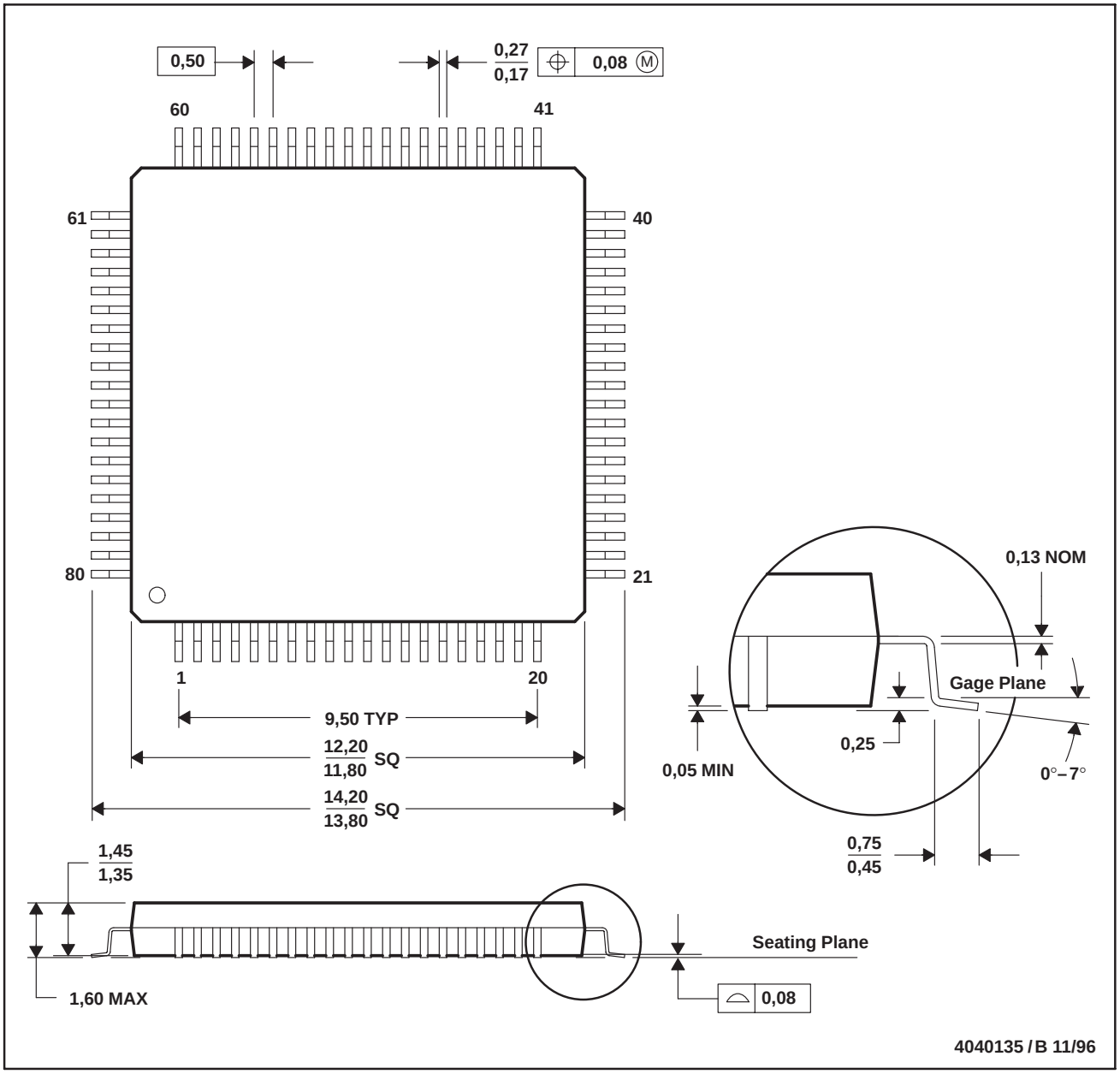
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265