

## Excellent Integrated System Limited

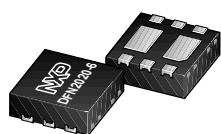
Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[NXP Semiconductors/Freescale Semiconductor, Inc.](#)  
[PBSS5160PAP,115](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)



# PBSS5160PAP

60 V, 1 A PNP/PNP low V<sub>CEsat</sub> (BISS) transistor

23 January 2013

Product data sheet

## 1. General description

PNP/PNP low V<sub>CEsat</sub> Breakthrough In Small Signal (BISS) transistor in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PBSS4160PANP. NPN/NPN complement: PBSS4160PAN.

## 2. Features and benefits

- Very low collector-emitter saturation voltage V<sub>CEsat</sub>
- High collector current capability I<sub>C</sub> and I<sub>CM</sub>
- High collector current gain h<sub>FE</sub> at high I<sub>C</sub>
- Reduced Printed-Circuit Board (PCB) requirements
- High energy efficiency due to less heat generation
- AEC-Q101 qualified

## 3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

## 4. Quick reference data

Table 1. Quick reference data

| Symbol                | Parameter                               | Conditions                                                                                                            | Min | Typ | Max  | Unit |
|-----------------------|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| <b>Per transistor</b> |                                         |                                                                                                                       |     |     |      |      |
| V <sub>CEO</sub>      | collector-emitter voltage               | open base                                                                                                             | -   | -   | -60  | V    |
| I <sub>C</sub>        | collector current                       |                                                                                                                       | -   | -   | -1   | A    |
| I <sub>CM</sub>       | peak collector current                  | single pulse; t <sub>p</sub> ≤ 1 ms                                                                                   | -   | -   | -1.5 | A    |
| <b>Per transistor</b> |                                         |                                                                                                                       |     |     |      |      |
| R <sub>CEsat</sub>    | collector-emitter saturation resistance | I <sub>C</sub> = -0.5 A; I <sub>B</sub> = -50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C | -   | -   | 360  | mΩ   |



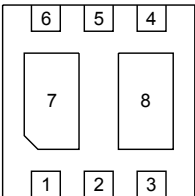
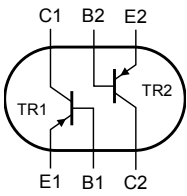
## NXP Semiconductors

## PBSS5160PAP

60 V, 1 A PNP/PNP low VCEsat (BISS) transistor

### 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description   | Simplified outline                                                                                                                           | Graphic symbol                                                                                    |
|-----|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|
| 1   | E1     | emitter TR1   |  <p>Transparent top view<br/><b>DFN2020-6 (SOT1118)</b></p> |  <p>sym138</p> |
| 2   | B1     | base TR1      |                                                                                                                                              |                                                                                                   |
| 3   | C2     | collector TR2 |                                                                                                                                              |                                                                                                   |
| 4   | E2     | emitter TR2   |                                                                                                                                              |                                                                                                   |
| 5   | B2     | base TR2      |                                                                                                                                              |                                                                                                   |
| 6   | C1     | collector TR1 |                                                                                                                                              |                                                                                                   |
| 7   | C1     | collector TR1 |                                                                                                                                              |                                                                                                   |
| 8   | C2     | collector TR2 |                                                                                                                                              |                                                                                                   |

### 6. Ordering information

Table 3. Ordering information

| Type number | Package   |                                                                                                        |         |
|-------------|-----------|--------------------------------------------------------------------------------------------------------|---------|
|             | Name      | Description                                                                                            | Version |
| PBSS5160PAP | DFN2020-6 | plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm | SOT1118 |

### 7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PBSS5160PAP | 2L           |

### 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                | Parameter                 | Conditions                          | Min | Max  | Unit |
|-----------------------|---------------------------|-------------------------------------|-----|------|------|
| <b>Per transistor</b> |                           |                                     |     |      |      |
| V <sub>CBO</sub>      | collector-base voltage    | open emitter                        | -   | -60  | V    |
| V <sub>CEO</sub>      | collector-emitter voltage | open base                           | -   | -60  | V    |
| V <sub>EBO</sub>      | emitter-base voltage      | open collector                      | -   | -7   | V    |
| I <sub>C</sub>        | collector current         |                                     | -   | -1   | A    |
| I <sub>CM</sub>       | peak collector current    | single pulse; t <sub>p</sub> ≤ 1 ms | -   | -1.5 | A    |
| I <sub>B</sub>        | base current              |                                     | -   | -0.3 | A    |

## NXP Semiconductors

## PBSS5160PAP

60 V, 1 A PNP/PNP low VCEsat (BISS) transistor

| Symbol           | Parameter               | Conditions                          |     | Min | Max  | Unit |
|------------------|-------------------------|-------------------------------------|-----|-----|------|------|
| I <sub>BM</sub>  | peak base current       | single pulse; t <sub>p</sub> ≤ 1 ms |     | -   | -1   | A    |
| P <sub>tot</sub> | total power dissipation | T <sub>amb</sub> ≤ 25 °C            | [1] | -   | 370  | mW   |
|                  |                         |                                     | [2] | -   | 570  | mW   |
|                  |                         |                                     | [3] | -   | 530  | mW   |
|                  |                         |                                     | [4] | -   | 700  | mW   |
|                  |                         |                                     | [5] | -   | 450  | mW   |
|                  |                         |                                     | [6] | -   | 760  | mW   |
|                  |                         |                                     | [7] | -   | 700  | mW   |
|                  |                         |                                     | [8] | -   | 1450 | mW   |
| Per device       |                         |                                     |     |     |      |      |
| P <sub>tot</sub> | total power dissipation | T <sub>amb</sub> ≤ 25 °C            | [1] | -   | 510  | mW   |
|                  |                         |                                     | [2] | -   | 780  | mW   |
|                  |                         |                                     | [3] | -   | 730  | mW   |
|                  |                         |                                     | [4] | -   | 960  | mW   |
|                  |                         |                                     | [5] | -   | 620  | mW   |
|                  |                         |                                     | [6] | -   | 1040 | mW   |
|                  |                         |                                     | [7] | -   | 960  | mW   |
|                  |                         |                                     | [8] | -   | 2000 | mW   |
| T <sub>j</sub>   | junction temperature    |                                     | -   | 150 | °C   |      |
| T <sub>amb</sub> | ambient temperature     |                                     | -55 | 150 | °C   |      |
| T <sub>stg</sub> | storage temperature     |                                     | -65 | 150 | °C   |      |

[1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

[3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.

[4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

[5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.

[6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

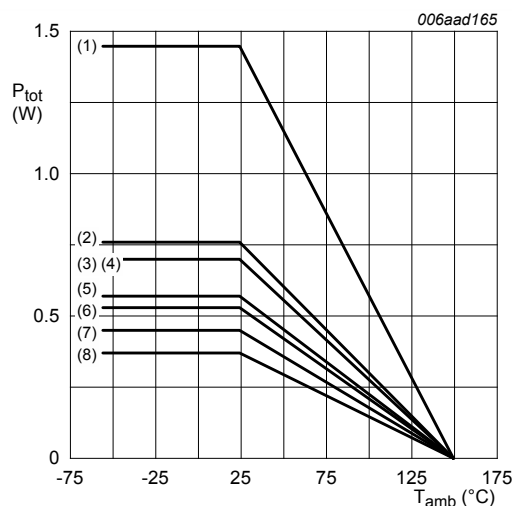
[7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.

[8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

## NXP Semiconductors

## PBSS5160PAP

60 V, 1 A PNP/PNP low VCEsat (BISS) transistor



- (1) 4-layer PCB 70  $\mu\text{m}$ , mounting pad for collector 1  $\text{cm}^2$
- (2) FR4 PCB 70  $\mu\text{m}$ , mounting pad for collector 1  $\text{cm}^2$
- (3) 4-layer PCB 70  $\mu\text{m}$ , standard footprint
- (4) 4-layer PCB 35  $\mu\text{m}$ , mounting pad for collector 1  $\text{cm}^2$
- (5) FR4 PCB 35  $\mu\text{m}$ , mounting pad for collector 1  $\text{cm}^2$
- (6) 4-layer PCB 35  $\mu\text{m}$ , standard footprint
- (7) FR4 PCB 70  $\mu\text{m}$ , standard footprint
- (8) FR4 PCB 35  $\mu\text{m}$ , standard footprint

Fig. 1. Per transistor: power derating curves

## 9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol                | Parameter                                        | Conditions  |     | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------------------|-------------|-----|-----|-----|-----|------|
| <b>Per transistor</b> |                                                  |             |     |     |     |     |      |
| $R_{th(j-a)}$         | thermal resistance from junction to ambient      | in free air | [1] | -   | -   | 338 | K/W  |
|                       |                                                  |             | [2] | -   | -   | 219 | K/W  |
|                       |                                                  |             | [3] | -   | -   | 236 | K/W  |
|                       |                                                  |             | [4] | -   | -   | 179 | K/W  |
|                       |                                                  |             | [5] | -   | -   | 278 | K/W  |
|                       |                                                  |             | [6] | -   | -   | 164 | K/W  |
|                       |                                                  |             | [7] | -   | -   | 179 | K/W  |
|                       |                                                  |             | [8] | -   | -   | 86  | K/W  |
| $R_{th(j-sp)}$        | thermal resistance from junction to solder point |             |     | -   | -   | 30  | K/W  |

## NXP Semiconductors

## PBSS5160PAP

60 V, 1 A PNP/PNP low VCEsat (BISS) transistor

| Symbol            | Parameter                                         | Conditions  |     | Min | Typ | Max | Unit |
|-------------------|---------------------------------------------------|-------------|-----|-----|-----|-----|------|
| <b>Per device</b> |                                                   |             |     |     |     |     |      |
| $R_{th(j-a)}$     | thermal resistance<br>from junction to<br>ambient | in free air | [1] | -   | -   | 245 | K/W  |
|                   |                                                   |             | [2] | -   | -   | 160 | K/W  |
|                   |                                                   |             | [3] | -   | -   | 171 | K/W  |
|                   |                                                   |             | [4] | -   | -   | 130 | K/W  |
|                   |                                                   |             | [5] | -   | -   | 202 | K/W  |
|                   |                                                   |             | [6] | -   | -   | 120 | K/W  |
|                   |                                                   |             | [7] | -   | -   | 130 | K/W  |
|                   |                                                   |             | [8] | -   | -   | 63  | K/W  |

[1] Device mounted on an FR4 PCB, single-sided 35  $\mu$ m copper strip line, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided 35  $\mu$ m copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

[3] Device mounted on 4-layer PCB 35  $\mu$ m copper strip line, tin-plated and standard footprint.

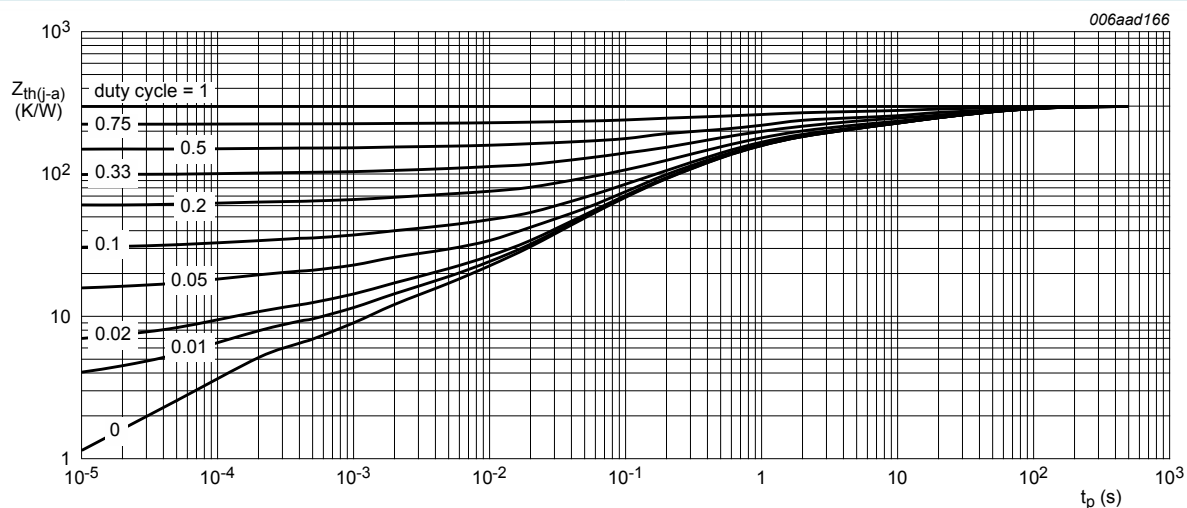
[4] Device mounted on 4-layer PCB 35  $\mu$ m copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

[5] Device mounted on an FR4 PCB, single-sided 70  $\mu$ m copper strip line, tin-plated and standard footprint.

[6] Device mounted on an FR4 PCB, single-sided 70  $\mu$ m copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

[7] Device mounted on 4-layer PCB 70  $\mu$ m copper strip line, tin-plated and standard footprint.

[8] Device mounted on 4-layer PCB 70  $\mu$ m copper strip line, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.



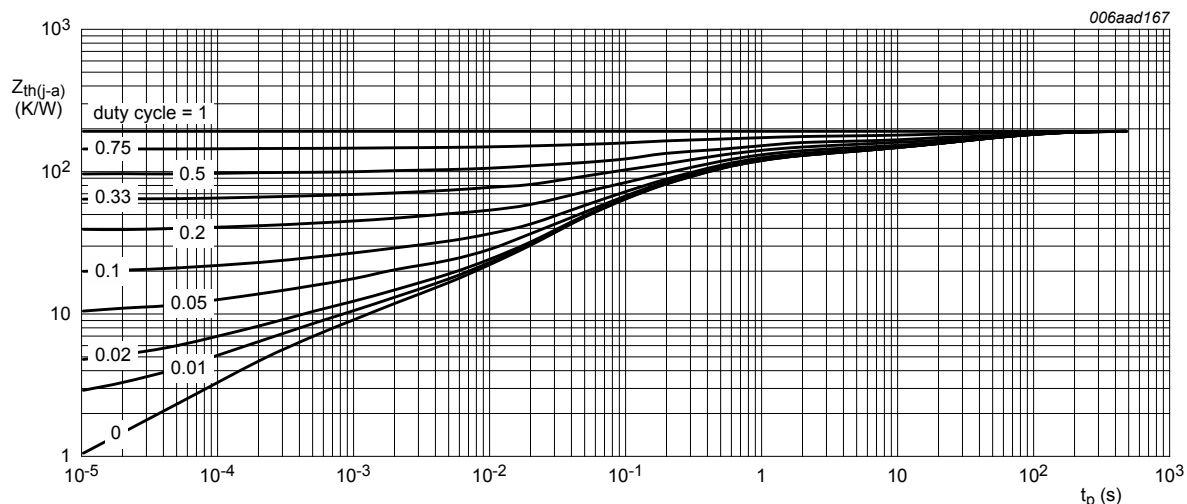
FR4 PCB 35  $\mu$ m, standard footprint

**Fig. 2. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

NXP Semiconductors

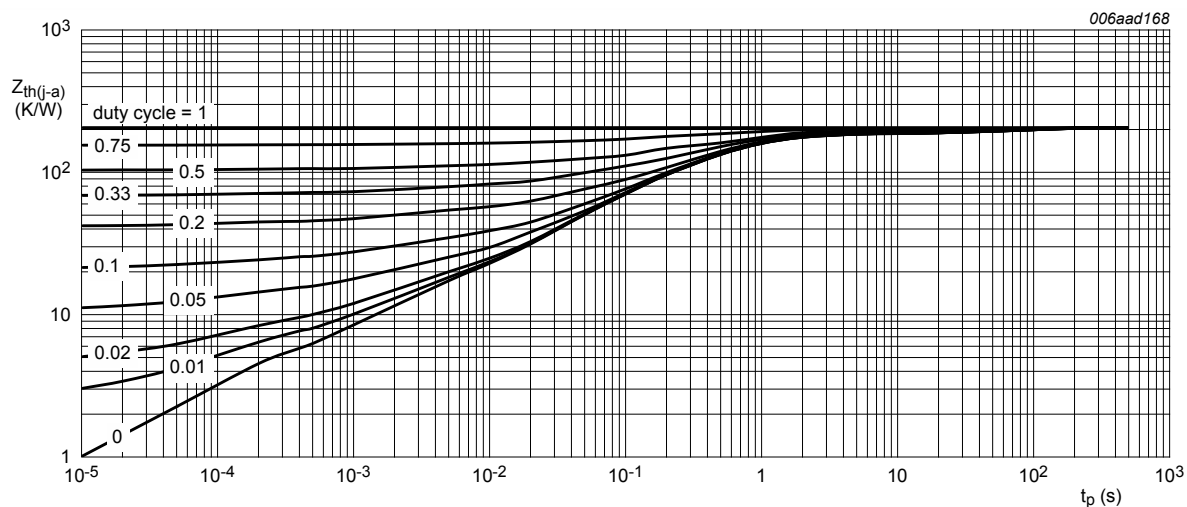
**PBSS5160PAP**

60 V, 1 A PNP/PNP low VCEsat (BISS) transistor



FR4 PCB 35  $\mu$ m, mounting pad for collector 1 cm<sup>2</sup>

**Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



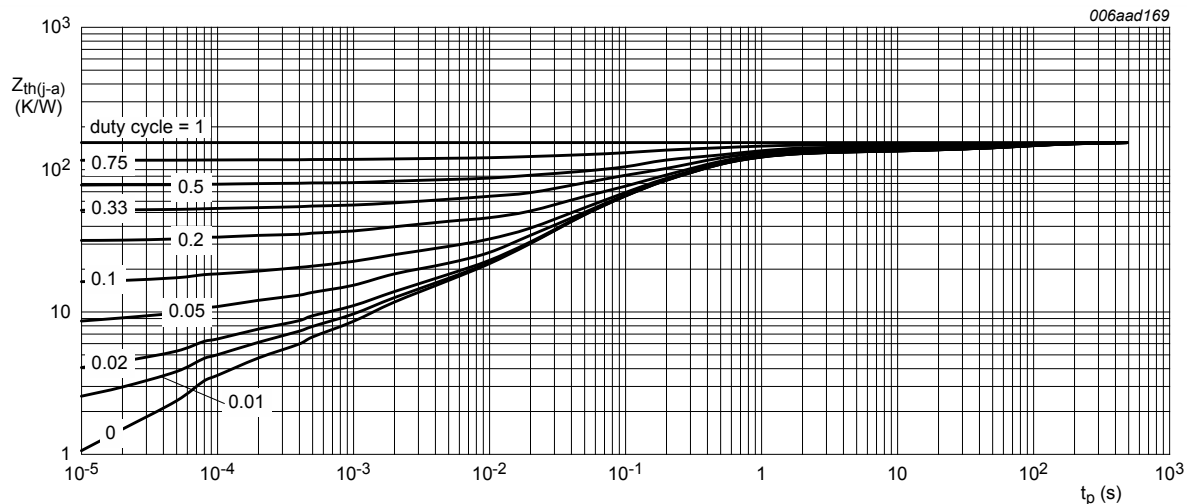
4-layer PCB 35  $\mu$ m, standard footprint

**Fig. 4. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

NXP Semiconductors

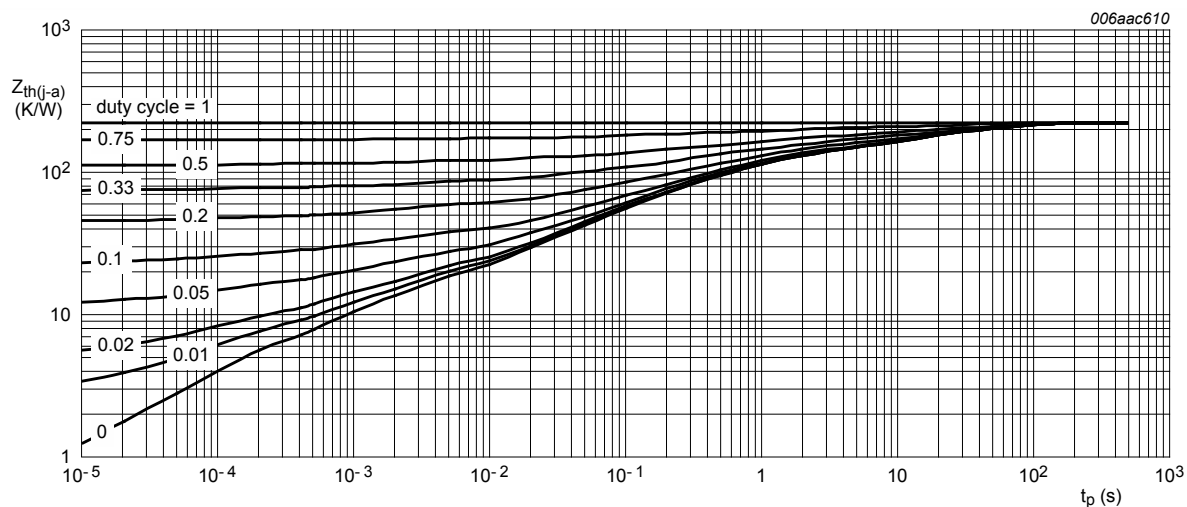
**PBSS5160PAP**

60 V, 1 A PNP/PPN low VCEsat (BISS) transistor



4-layer PCB 35  $\mu\text{m}$ , mounting pad for collector 1  $\text{cm}^2$

**Fig. 5. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



FR4 PCB 70  $\mu\text{m}$ , standard footprint

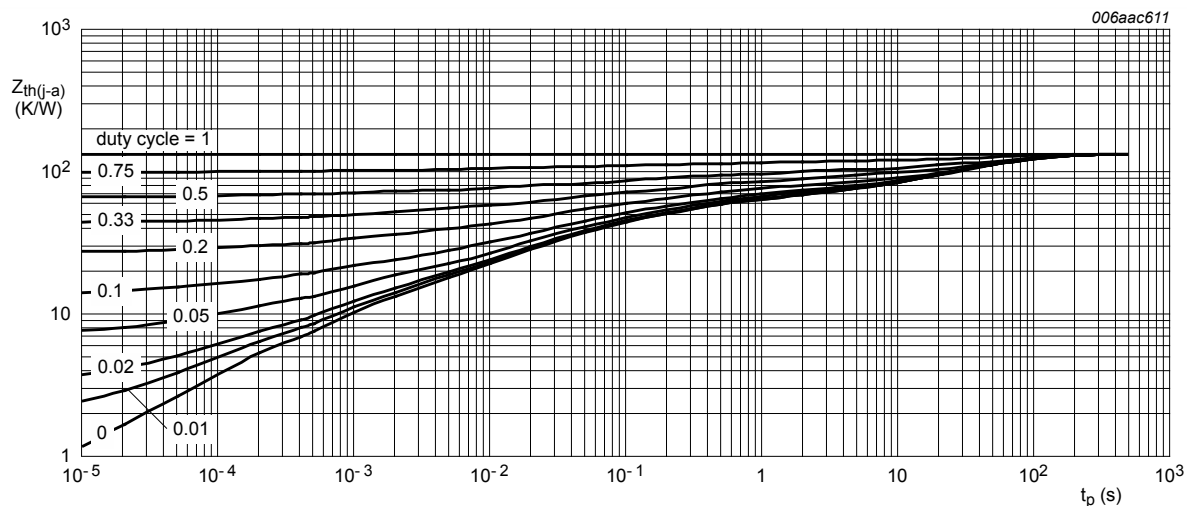
**Fig. 6. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



NXP Semiconductors

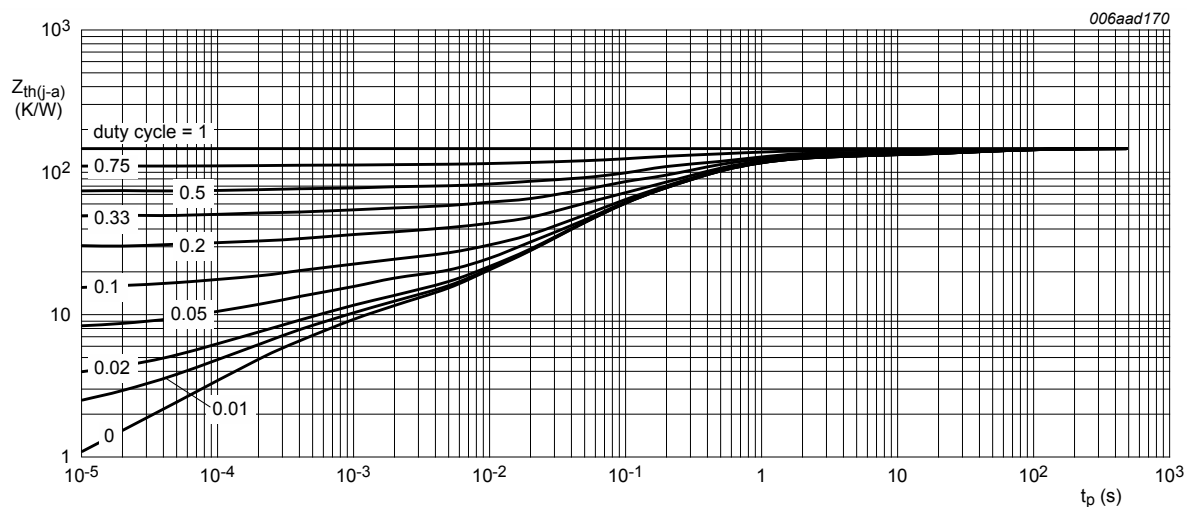
**PBSS5160PAP**

60 V, 1 A PNP/PPN low VCEsat (BISS) transistor



FR4 PCB 70  $\mu$ m, mounting pad for collector 1 cm<sup>2</sup>

**Fig. 7. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



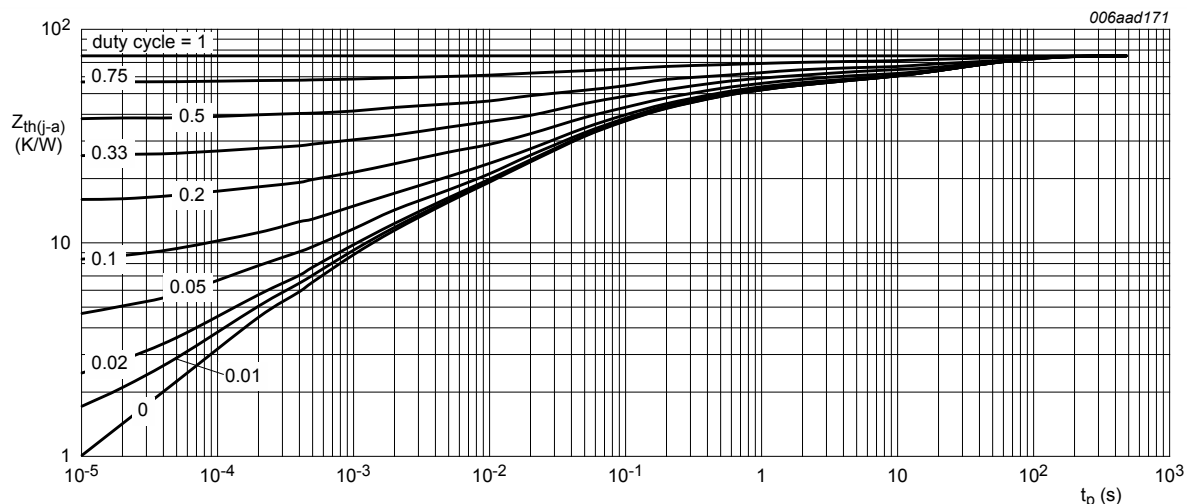
4-layer PCB 70  $\mu$ m, standard footprint

**Fig. 8. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## NXP Semiconductors

## PBSS5160PAP

60 V, 1 A PNP/2PNP low VCEsat (BISS) transistor



4-layer PCB 70  $\mu\text{m}$ , mounting pad for collector 1  $\text{cm}^2$

**Fig. 9. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 10. Characteristics

**Table 7. Characteristics**

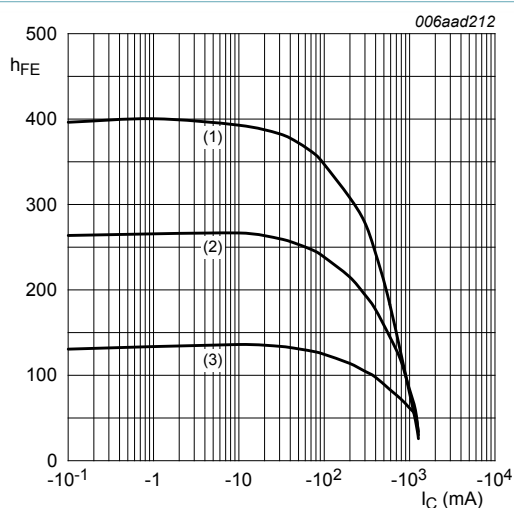
| Symbol                | Parameter                               | Conditions                                                                                                                                                                                 | Min | Typ  | Max  | Unit          |
|-----------------------|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|---------------|
| <b>Per transistor</b> |                                         |                                                                                                                                                                                            |     |      |      |               |
| $I_{\text{CBO}}$      | collector-base cut-off current          | $V_{\text{CB}} = -48 \text{ V}; I_{\text{E}} = 0 \text{ A}; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$                                                                                  | -   | -    | -100 | nA            |
|                       |                                         | $V_{\text{CB}} = -48 \text{ V}; I_{\text{E}} = 0 \text{ A}; T_{\text{j}} = 150 \text{ }^{\circ}\text{C}$                                                                                   | -   | -    | -50  | $\mu\text{A}$ |
| $I_{\text{EBO}}$      | emitter-base cut-off current            | $V_{\text{EB}} = -5 \text{ V}; I_{\text{C}} = 0 \text{ A}; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$                                                                                   | -   | -    | -100 | nA            |
| $h_{\text{FE}}$       | DC current gain                         | $V_{\text{CE}} = -2 \text{ V}; I_{\text{C}} = -100 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$  | 170 | 245  | -    |               |
|                       |                                         | $V_{\text{CE}} = -2 \text{ V}; I_{\text{C}} = -500 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$  | 120 | 170  | -    |               |
|                       |                                         | $V_{\text{CE}} = -2 \text{ V}; I_{\text{C}} = -1 \text{ A}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$     | 70  | 100  | -    |               |
| $V_{\text{CEsat}}$    | collector-emitter saturation voltage    | $I_{\text{C}} = -500 \text{ mA}; I_{\text{B}} = -50 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$ | -   | -125 | -180 | mV            |
|                       |                                         | $I_{\text{C}} = -1 \text{ A}; I_{\text{B}} = -50 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$    | -   | -390 | -550 | mV            |
|                       |                                         | $I_{\text{C}} = -1 \text{ A}; I_{\text{B}} = -100 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$   | -   | -240 | -340 | mV            |
| $R_{\text{CEsat}}$    | collector-emitter saturation resistance | $I_{\text{C}} = -0.5 \text{ A}; I_{\text{B}} = -50 \text{ mA}; \text{pulsed}; t_{\text{p}} \leq 300 \text{ } \mu\text{s}; \delta \leq 0.02; T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$  | -   | -    | 360  | m $\Omega$    |

## NXP Semiconductors

## PBSS5160PAP

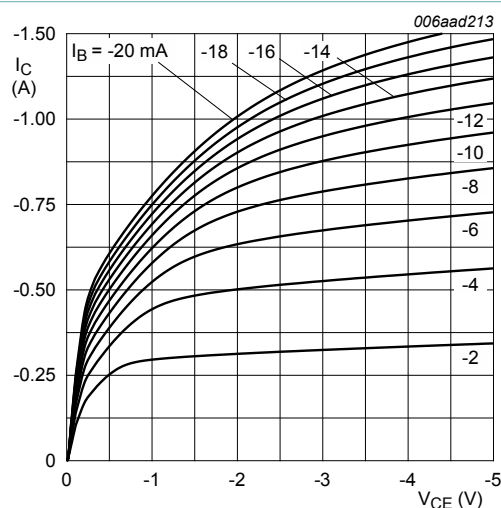
60 V, 1 A PNP/PNP low VCEsat (BISS) transistor

| Symbol      | Parameter                       | Conditions                                                                                                                                    | Min | Typ | Max  | Unit |
|-------------|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| $V_{BEsat}$ | base-emitter saturation voltage | $I_C = -500 \text{ mA}$ ; $I_B = -50 \text{ mA}$ ; pulsed;<br>$t_p \leq 300 \mu\text{s}$ ; $\delta \leq 0.02$ ; $T_{amb} = 25^\circ\text{C}$  | -   | -   | -1   | V    |
|             |                                 | $I_C = -1 \text{ A}$ ; $I_B = -50 \text{ mA}$ ; $T_{amb} = 25^\circ\text{C}$                                                                  | -   | -   | -1   | V    |
|             |                                 | $I_C = -1 \text{ A}$ ; $I_B = -100 \text{ mA}$ ; pulsed;<br>$t_p \leq 300 \mu\text{s}$ ; $\delta \leq 0.02$ ; $T_{amb} = 25^\circ\text{C}$    | -   | -   | -1.1 | V    |
| $V_{BEon}$  | base-emitter turn-on voltage    | $V_{CE} = -2 \text{ V}$ ; $I_C = -0.5 \text{ A}$ ; pulsed;<br>$t_p \leq 300 \mu\text{s}$ ; $\delta \leq 0.02$ ; $T_{amb} = 25^\circ\text{C}$  | -   | -   | -0.9 | V    |
| $t_d$       | delay time                      | $V_{CC} = -10 \text{ V}$ ; $I_C = -0.5 \text{ A}$ ; $I_{Bon} = -25 \text{ mA}$ ;<br>$I_{Boff} = 25 \text{ mA}$ ; $T_{amb} = 25^\circ\text{C}$ | -   | 15  | -    | ns   |
| $t_r$       | rise time                       |                                                                                                                                               | -   | 40  | -    | ns   |
| $t_{on}$    | turn-on time                    |                                                                                                                                               | -   | 55  | -    | ns   |
| $t_s$       | storage time                    |                                                                                                                                               | -   | 95  | -    | ns   |
| $t_f$       | fall time                       |                                                                                                                                               | -   | 40  | -    | ns   |
| $t_{off}$   | turn-off time                   |                                                                                                                                               | -   | 135 | -    | ns   |
| $f_T$       | transition frequency            | $V_{CE} = -10 \text{ V}$ ; $I_C = -50 \text{ mA}$ ; $f = 100 \text{ MHz}$ ;<br>$T_{amb} = 25^\circ\text{C}$                                   | 65  | 125 | -    | MHz  |
| $C_c$       | collector capacitance           | $V_{CB} = -10 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $i_e = 0 \text{ A}$ ;<br>$f = 1 \text{ MHz}$ ; $T_{amb} = 25^\circ\text{C}$                  | -   | 9.5 | 13   | pF   |



$V_{CE} = -2 \text{ V}$   
(1)  $T_{amb} = 100^\circ\text{C}$   
(2)  $T_{amb} = 25^\circ\text{C}$   
(3)  $T_{amb} = -55^\circ\text{C}$

**Fig. 10. DC current gain as a function of collector current; typical values**



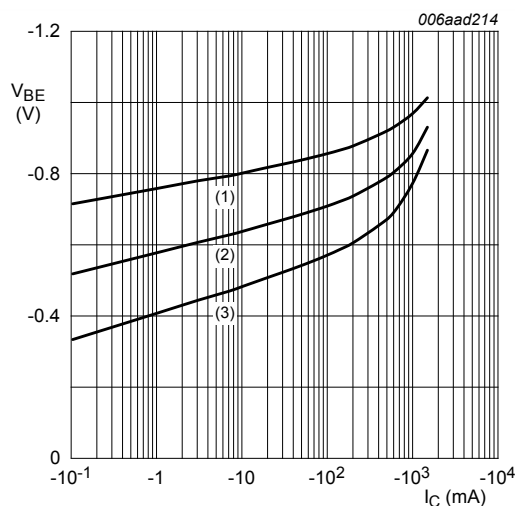
$T_{amb} = 25^\circ\text{C}$

**Fig. 11. Collector current as a function of collector-emitter voltage; typical values**

## NXP Semiconductors

## PBSS5160PAP

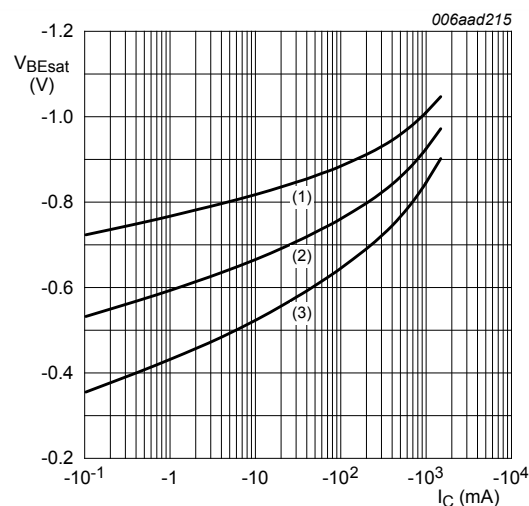
60 V, 1 A PNP/PNP low VCEsat (BISS) transistor



$V_{CE} = -2 \text{ V}$

- (1)  $T_{amb} = -55 \text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$

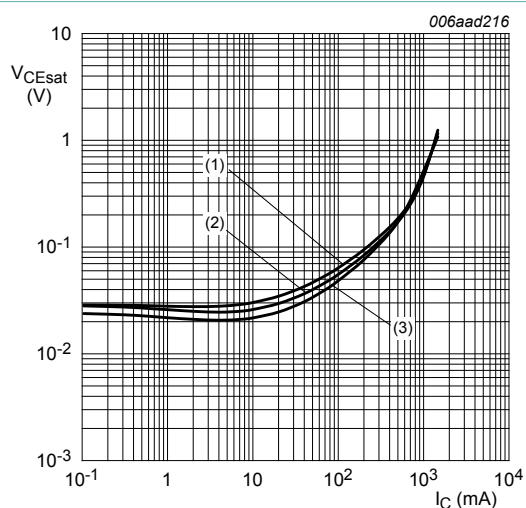
**Fig. 12. Base-emitter voltage as a function of collector current; typical values**



$I_C/I_B = 20$

- (1)  $T_{amb} = -55 \text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$

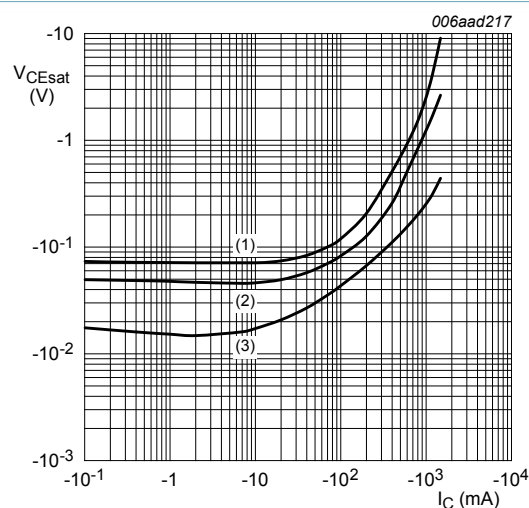
**Fig. 13. Base-emitter saturation voltage as a function of collector current; typical values**



$I_C/I_B = 20$

- (1)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = -55 \text{ }^{\circ}\text{C}$

**Fig. 14. Collector-emitter saturation voltage as a function of collector current; typical values**



$T_{amb} = 25 \text{ }^{\circ}\text{C}$

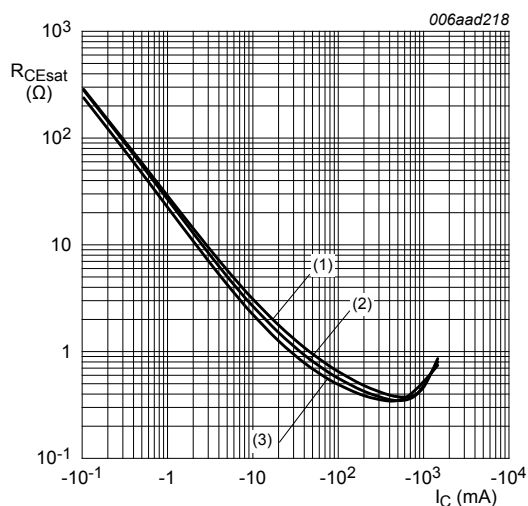
- (1)  $I_C/I_B = 100$
- (2)  $I_C/I_B = 50$
- (3)  $I_C/I_B = 10$

**Fig. 15. Collector-emitter saturation voltage as a function of collector current; typical values**

## NXP Semiconductors

## PBSS5160PAP

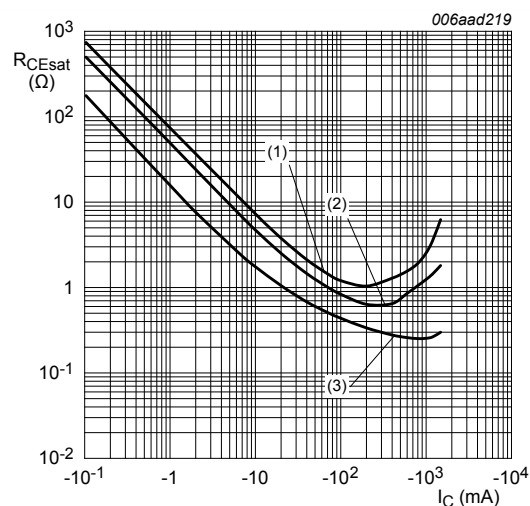
60 V, 1 A PNP/PNP low VCEsat (BISS) transistor



$$I_C/I_B = 20$$

- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = -55\text{ }^{\circ}\text{C}$

**Fig. 16. Collector-emitter saturation resistance as a function of collector current; typical values**



$$T_{amb} = 25\text{ }^{\circ}\text{C}$$

- (1)  $I_C/I_B = 100$
- (2)  $I_C/I_B = 50$
- (3)  $I_C/I_B = 10$

**Fig. 17. Collector-emitter saturation resistance as a function of collector current; typical values**

## NXP Semiconductors

## PBSS5160PAP

60 V, 1 A PNP/PNP low VCEsat (BISS) transistor

### 11. Test information

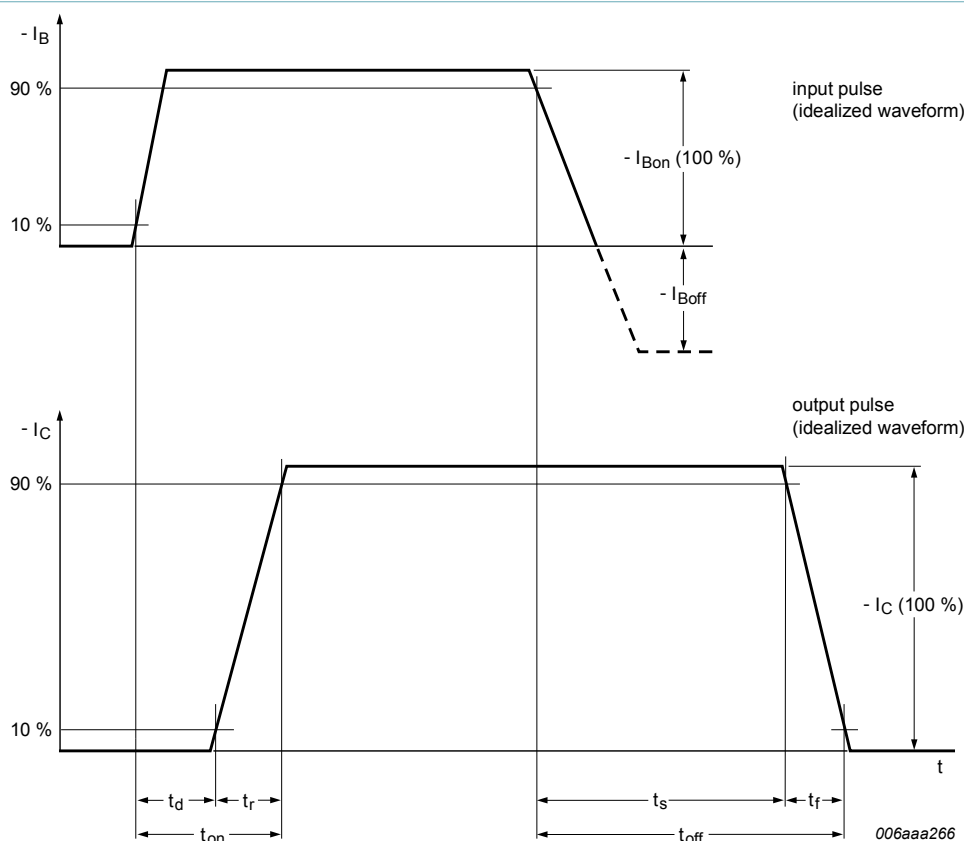


Fig. 18. BISS transistor switching time definition

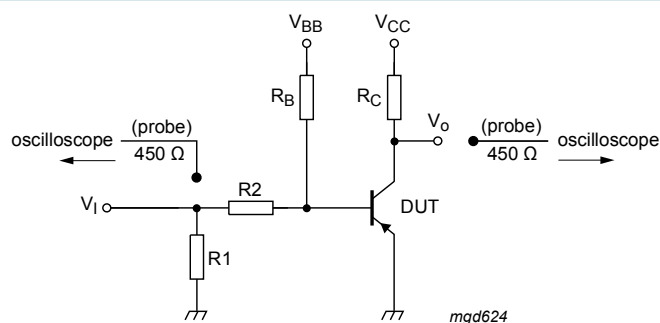


Fig. 19. Test circuit for switching times

#### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## NXP Semiconductors

## PBSS5160PAP

60 V, 1 A PNP/PNP low VCEsat (BISS) transistor

### 12. Package outline

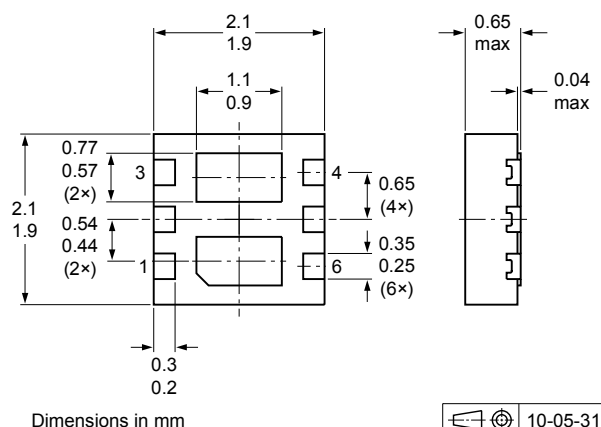


Fig. 20. Package outline DFN2020-6 (SOT1118)

### 13. Soldering

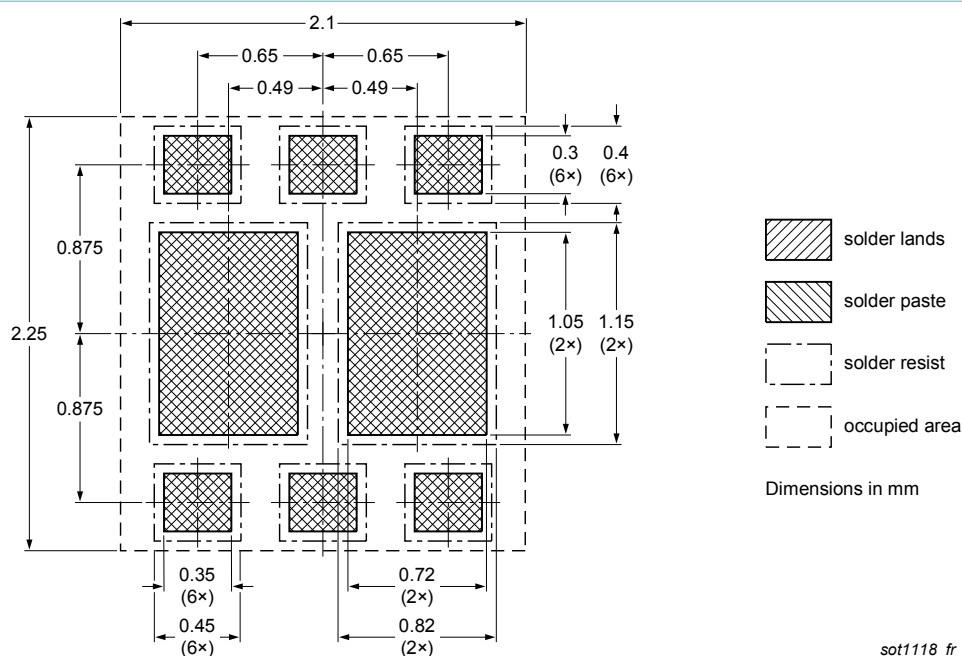


Fig. 21. Reflow soldering footprint for DFN2020-6 (SOT1118)

### 14. Revision history

Table 8. Revision history

| Data sheet ID   | Release date | Data sheet status  | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|------------|
| PBSS5160PAP v.1 | 20130123     | Product data sheet | -             | -          |

## NXP Semiconductors

## PBSS5160PAP

### 60 V, 1 A PNP/PNP low VCEsat (BISS) transistor

## 15. Legal information

### 15.1 Data sheet status

| Document status [1][2]         | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Preview** — The document is a preview version only. The document is still subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 15.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.



## NXP Semiconductors

## PBSS5160PAP

60 V, 1 A PNP/PNP low VCEsat (BISS) transistor

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**Adelante, Bitport, Bitsound, CoolFlux, CoReUse, DESFire, EZ-HV, FabKey, GreenChip, HiPerSmart, HITAG, I<sup>2</sup>C-bus logo, ICODE, I-CODE, ITEC, Labelution, MIFARE, MIFARE Plus, MIFARE Ultralight, MoReUse, QLPAK, Silicon Tuner, SiliconMAX, SmartXA, STARplug, TOPFET, TrenchMOS, TriMedia and UCODE** — are trademarks of NXP B.V.

**HD Radio** and **HD Radio** logo — are trademarks of iBiquity Digital Corporation.

## NXP Semiconductors

## PBSS5160PAP

60 V, 1 A PNP/PNP low VCEsat (BISS) transistor

## 16. Contents

|      |                               |    |
|------|-------------------------------|----|
| 1    | General description .....     | 1  |
| 2    | Features and benefits .....   | 1  |
| 3    | Applications .....            | 1  |
| 4    | Quick reference data .....    | 1  |
| 5    | Pinning information .....     | 2  |
| 6    | Ordering information .....    | 2  |
| 7    | Marking .....                 | 2  |
| 8    | Limiting values .....         | 2  |
| 9    | Thermal characteristics ..... | 4  |
| 10   | Characteristics .....         | 9  |
| 11   | Test information .....        | 13 |
| 11.1 | Quality information .....     |    |
| 12   | Package outline .....         | 14 |
| 13   | Soldering .....               | 14 |
| 14   | Revision history .....        | 14 |
| 15   | Legal information .....       | 15 |
| 15.1 | Data sheet status .....       | 15 |
| 15.2 | Definitions .....             | 15 |
| 15.3 | Disclaimers .....             | 15 |
| 15.4 | Trademarks .....              | 16 |

---

© NXP B.V. 2013. All rights reserved

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 23 January 2013

---