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# STY145N65M5

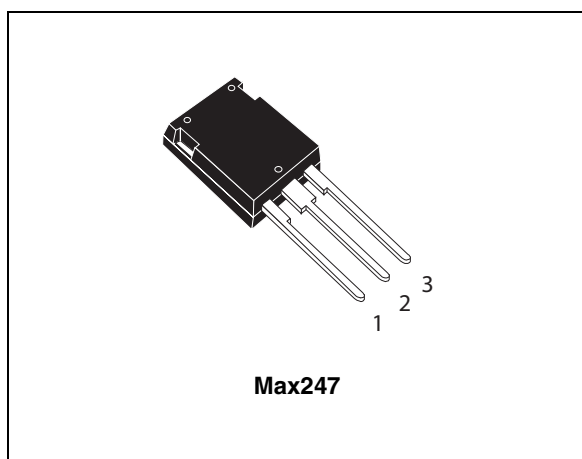
N-channel 650 V, 0.012  $\Omega$  typ., 138 A, MDmesh™ V Power MOSFET in Max247 package

Datasheet — preliminary data

## Features

Order code	V <sub>DSS</sub> @T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STY145N65M5	710 V	< 0.015 $\Omega$	138 A

- Max247 worldwide best R<sub>DS(on)</sub>
- Higher V<sub>DSS</sub> rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



## Applications

- Switching applications

## Description

The device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

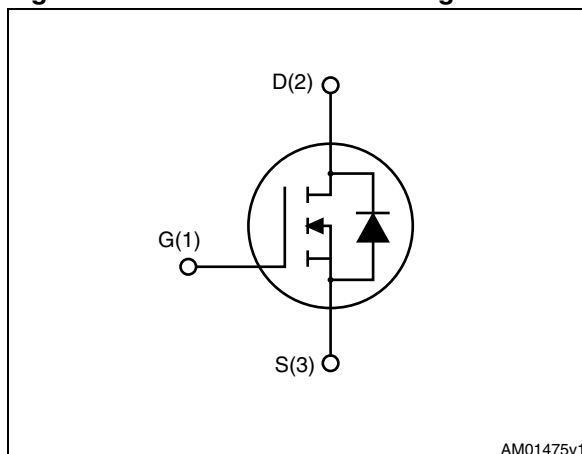


Table 1. Device summary

Order code	Marking	Package	Packaging
STY145N65M5	145N65M5	Max247	Tube

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## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>GS</sub>	Gate- source voltage	± 25	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	138	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	87	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	552	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	625	W
I <sub>AR</sub>	Max current during repetitive or single pulse avalanche (pulse width limited by T <sub>JMAX</sub> )	17	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25°C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50V)	2420	mJ
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	15	V/ns
T <sub>stg</sub>	Storage temperature	- 55 to 150	°C
T <sub>j</sub>	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area.

2. I<sub>SD</sub> ≤ 138 A, di/dt = 400 A/μs, V<sub>DD</sub> = 400 V, peak V<sub>DS</sub> < V<sub>(BR)DSS</sub>.

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.2	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max	30	°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300	°C

Electrical characteristics

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## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 69\text{ A}$		0.012	0.015	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	18500 413 11	-	pF pF pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }520\text{ V}$	-	1950	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related	$V_{GS} = 0, V_{DS} = 0\text{ to }520\text{ V}$	-	415	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	0.7	-	$\Omega$
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 520\text{ V}, I_D = 69\text{ A},$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )	-	414 114 164	-	nC nC nC

- $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

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Electrical characteristics

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 85\text{ A}$ ,		255		ns
$t_{r(v)}$	Voltage rise time	$R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$		11		ns
$t_{f(i)}$	Current fall time	(see <a href="#">Figure 16</a> )	-	82	-	ns
$t_{c(off)}$	Crossing time	(see <a href="#">Figure 19</a> )		88		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		138	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				552	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 138\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 138\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		568		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$ (see <a href="#">Figure 16</a> )	-	14.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			51		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 138\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		728		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	24.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 16</a> )		67		A

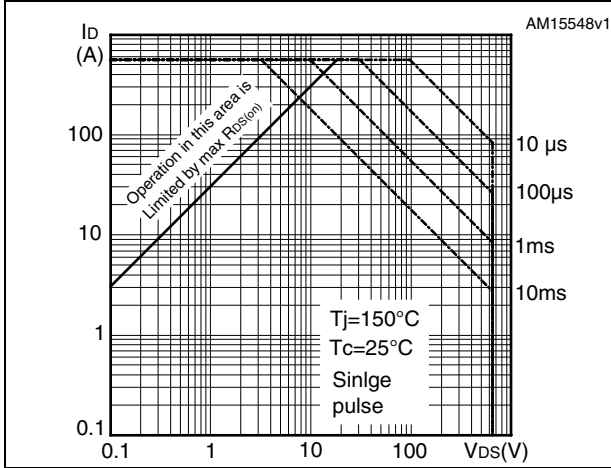
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Electrical characteristics**

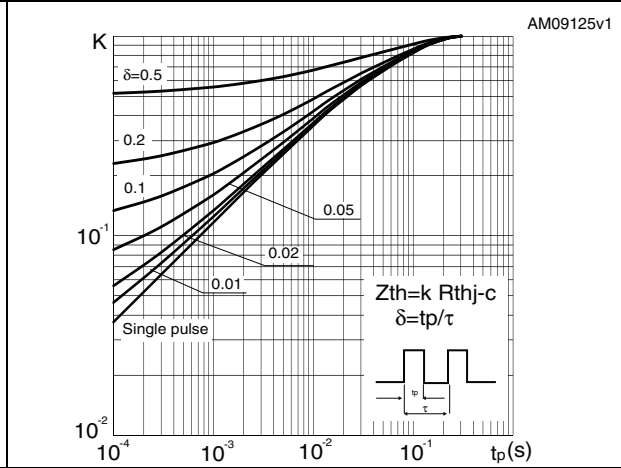
**STY145N65M5**

**2.1 Electrical characteristics (curves)**

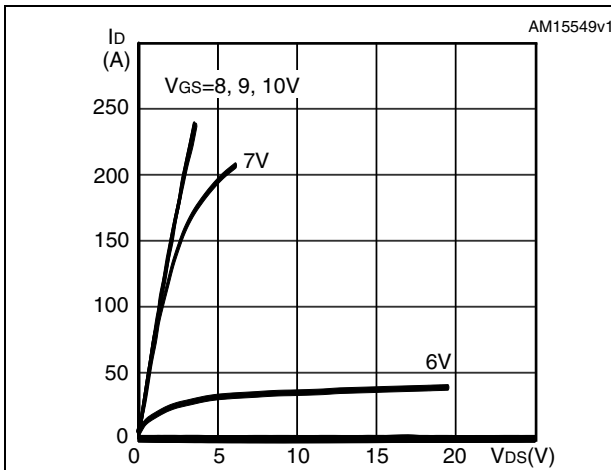
**Figure 2. Safe operating area**



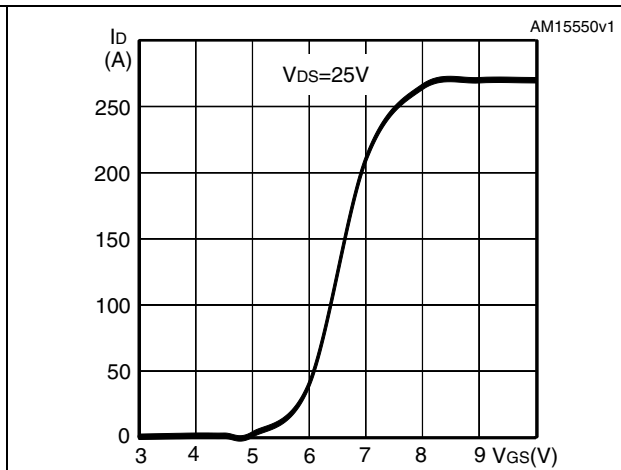
**Figure 3. Thermal impedance**



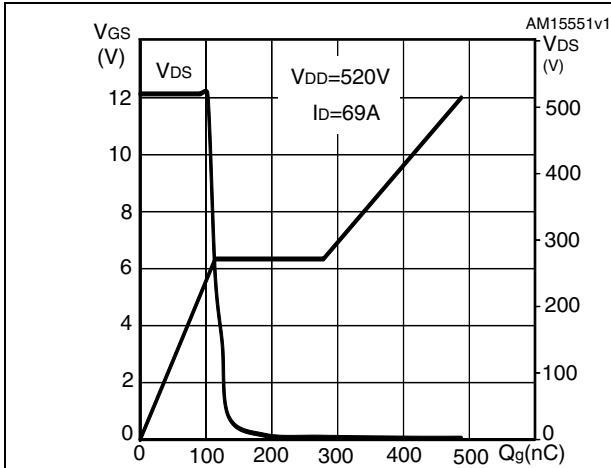
**Figure 4. Output characteristics**



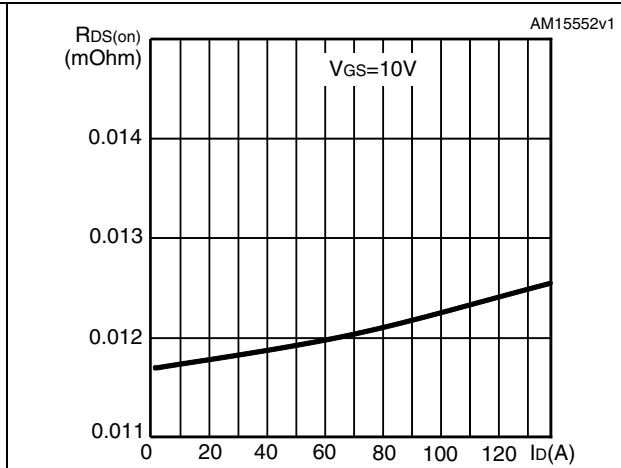
**Figure 5. Transfer characteristics**



**Figure 6. Gate charge vs gate-source voltage**



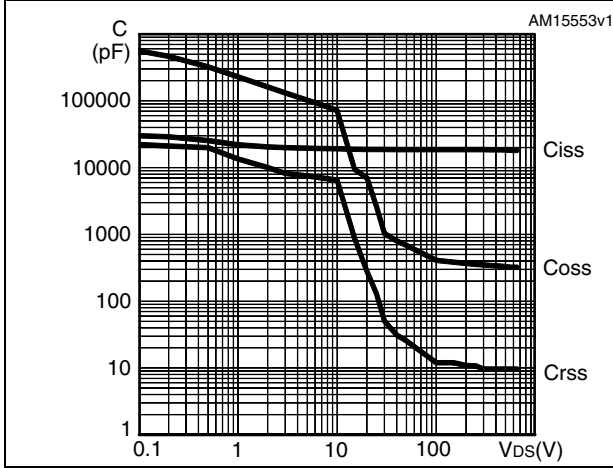
**Figure 7. Static drain-source on-resistance**



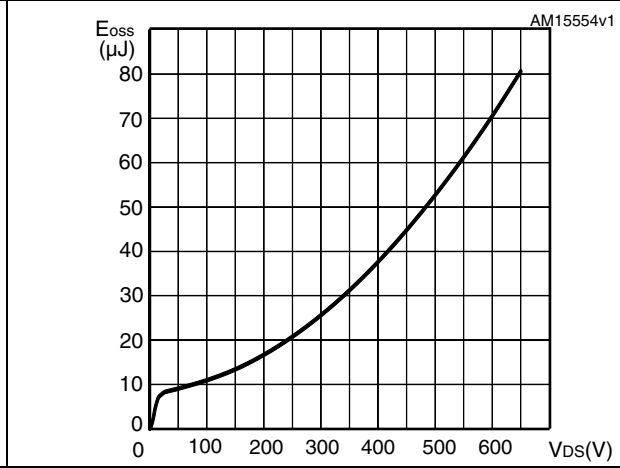
**STY145N65M5**

**Electrical characteristics**

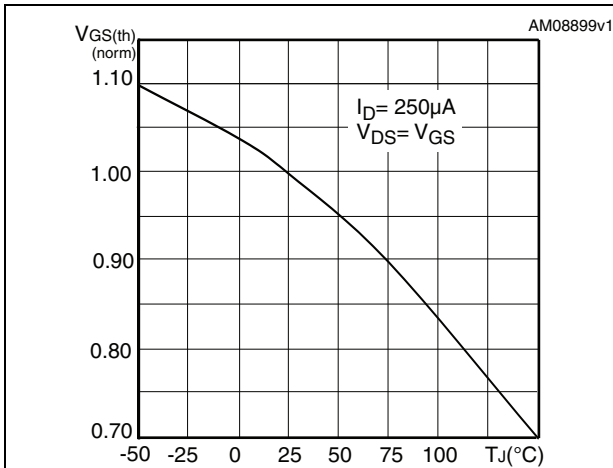
**Figure 8. Capacitance variations**



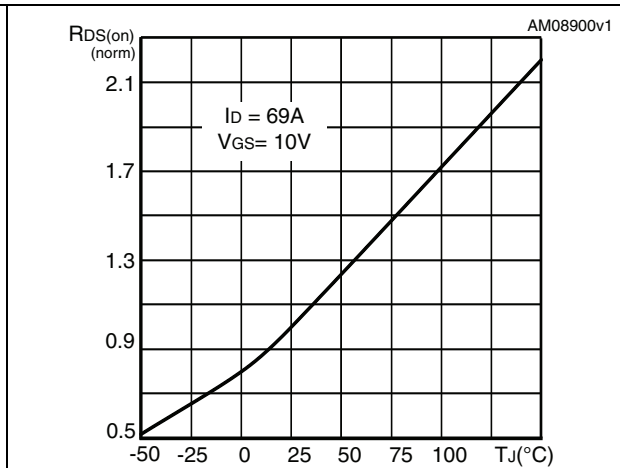
**Figure 9. Output capacitance stored energy**



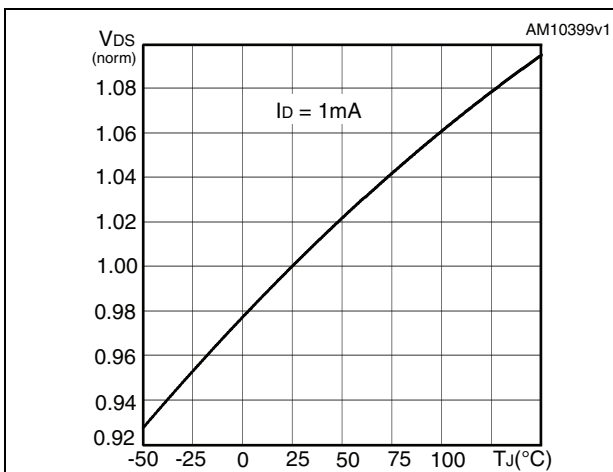
**Figure 10. Normalized gate threshold voltage vs temperature**



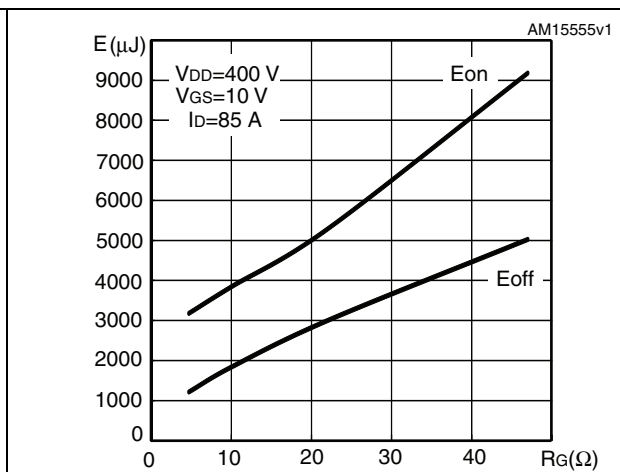
**Figure 11. Normalized on-resistance vs temperature**



**Figure 12. Normalized BVDS vs temperature**



**Figure 13. Switching losses vs gate resistance<sup>(1)</sup>**



1. Eon including reverse recovery of a SiC diode.



### 3 Test circuits

Figure 14. Switching times test circuit for resistive load

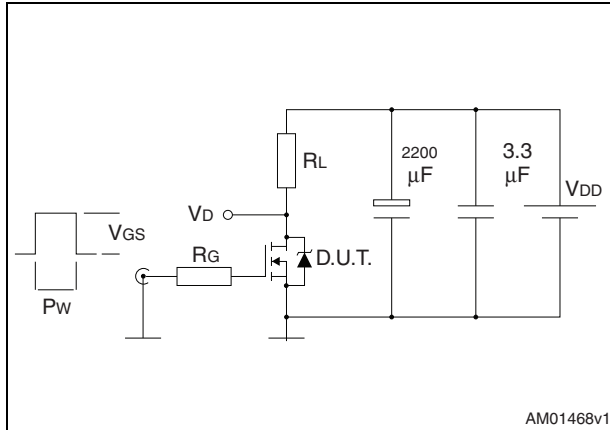


Figure 15. Gate charge test circuit

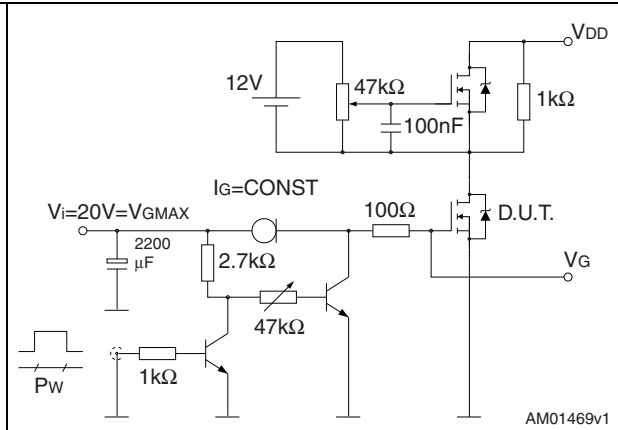


Figure 16. Test circuit for inductive load switching and diode recovery times

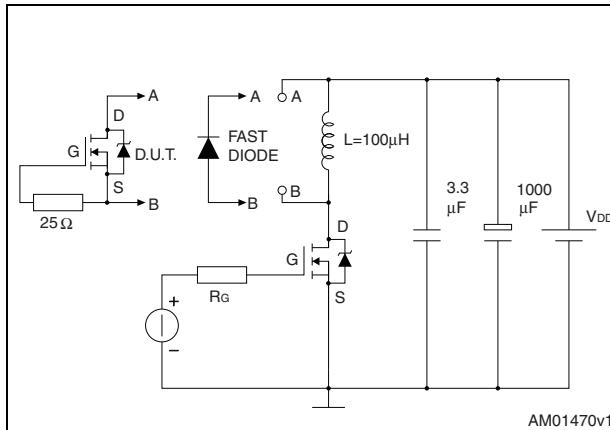


Figure 17. Unclamped inductive load test circuit

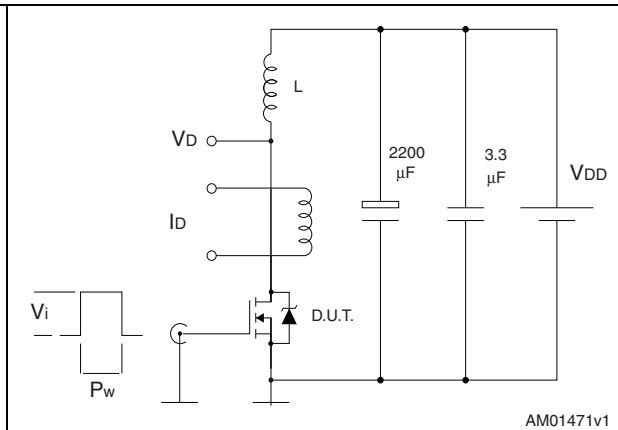


Figure 18. Unclamped inductive waveform

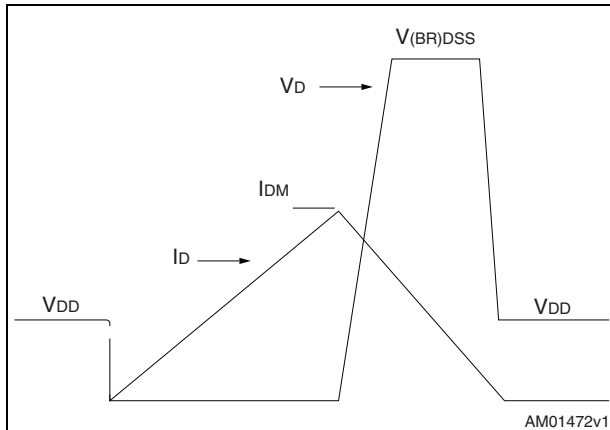
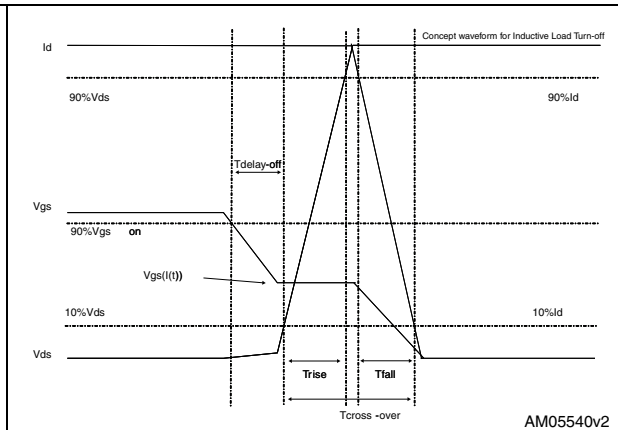


Figure 19. Switching time waveform



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Package mechanical data

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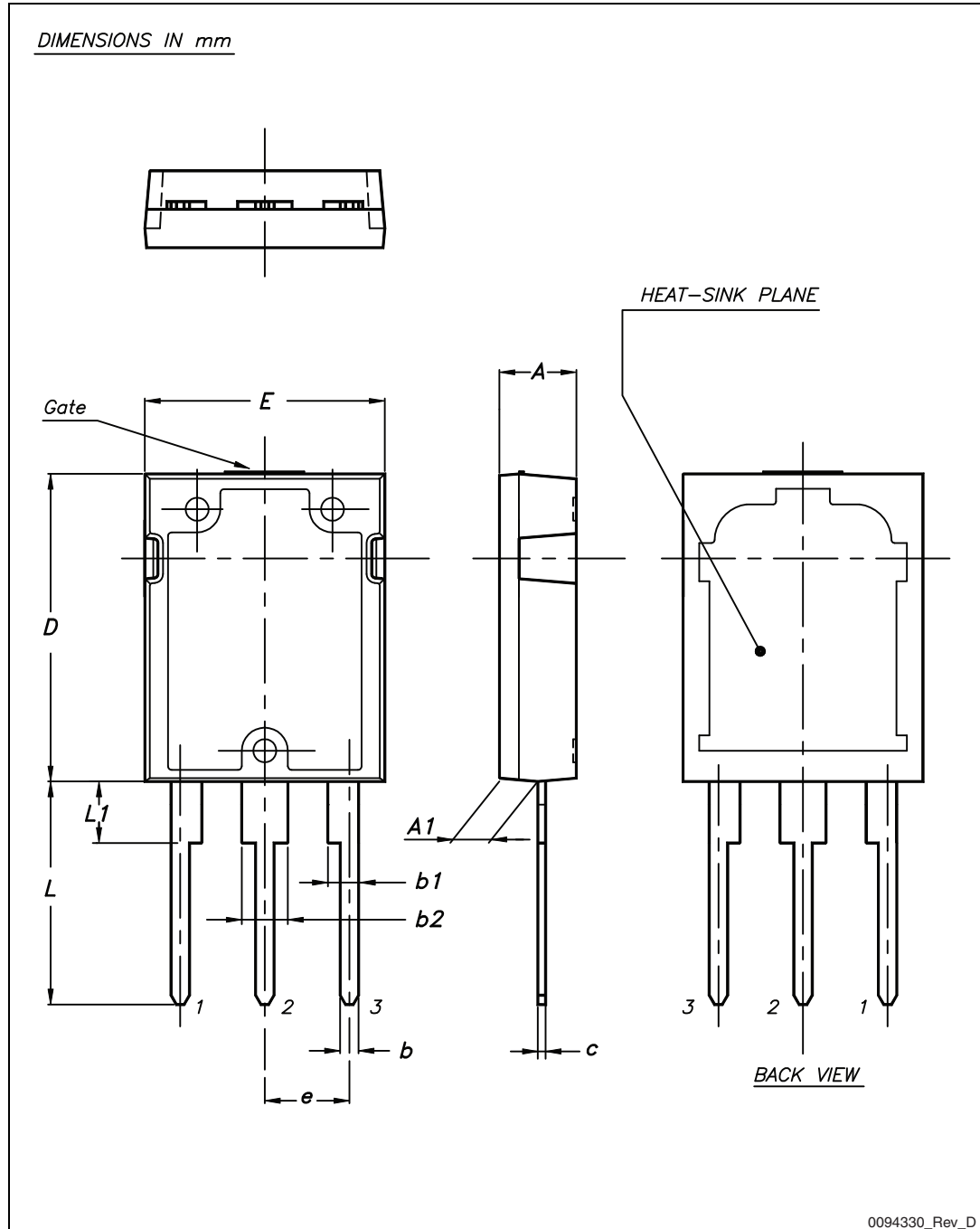
Table 8. Max247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.70		5.30
A1	2.20		2.60
b	1.00		1.40
b1	2.00		2.40
b2	3.00		3.40
c	0.40		0.80
D	19.70		20.30
e	5.35		5.55
E	15.30		15.90
L	14.20		15.20
L1	3.70		4.30

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**Package mechanical data**

**Figure 20. Max247 drawing**



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
25-Sep-2012	1	First release.
17-Jan-2013	2	– Modified: $I_{AR}$ and $E_{AS}$ values – Modified: typical values on <a href="#">Table 5</a> , <a href="#">6</a> and <a href="#">7</a>

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