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# BUK7Y21-40E

N-channel 40 V, 21 mΩ standard level MOSFET in LPAK56

7 May 2013

Product data sheet

## 1. General description

Standard level N-channel MOSFET in an LPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with  $V_{GS(th)}$  rating of greater than 1V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	33	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	45	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	-	17.8	21	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; V_{DS} = 32\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	-	3	-	nC



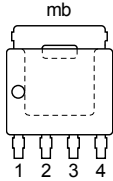
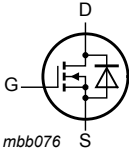
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### 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT669)</b></p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

### 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y21-40E	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

### 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Y21-40E	72140E

### 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}$ ; DC	-20	20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 1</a>	-	33	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 1</a>	-	23	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">Fig. 4</a>	-	132	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	45	W
$T_{stg}$	storage temperature		-55	175	°C

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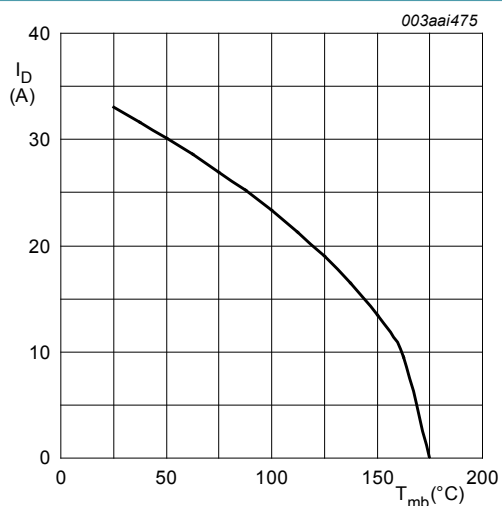
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Symbol	Parameter	Conditions	Min	Max	Unit
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	33	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	132	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 33\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; unclamped; <a href="#">Fig. 3</a>	[1][2]	-	12 mJ

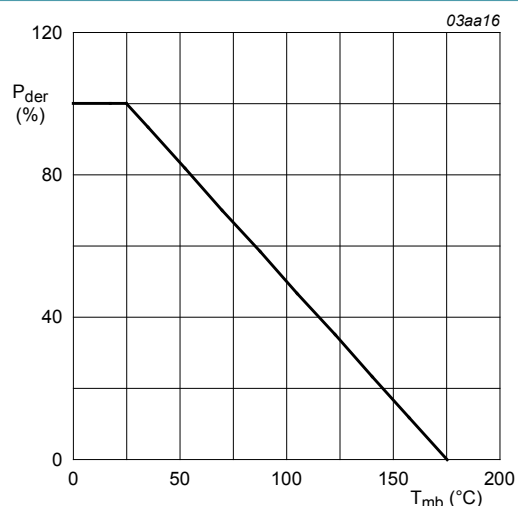
[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[2] Refer to application note AN10273 for further information.



**Fig. 1. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 10V$$



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

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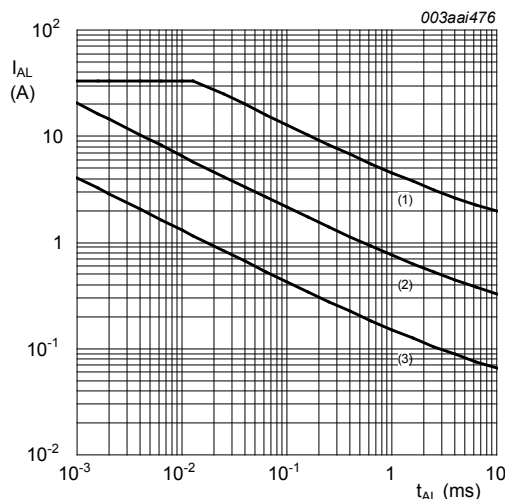


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (init)} = 25^{\circ}C$ ; (2)  $T_{j (init)} = 150^{\circ}C$ ; (3) Repetitive Avalanche

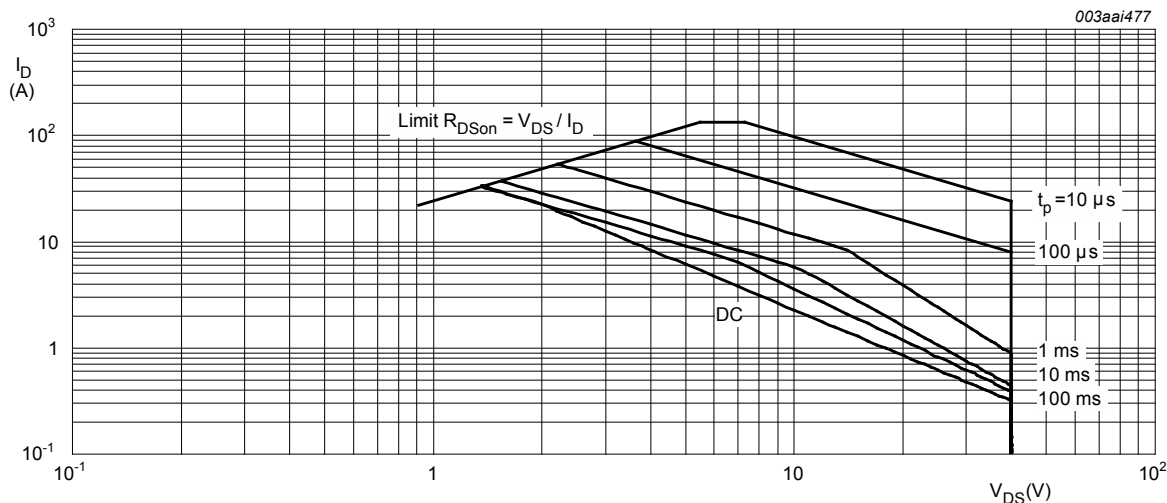


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

**9. Thermal characteristics**

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	3.33	K/W

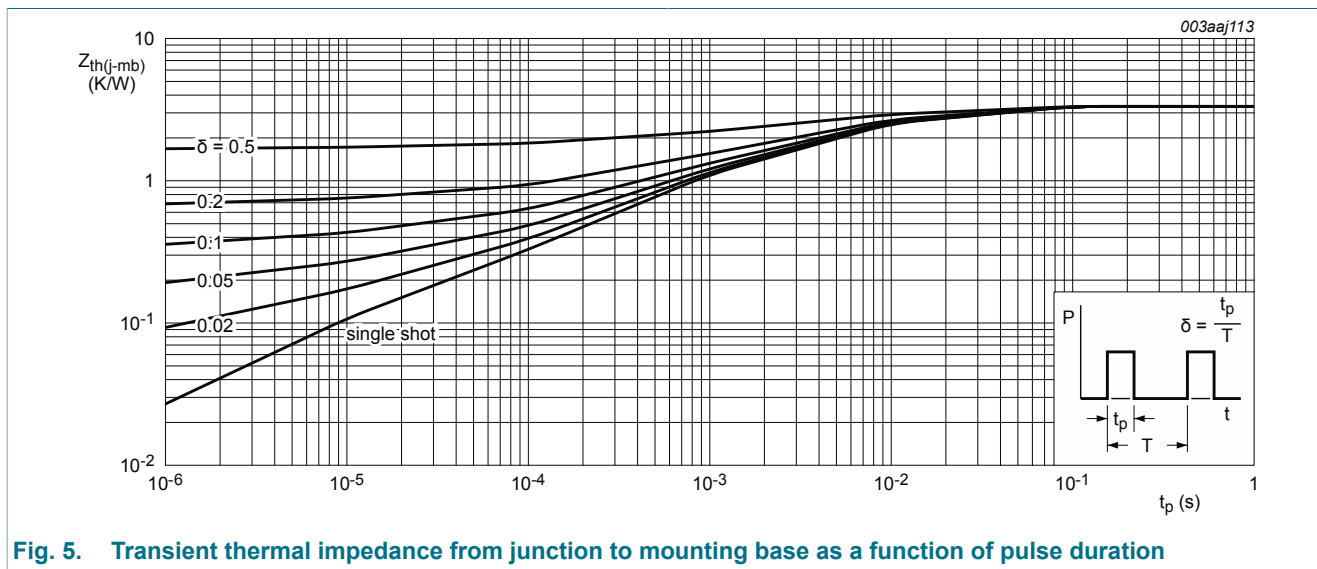


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

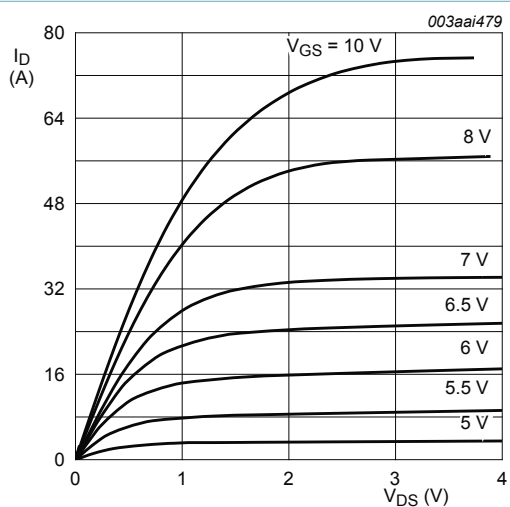
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	40	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -55 °C	36	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = 25 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>	2.4	3	4	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = -55 °C; <a href="#">Fig. 9</a>	-	-	4.5	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = 175 °C; <a href="#">Fig. 9</a>	1	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	0.01	1	μA
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 11</a>	-	17.8	21	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	-	-	41.4	mΩ
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	10	-	nC
Q <sub>GS</sub>	gate-source charge		-	2	-	nC
Q <sub>GD</sub>	gate-drain charge		-	3	-	nC

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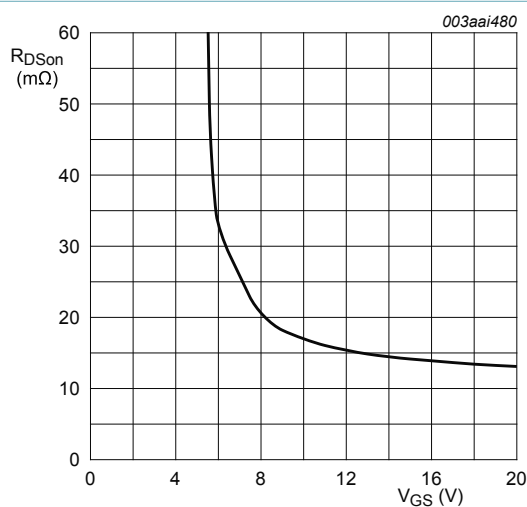
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	462	617	pF
$C_{oss}$	output capacitance		-	118	142	pF
$C_{rss}$	reverse transfer capacitance		-	90	123	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 3\text{ }^\Omega; V_{GS} = 10\text{ V}; R_{G(ext)} = 5\text{ }^\Omega; T_j = 25\text{ }^\circ\text{C}$	-	4.9	-	ns
$t_r$	rise time		-	6.4	-	ns
$t_{d(off)}$	turn-off delay time		-	6.7	-	ns
$t_f$	fall time		-	5.5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	0.88	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	14	-	ns
$Q_r$	recovered charge		-	8	-	nC



$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }^\mu\text{s}$

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



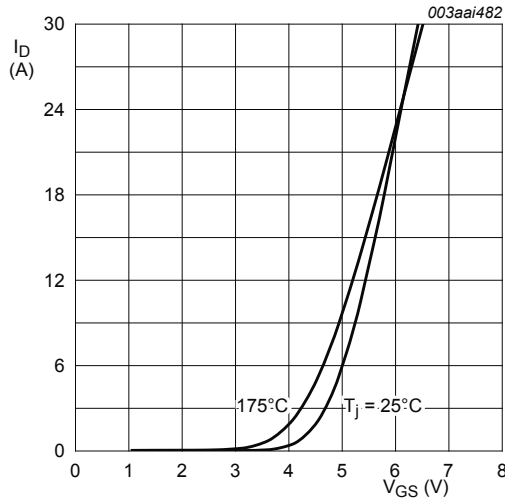
$T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{ A}$

**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

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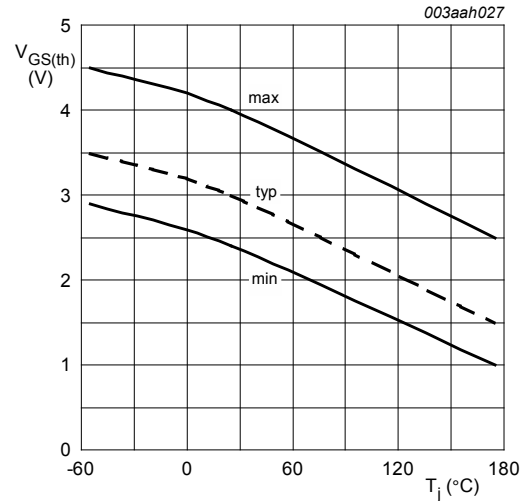
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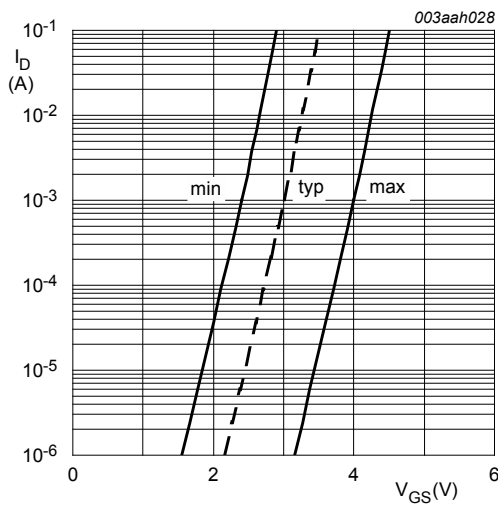
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10V$



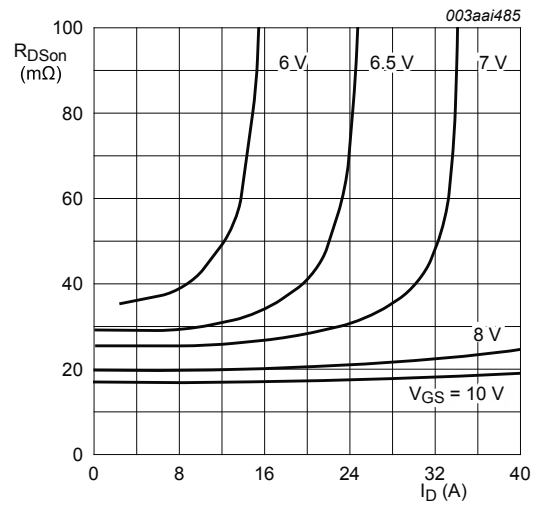
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$



**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ\text{C}; V_{DS} = 5V$



**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

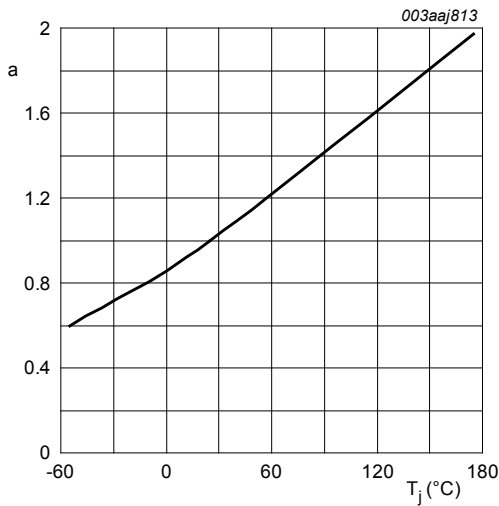
$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$



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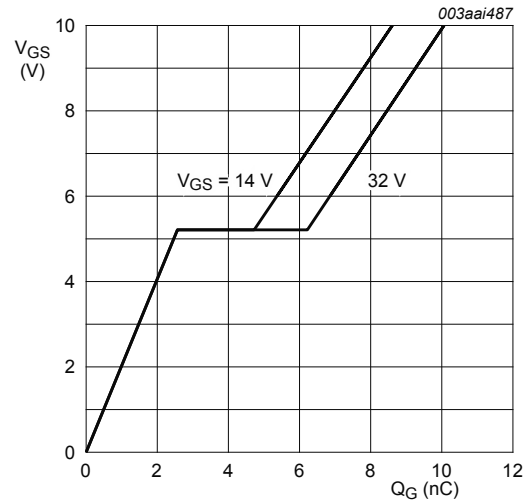
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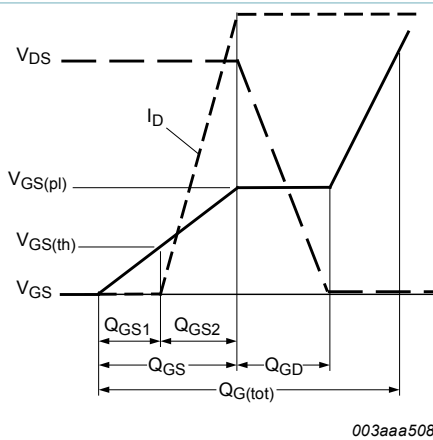
**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ C)}$$

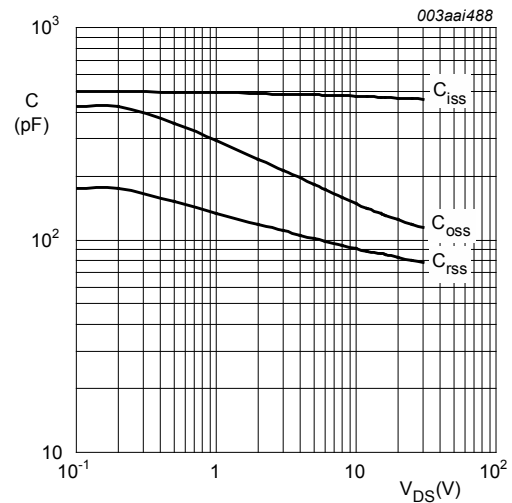


**Fig. 13. Gate-source voltage as a function of gate charge; typical values**

$T_j = 25^\circ C; I_D = 10A$



**Fig. 14. Gate charge waveform definitions**



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$V_{GS} = 0V; f = 1MHz$

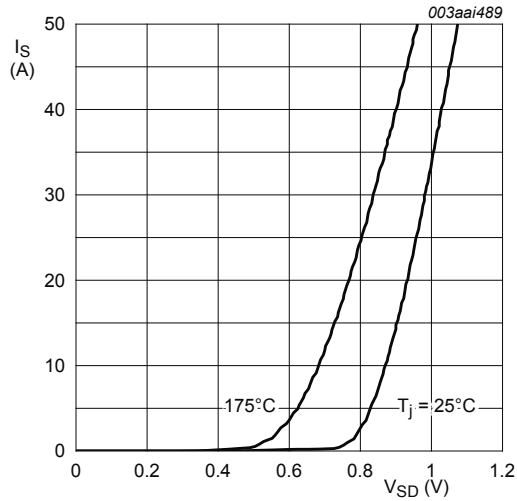


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

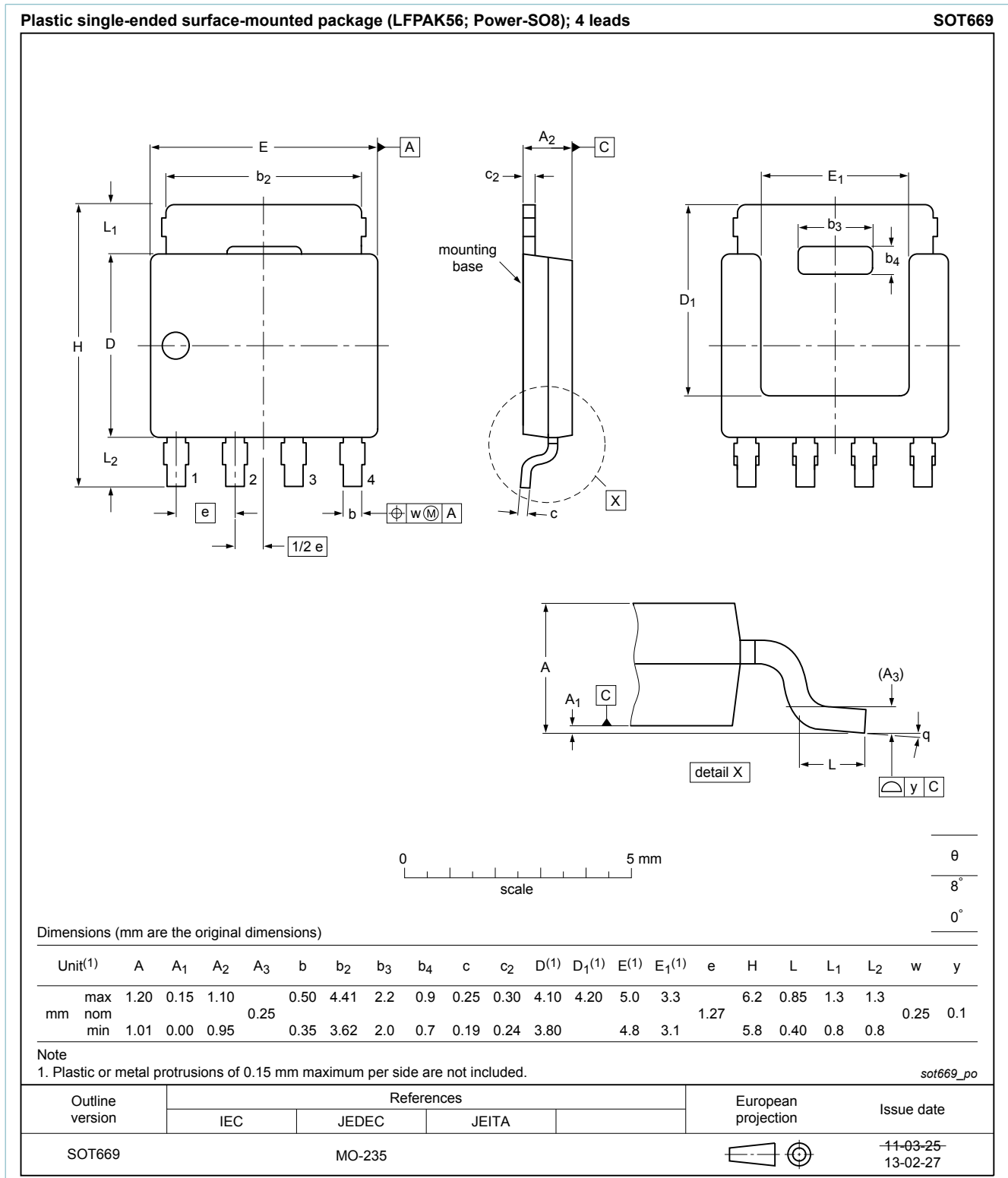
$$V_{GS} = 0V$$

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**11. Package outline**



**Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)**

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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