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[Vishay Semiconductor/Diodes Division](#)  
[VS-50WQ03FNPBF](#)

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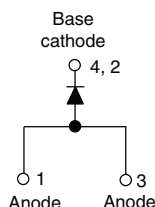
## VS-50WQ03FNPbF

Vishay Semiconductors

### Schottky Rectifier, 5.5 A



D-PAK (TO-252AA)



#### FEATURES

- Popular D-PAK outline
- Small foot print, surface mountable
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Compliant to RoHS Directive 2002/95/EC
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C



#### DESCRIPTION

The VS-50WQ03FNPbF surface mount Schottky rectifier has been designed for applications requiring low forward drop and small foot prints on PC board. Typical applications are in disk drives, switching power supplies, converters, freewheeling diodes, battery charging, and reverse battery protection.

#### MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	5.5	A
$V_{RRM}$		30	V
$I_{FSM}$	$t_p = 5 \mu s$ sine	320	A
$V_F$	5 Apk, $T_J = 125^\circ C$	0.35	V
$T_J$	Range	- 40 to 150	$^\circ C$

#### VOLTAGE RATINGS

PARAMETER	SYMBOL	VS-50WQ03FNPbF	UNITS
Maximum DC reverse voltage	$V_R$	30	V
Maximum working peak reverse voltage	$V_{RWM}$		

#### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current See fig. 5	$I_{F(AV)}$	50 % duty cycle at $T_C = 136^\circ C$ , rectangular waveform	5.5	A
Maximum peak one cycle non-repetitive surge current See fig. 7	$I_{FSM}$	5 $\mu s$ sine or 3 $\mu s$ rect. pulse	320	A
		10 ms sine or 6 ms rect. pulse	130	
Non-repetitive avalanche energy	$E_{AS}$	$T_J = 25^\circ C$ , $I_{AS} = 2 A$ , $L = 5 mH$	10	mJ
Repetitive avalanche current	$I_{AR}$	Current decaying linearly to zero in 1 $\mu s$ Frequency limited by $T_J$ maximum $V_A = 1.5 \times V_R$ typical	2.0	A

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ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum forward voltage drop See fig. 1	V <sub>FM</sub> <sup>(1)</sup>	5 A	T <sub>J</sub> = 25 °C	0.46	V	
		10 A		0.53		
		5 A	T <sub>J</sub> = 125 °C	0.35		0.46
		10 A				
Maximum reverse leakage current See fig. 2	I <sub>RM</sub> <sup>(1)</sup>	T <sub>J</sub> = 25 °C	V <sub>R</sub> = Rated V <sub>R</sub>	3	mA	
		T <sub>J</sub> = 125 °C		58		
Threshold voltage	V <sub>F(TO)</sub>	T <sub>J</sub> = T <sub>J</sub> maximum		0.19	V	
Forward slope resistance	r <sub>t</sub>			22.22	mΩ	
Typical junction capacitance	C <sub>T</sub>	V <sub>R</sub> = 5 V <sub>DC</sub> (test signal range 100 kHz to 1 MHz), 25 °C		590	pF	
Typical series inductance	L <sub>S</sub>	Measured lead to lead 5 mm from package body		5.0	nH	

### Note

<sup>(1)</sup> Pulse width < 300  $\mu\text{s}$ , duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	$T_J^{(1)}, T_{Stg}$		- 40 to 150	$^{\circ}\text{C}$
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation See fig. 4	3.0	$^{\circ}\text{C/W}$
Approximate weight			0.3	g
			0.01	oz.
Marking device		Case style D-PAK (similar to TO-252AA)	50WQ03FN	

### Note

<sup>(1)</sup>  $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$  thermal runaway condition for a diode on its own heatsink



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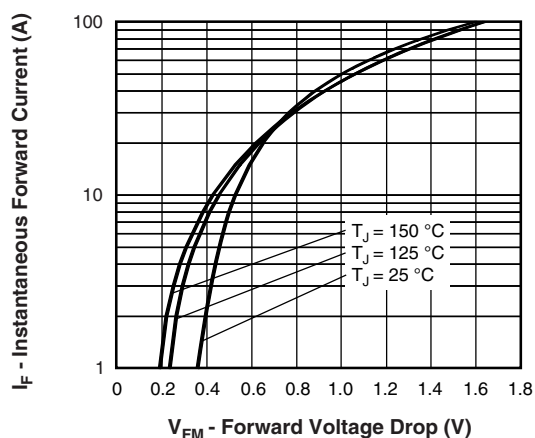


Fig. 1 - Maximum Forward Voltage Drop Characteristics

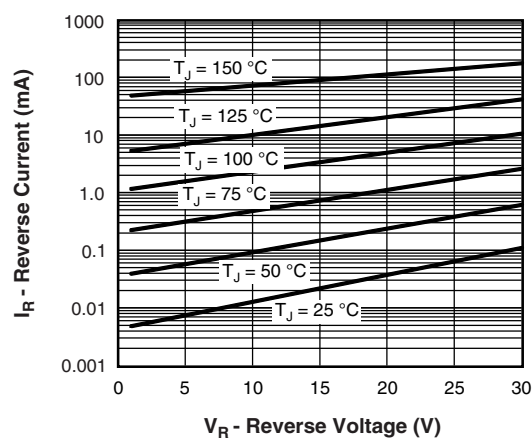


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

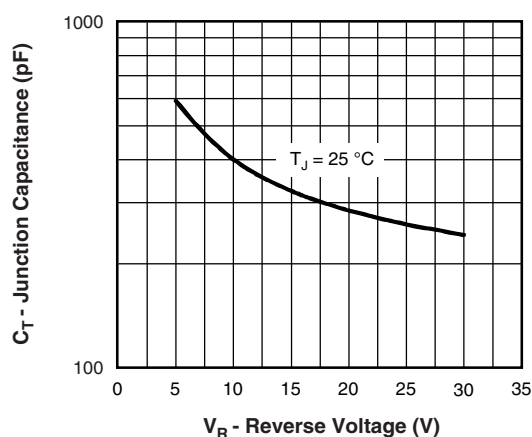


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

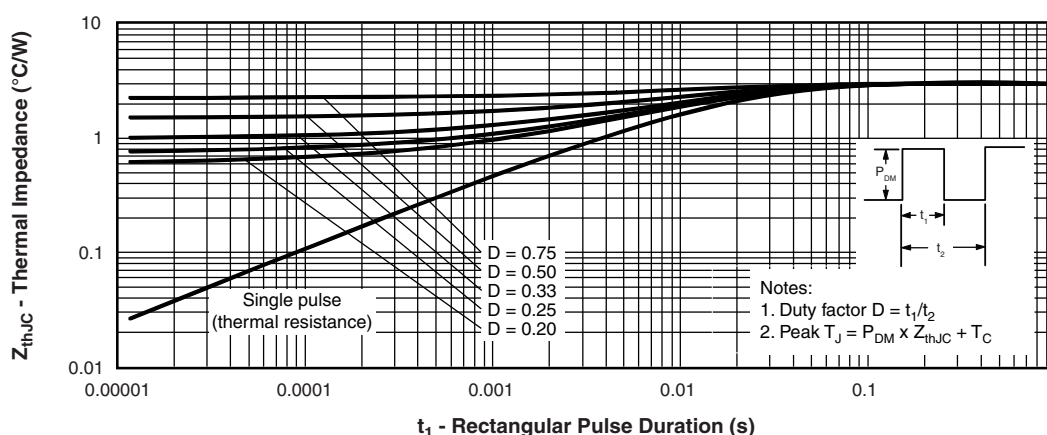


Fig. 4 - Maximum Thermal Impedance  $Z_{thJC}$  Characteristics

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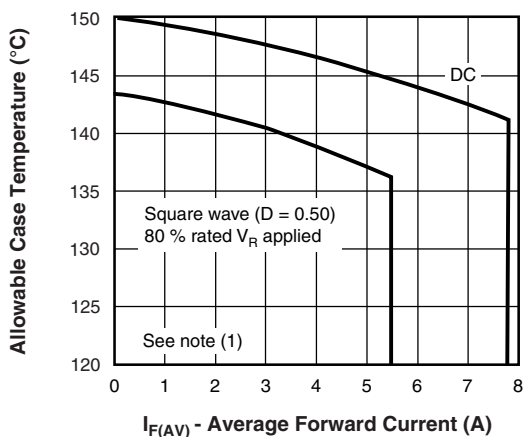


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

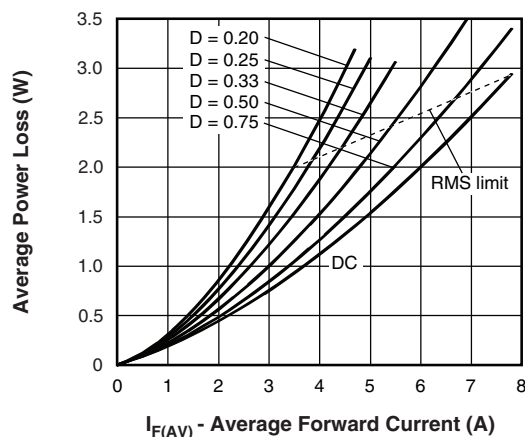


Fig. 6 - Forward Power Loss Characteristics

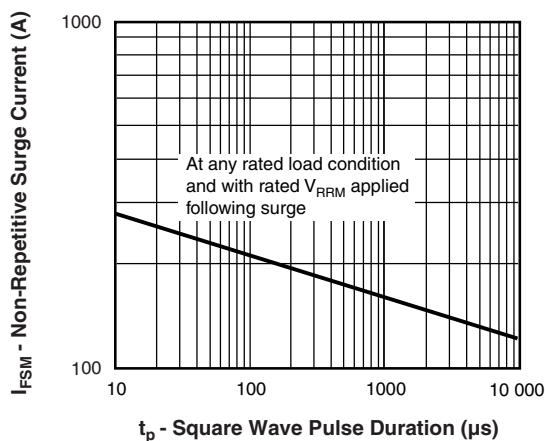


Fig. 7 - Maximum Non-Repetitive Surge Current

### Note

- (1) Formula used:  $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$ ;  
 $P_d$  = Forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);  
 $P_{dREV}$  = Inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at  $V_{R1} = 80\%$  rated  $V_R$



- 1 Vishay Semiconductors product
- 2 Current rating (5.5 A)
- 3 Package identifier:  
W = D-PAK
- 4 Schottky "Q" series
- 5 Voltage rating (03 = 30 V)
- 6 FN = TO-252AA (D-PAK)
- 7
  - None = Tube (50 pieces)
  - TR = Tape and reel
  - TRL = Tape and reel (left oriented)
  - TRR = Tape and reel (right oriented)
- 8 PbF = Lead (Pb)-free

5



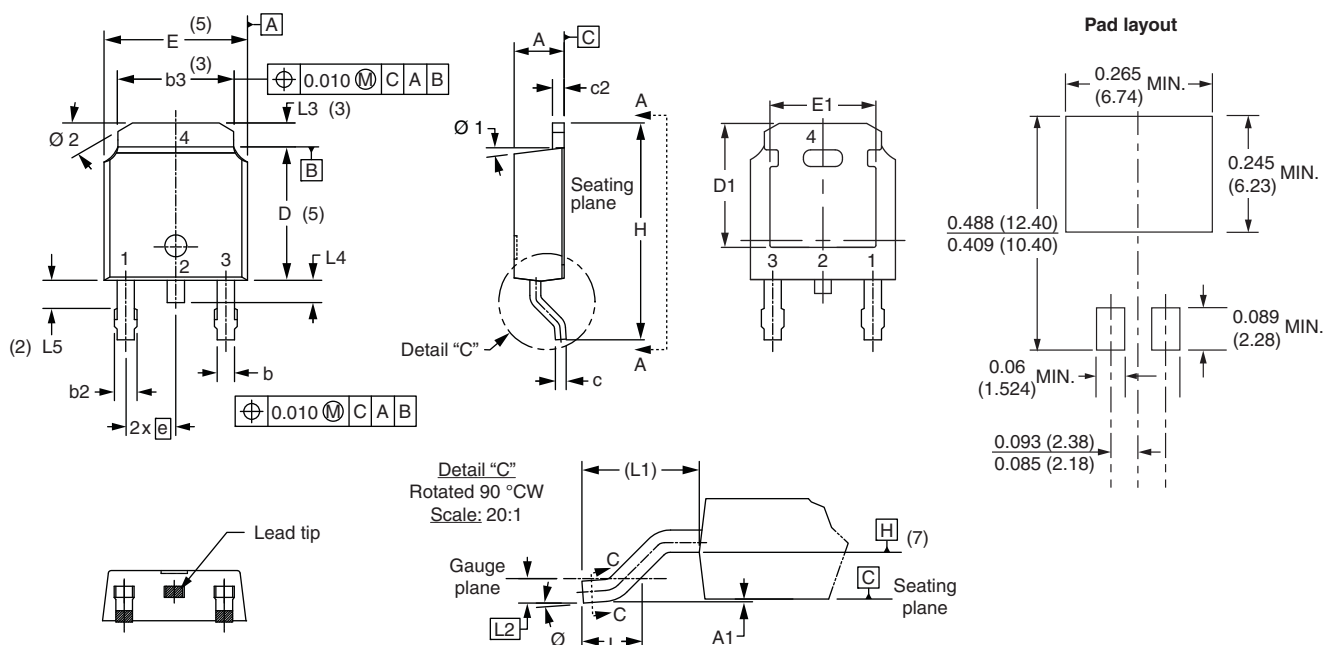
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## Outline Dimensions

Vishay Semiconductors

### D-PAK (TO-252AA)

**DIMENSIONS** in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	0.094	
A1	-	0.13	-	0.005	
b	0.64	0.89	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	3
c	0.46	0.61	0.018	0.024	
c2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	5
D1	5.21	-	0.205	-	3
E	6.35	6.73	0.250	0.265	5
E1	4.32	-	0.170	-	3

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
e	2.29 BSC		0.090 BSC		
H	9.40	10.41	0.370	0.410	
L	1.40	1.78	0.055	0.070	
L1	2.74 BSC		0.108 REF.		
L2	0.51 BSC		0.020 BSC		
L3	0.89	1.27	0.035	0.050	3
L4	-	1.02	-	0.040	
L5	1.14	1.52	0.045	0.060	2
Ø	0°	10°	0°	10°	
Ø1	0°	15°	0°	15°	
Ø2	25°	35°	25°	35°	

#### Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension uncontrolled in L5
- (3) Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad
- (4) Section C - C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.010") from the lead tip
- (5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (6) Dimension b1 and c1 applied to base metal only
- (7) Datum A and B to be determined at datum plane H
- (8) Outline conforms to JEDEC outline TO-252AA



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