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TL499A

SLVS029H-JANUARY 1984-REVISED NOVEMBER 2015

## TL499A Wide-Range Power-Supply Controllers

### 1 Features

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- Internal Series-Pass and Step-Up Switching Regulator
- Output Adjustable From 2.9 V to 30 V
- 1-V to 10-V Input for Switching Regulator
- 4.5-V to 32-V Input for Series Regulator
- Externally Controlled Switching Current
- No External Rectifier Required

### 2 Applications

- Voltage Boosting
- Dual-Supply Voltage Reglation
- Battery Back-Ups
- Microprocessor Memory Power

### 3 Description

🥖 Tools &

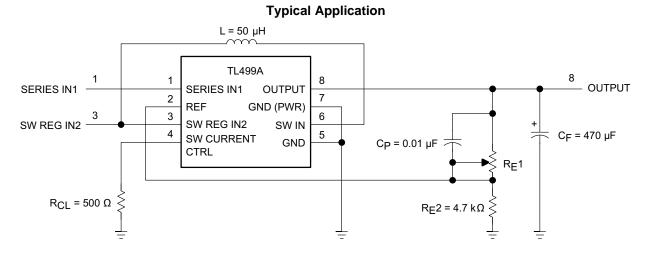
Software

The TL499A device is an integrated circuit designed to provide a wide range of adjustable regulated supply voltages. The regulated output voltage can be varied from 2.9 V to 30 V by adjusting two external resistors. When the TL499A is ac-coupled to line power through a step-down transformer, it operates as a series DC voltage regulator to maintain the regulated output voltage. With the addition of a battery from 1.1 V to 10 V, an inductor, a filter capacitor, and two resistors, the TL499A operates as a step-up switching regulator during an AC-line failure. The adjustable regulated output voltage makes the TL499A useful for a wide range of applications. Providing backup power during an ACline failure makes the TL499A extremely useful in microprocessor memory applications. The TL499AC is characterized for operation from -20°C to +85°C.

**Device Information**<sup>(1)</sup>

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)		
TI 400A	SO (8)	6.20 mm × 5.30 mm		
TL499A	PDIP (8)	9.81 mm × 6.35 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.





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### **4** Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

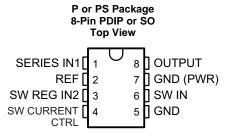
#### Changes from Revision G (September 2001) to Revision H



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## 5 Pin Configuration and Functions



#### **Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
GND	5	—	Signal ground.
GND (PWR)	7	—	Power ground.
OUTPUT	8	0	Regulated output
REF	2	I	Feedback tap for output voltage
SERIES IN1	1	—	Power source for series voltage regulator.
SW CURRENT CTRL	4	I/O	Resistor to ground controls switching current
SW IN	6	I/O	Step up switching inductor node
SW REG IN2	3	—	Power source for step-up switching regulator.

### 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Vo	Output voltage <sup>(2)</sup>	-0.3	35	V
V <sub>I</sub> 1	Input voltage, series regulator	-0.3	35	V
V <sub>l</sub> 2	Input voltage, switching regulator	-0.3	10	V
	Blocking-diode reverse voltage		35	V
	Blocking-diode forward current		1	А
SW IN	Power switch current		1	А
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C
TJ	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

### 6.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±200	V
V <sub>(ESD)</sub>	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±2000	v

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±200-V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



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#### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM MAX	UNIT
Output voltage, V <sub>O</sub>	2.9	30	V
Input voltage, VI1 (SERIES IN1)	4.5	32	V
Input voltage, VI2 (SW REG IN2)	1.1	10	V
Output-to-input differential voltage, switching regulator, $V_O - V_I 2$ (see <sup>(1)</sup> )	1.2	28.9	V
Continuous output current, I <sub>O</sub>		100	mA
Power switch current (at SW IN)		500	mA
Current-limiting resistor, R <sub>CL</sub>	150	1000	Ω
Filter capacitor	100	470	μF
Pass capacitor		0.1	μF
Inductor, L (dcr $\leq 0.1 \Omega$ )	50	150	μH
Operating free-air temperature, T <sub>A</sub>	-20	85	°C

When operating temperature range is  $T_A \le 70^{\circ}$ C, minimum  $V_O - V_I 2$  is  $\ge 1.2$  V. When operating temperature range is  $T_A \le 85^{\circ}$ C, (1) minimum  $V_0 - V_12$  is  $\ge 1.9$  V.

#### 6.4 Thermal Information

		TL4	TL499A			
	THERMAL METRIC <sup>(1)</sup>	P (PDIP)	PS (SO)	UNIT		
		8 PINS	8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(2)(3)</sup>	49.7	110.7	°C/W		
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	38.8	69.0	°C/W		
$R_{\theta J B}$	Junction-to-board thermal resistance	26.9	55.7	°C/W		
ΨJT	Junction-to-top characterization parameter	16.1	20.1	°C/W		
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	26.7	54.9	°C/W		

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application (1) report, SPRA953.

Maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(max)} - T_A) / \theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability. The package thermal impedance is calculated in accordance with JESD 51-7. (2)

(3)

### 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage deviation	(see <sup>(1)</sup> )			20	30	mV/V
N N2		$T_A = -20^{\circ}C$ to $70^{\circ}C$	1.2			N/
$V_0 - V_1 2$	Switching regulator minimum boost	$T_A = -20^{\circ}C$ to $85^{\circ}C$	1.9			V
Dropout voltage	Series regulator	V <sub>I</sub> 1 = 15 V, I <sub>O</sub> = 50 mA			1.8	V
Reference voltage	(internal)	$V_1 1 = 5 V, V_0 = 3 V, I_0 = 1 mA$	1.2	1.26	1.32	V
Reference-voltage	e change with temperature			5	10	mV/V
Output regulation	(of reference voltage)	$I_{O} = 1 \text{ mA to } 50 \text{ mA}$		10	30	mV/V
					10	
Output current	Switching regulator				15	mA
(see Figure 3)					65	
	Series regulator				100	
Standby current	Switching regulator	V <sub>I</sub> 2 = 3 V, V <sub>O</sub> = 9 V, T <sub>A</sub> = 25°C		15	80	μΑ
	Series regulator	$V_1 1 = 15 V, V_0 = 9 V, R_E 2 = 4.7 k\Omega$		0.8	1.2	mA

(1) Voltage deviation is the output voltage difference that occurs in a change from series regulation to switching regulation: Voltage deviation =  $V_{O}$  (series regulation) –  $V_{O}$  (switching regulation)



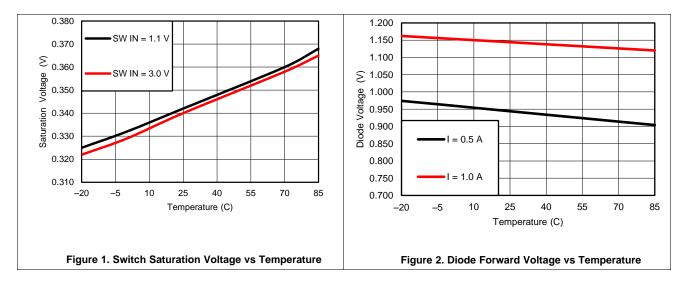
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### 6.6 Typical Characteristics



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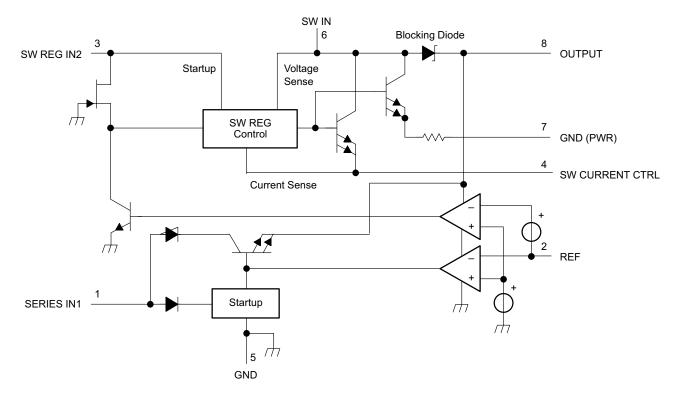
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### 7 Detailed Description

### 7.1 Overview

The TL499A provides an adjustable output voltage between 2.9 V and 30 V. The primary power source uses the internal linear regulator to provide the output voltage. When the primary power source is removed, the secondary power source is stepped up using the internal switching regulator to provide the output voltage.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The TL499A has an adjustable output voltage set by feedback provided to REF pin abs an adjustable switching current is set by value of resistor on SW CURRENT CONTROL pin. The lower resistance provides increased switching current.

Dual power supply inputs also provide protection against power faults on the main supply of the TL499A.

### 7.4 Device Functional Modes

The TL499A has two functional modes:

- Linear voltage regulation when SERIES IN1 supply is present.
- Step-up voltage regulation when SERIES IN1 supply is absent.



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### 8 Application and Implementation

**NOTE** Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

One or two power sources will be regulated to an output voltage set by two feedback resistors.

### 8.2 Typical Application

Figure 3 shows the basic configuration of the two power source voltage regulator

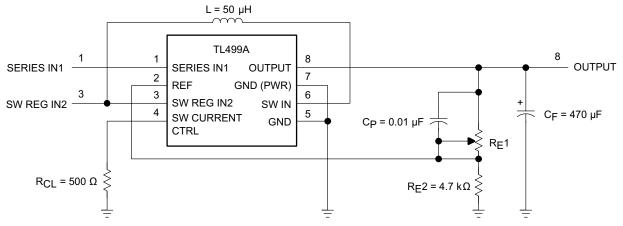


Figure 3. TL499A Basic Configuration

### 8.2.1 Design Requirements

Provide one or more of the following power sources:

- SERIES IN1 voltage greater than OUTPUT voltage by more than dropout voltage
- SW REG IN2 voltage less than OUTPUT voltage

Select R<sub>CL</sub> value based on Table 1 through Table 5.

# Table 1. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With $R_{CL}$ = 150 $\Omega$

		S	WITCHIN	G REGUL	ATOR IN		TAGE (SW	REG IN2	2) (V)				
OUTPUT VOLTAGE (V)	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9		
	OUTPUT CURRENT (mA)												
30										65	90		
25									50	80	100		
20						20	25	30	85	100	100		
15				15	20	30	45	55	100	100	100		
12	10	15	20	25	30	40	55	70	100	100	100		
10	15	20	25	30	35	45	65	80	100	100			
9	20	25	25	35	40	50	70	90	100	100			
6	30	35	40	45	55	75	95	100					



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### **Typical Application (continued)**

# Table 1. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With $R_{CL}$ = 150 $\Omega$ (continued)

		SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)													
OUTPUT VOLTAGE (V)	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9				
10211102(1)				0		URRENT	(mA)								
5	35	40	45	55	70	85	100	100	Circuit	of Figure	1 over				
4.5	35	45	50	60	75	95	100	100 <sup>(1)</sup>	Circuit	$R_{Cl} = 150$	1, except: ΩΩ				
3	55	65 <sup>(1)</sup>	75 <sup>(1)</sup>	95 <sup>(1)</sup>	100 <sup>(1)</sup>				$R_{CL} = 150 \Omega$ $C_F = 330 \mu F$ $C_P = 0.1 \mu F$						
2.9	60 <sup>(1)</sup>	70 <sup>(1)</sup>	75 <sup>(1)</sup>	100 <sup>(1)</sup>	100 <sup>(1)</sup>					C <sub>P</sub> = 0.1 μF					

(1) The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential-voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

# Table 2. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With $R_{CL}$ = 200 $\Omega$

		SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)												
OUTPUT VOLTAGE (V)	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9			
1021/102 (1)	OUTPUT CURRENT (mA)													
30										50	100			
25									50	70	100			
20						15	25	30	70	90	100			
15				10	15	25	35	45	90	100	100			
12	10	10	15	20	25	35	45	60	100	100	100			
10	15	20	20	25	30	40	55	70	100	100				
9	20	20	25	30	35	45	60	80	100					
6	25	30	35	45	50	65	90	100						
5	30	35	40	55	60	75	100	100	Circuit of Figure 1, except: $R_{CL} = 200 \Omega$ $C_F = 330 \mu F$ $C_P = 0.1 \mu F$					
4.5	35	40	45	55	65	85	100	100 <sup>(1)</sup>						
3	50	55 <sup>(1)</sup>	65 <sup>(1)</sup>	80 <sup>(1)</sup>	90 <sup>(1)</sup>									
2.9	50 <sup>(1)</sup>	60 <sup>(1)</sup>	65 <sup>(1)</sup>	85 <sup>(1)</sup>	100 <sup>(1)</sup>									

(1) The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differentialvoltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

# Table 3. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With $R_{CL}$ = 300 $\Omega$

		SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)										
OUTPUT VOLTAGE (V)	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9	
	OUTPUT CURRENT (mA)											
30										40	70	
25									40	55	100	
20						10	15	20	55	70	100	
15				10	10	20	30	35	75	95	100	
12	10	10	10	15	20	25	35	45	95	100	100	
10	15	15	15	20	25	30	45	55	100	100		
9	15	15	20	25	30	35	50	60	100	100		
6	25	25	30	35	45	55	70	90				

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# Table 3. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With $R_{CL}$ = 300 $\Omega$ (continued)

		S	WITCHIN	G REGUL	ATOR INF		TAGE (SW	REG IN2	2) (V)		
OUTPUT VOLTAGE (V)	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
VOLTAGE (V)	OUTPUT CURRENT (mA)										
5	30	30	35	45	50	65	85	100	Circuit of Figure 1, except: $R_{CL} = 300 \Omega$ $C_F = 330 \mu F$ $C_P = 0.1 \mu F$		
4.5	30	35	40	45	55	70	95	100 <sup>(1)</sup>			
3	45	50 <sup>(1)</sup>	55 <sup>(1)</sup>	70 <sup>(1)</sup>	90 <sup>(1)</sup>						
2.9	45 <sup>(1)</sup>	50 <sup>(1)</sup>	60 <sup>(1)</sup>	75 <sup>(1)</sup>	95 <sup>(1)</sup>						

(1) The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differentialvoltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

# Table 4. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With $R_{CL}$ = 510 $\Omega$

		S	WITCHIN	G REGUL	ATOR INF	UT VOLT	AGE (SV	REG IN2	) (V)		
OUTPUT VOLTAGE (V)	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	OUTPUT CURRENT (mA)										
30										30	50
25									25	40	75
20									40	55	90
15							15	20	55	70	100
12					10	15	25	35	65	80	100
10				10	20	25	30	40	70	85	
9	10	10	10	15	20	25	35	45	75	100	
6	15	20	20	25	30	35	50	60			
5	20	20	35	30	35	45	55	70	Circuit	of Eiguro	1 avaant:
4.5	25	25	30	35	40	50	65	90 <sup>(1)</sup>	Circuit of Figure 1, except: $R_{CL} = 510 \Omega$ $C_F = 330 \mu F$ $C_P = 0.1 \mu F$		
3	35	35 <sup>(1)</sup>	40 <sup>(1)</sup>	50 <sup>(1)</sup>	75 <sup>(1)</sup>						
2.9	35 <sup>(1)</sup>	35 <sup>(1)</sup>	40 <sup>(1)</sup>	55 <sup>(1)</sup>	80 <sup>(1)</sup>					$C_{\rm P} = 0.1$	μr

(1) The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differentialvoltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

# Table 5. Maximum Output Current vs Input and Output Voltages for Step-Up Switching Regulator With $R_{CL}$ = 1 $k\Omega$

		-											
		SWITCHING REGULATOR INPUT VOLTAGE (SW REG IN2) (V)											
OUTPUT VOLTAGE (V)	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9		
101/101(1)		OUTPUT CURRENT (mA)											
30											35		
25										35	50		
20										35	60		
15								10	30	45	65		
12								20	40	45	85		
10							15	25	40	55			
9				10	10	15	25	30	45	60			
6	10	10	10	15	20	20	30	35					
5	10	10	15	20	20	25	35	40	Circuit of Figure 1, except: $R_{CL} = 1 k\Omega$ $C_F = 330 \mu F$ $C_P = 0.1 \mu F$				
4.5	15	15	15	20	25	30	40	45 <sup>(1)</sup>					
3	20	25 <sup>(1)</sup>	25 <sup>(1)</sup>	30 <sup>(1)</sup>	35 <sup>(1)</sup>								
2.9	20 <sup>(1)</sup>	25 <sup>(1)</sup>	25 <sup>(1)</sup>	30 <sup>(1)</sup>	45 <sup>(1)</sup>					$C_{\rm P} = 0.1$	μr		

(1) The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential-voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).



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### 8.2.2 Detailed Design Procedure

Select the values for  $R_E1$  and  $R_E2$  using Equation 1: VOUT = REF x (1 +  $R_E1/R_E2$ )

### 8.2.3 Application Curve

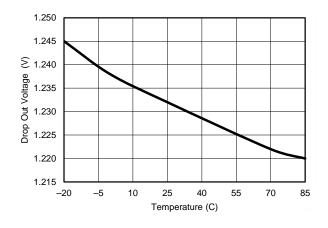




Figure 4. Dropout Voltage vs Temperature

### 9 Power Supply Recommendations

See *Recommended Operating Conditions* for allowable range for the power supply. Bypass capacitors must be placed near device supply pins.

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(1)



### 10 Layout

### 10.1 Layout Guidelines

The switching nodes at pins 3, 6, 7, and 8 must use short traces with ground and power planes for reduced noise and improved performance.

### 10.2 Layout Example

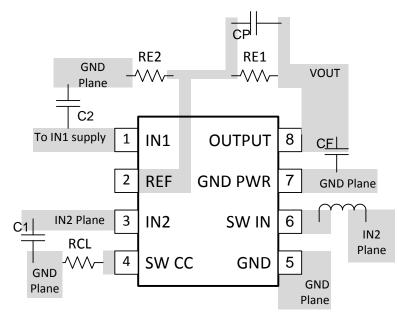


Figure 5. Typical Layout



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### **11 Device and Documentation Support**

### **11.1 Community Resources**

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E<sup>™</sup> Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.2 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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#### PACKAGING INFORMATION

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Orderable Device	Status	Package Type		Pins	•	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TL499ACP	ACTIVE	PDIP	Ρ	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-20 to 85	TL499ACP	Samples
TL499ACPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-20 to 85	TL499ACP	Samples
TL499ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	T499A	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs. LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect. NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available. OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

PBD: The Pb-Free/Green conversion plan has not been defined. Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS Exempt): The formation of the regularized at the temperatures of the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above. Green (RoHS & no Sb/Br): Ti defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight is between the die and package). in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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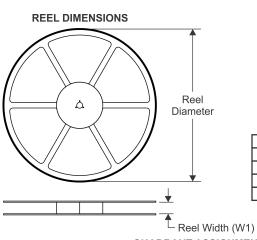


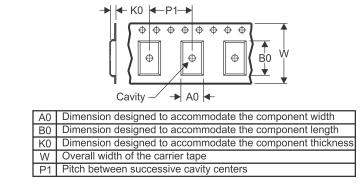


## PACKAGE MATERIALS INFORMATION

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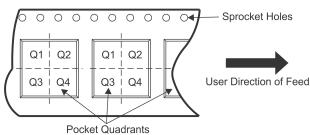
## TAPE AND REEL INFORMATION





TAPE DIMENSIONS

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL499ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

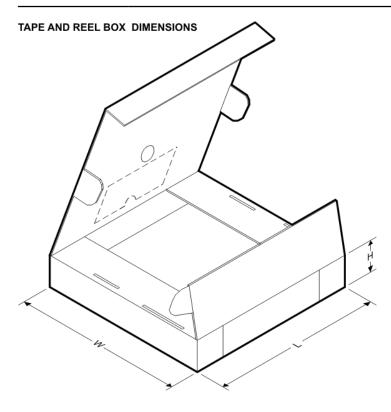


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## PACKAGE MATERIALS INFORMATION

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\*All dimensions are nominal

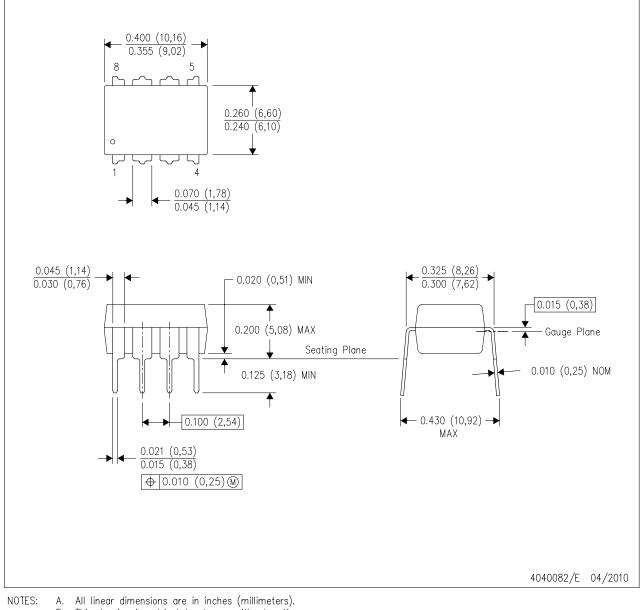
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL499ACPSR	SO	PS	8	2000	367.0	367.0	38.0



### **MECHANICAL DATA**

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.

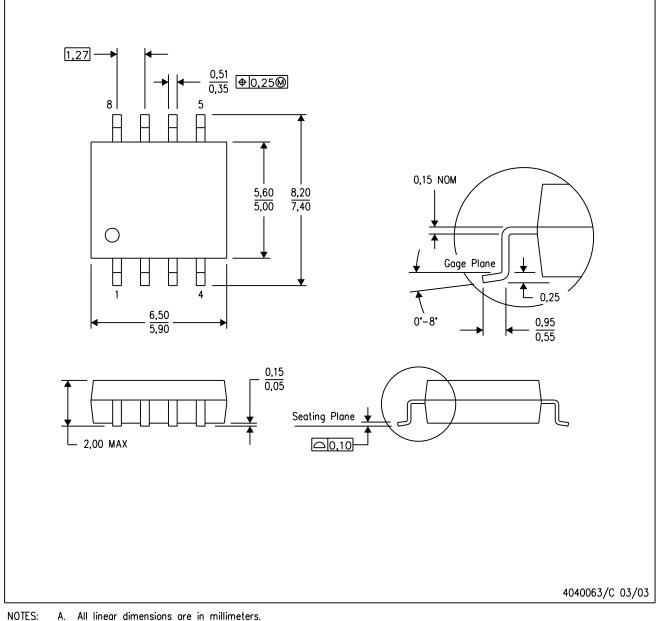




### PS (R-PDSO-G8)

**MECHANICAL DATA** 

PLASTIC SMALL-OUTLINE PACKAGE



A. All linear dimensions are in millimeters.

Β. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.





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