FGLS12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

The ***Tomodachi*** Series of non-isolated dc-dc converters deliver exceptional electrical and thermal performance in DOSA based footprints for Point-of-Load converters. Operating from a 4.5Vdc-14.4Vdc input, these are the converters of choice for Intermediate Bus Architecture (IBA) and Distributed Power Architecture applications that require high efficiency, tight regulation, and high reliability in elevated temperature environments with low airflow. The Tunable Loop™ feature allows the user to optimize the dynamic response of the converter to match the load with reduced amount of output capacitance leading to savings on cost and PWB area.

The **FGLS12SR6040*A** converter of the ***Tomodachi*** Series delivers 40A of output current at a tightly regulated programmable output voltage of 0.6Vdc to 2.0Vdc. The thermal performance of the **FGLS12SR6040*A** is best-in-class: Little derating is needed up to 85℃, under natural convection.

TUNABLE LOOP™
A LINEAGE POWER TRADEMARK

Applications

- Intermediate Bus Architecture
- Telecommunications
- Data/Voice processing
- Distributed Power Architecture
- Computing (Servers, Workstations)
- Test Equipments

Features

- Compliant to RoHS EU Directive 2011/65/EU
- Delivers up to 40A (80W)
- High efficiency, no heatsink required
- Negative and Positive ON/OFF logic
- DOSA based
- Small size: 33.02 x 13.46 x 10.9mm (1.3 in x 0.53 in x 0.429 in)
- Tape & reel packaging
- Programmable output voltage from 0.6V to 2.0V via external resistor
- Tunable Loop™ to optimize dynamic output voltage response
- Power Good signal
- Fixed switching frequency with capability of external synchronization
- Over-current protection (non-latching)
- Over-temperature protection
- Remote ON/OFF
- Ability to sink and source current
- No minimum load required
- *UL** 60950-1 2nd Ed. Recognized, *CSA*† C22.2 No. 60950-1-07 Certified, and *VDE*‡ (EN60950-1 2nd Ed.) Licensed (Pending)
- ISO** 9001 and ISO 14001 certified manufacturing facilities

* *UL* is a registered trademark of Underwriters Laboratories, Inc.
† *CSA* is a registered trademark of Canadian Standards Association.
‡ *VDE* is a trademark of Verband Deutscher Elektrotechniker e.V.
** ISO is a registered trademark of the International Organization of Standards

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Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may lead to degradation in performance and reliability of the converter and may result in permanent damage.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Input Voltage	Continuous	-0.3		15	Vdc
Operating Temperature	Ambient temperature	-40		85	°C
Storage Temperature		-55		125	°C
Output Voltage		0.6		2.0	Vdc

Electrical Specifications

All specifications apply over specified input voltage, output load, and temperature range, unless otherwise noted.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Operating Input Voltage Range		4.5		14.4	Vdc
Maximum Input Current	Vin=4.5V to 14V, Io=Max			24	Adc
Input No Load Current	Vout=2.0V		104		mA
	Vout=0.6V		54.7		mA
Input Stand-by Current	Vin=12V, module disabled		12.5		mA
Inrush Transient, I^2t				1	A^2s
Input Reflected-Ripple Current	Peak-to-peak (5Hz to 20MHz, 1uH source impedance; Vin=0 to 14V, Io=Max		90		mAp-p
Input Ripple Rejection (120Hz)			-60		dB

FGLS12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Electrical Specifications (Continued)

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS					
Output Voltage Set Point (no load)	With 0.1% tolerance for external resistor used to set output voltage	-1.0		+1.0	%Vout
Output Voltage Range	(Over all operating input voltage, resistive load and temperature conditions until end of life)	-3.0		+3.0	%Vout
Adjustment Range (selected by an external resistor)	Some output voltages may not be possible depending on the input voltage – see feature description section	0.6		2.0	Vdc
Remote Sense Range				0.5	Vdc
Output Regulation	Line (Vin = min to max)			6	mV
	Load (Io = min to max)			10	mV
	Temperature (Ta = min to max)		0.4		%Vout
Output Ripple and Noise	Vin=12V, Io= min to max, Co = 0.1uF+22uF ceramic capacitors				
Peak to Peak	5MHz to 20MHz bandwidth		50	100	mVp-p
RMS	5MHz to 20MHz bandwidth		20	38	mVrms
External Load Capacitance [1]	Plus full load (resistive)				%
Without the Tunable Loop	ESR ≥ 1mΩ	6x47		6x47	uF
With the Tunable Loop	ESR ≥ 0.15mΩ	6x47		7,000	uF
	ESR ≥ 10mΩ	6x47		8,500	uF
Output Current Range	(in either sink or source mode)	0		40	Adc
Output Current Limit Inception (Hiccup mode)	Current limit does not operate in sink mode		150		% Io-max
Output Short-Circuit Current	Vo ≤ 250mV, Hiccup mode		2.1		Arms
Efficiency					
Vin = 12Vdc, Ta = 25°C, Io = max	Vout=1.8Vdc		91.5		%
	Vout=1.2Vdc		88.5		%
	Vout=0.6Vdc		81.3		%
Switching Frequency			400		kHz
Frequency Synchronization					
Synchronization Frequency Range		350		480	kHz
High Level Input Voltage	VIH	2.0			V
Low Level Input Voltage	VIL			0.4	V
Input Current, SYNC				100	nA
Minimum Pulse Width, SYNC		100			nS
Maximum SYNC rise time		100			nS

[1] External capacitors may require using the new Tunable Loop™ feature to ensure that the module is stable as well as getting the best transient response. See the Tunable Loop™ section for details.

FGLS12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

General Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Calculated MTBF	Io = 0.8 Io-max, Ta = 40°C Telecordia Issue 2 Method 1 Case 3		6,498,438		Hours
Weight			11.7 (0.41)		g (oz.)

Feature Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
ON/OFF Signal Interface	Vin = min to max, open collector or equivalent, Signal reference to GND				
Positive Logic					
Logic High (Module ON)					
Input High Current				10	uA
Input High Voltage		3.5		Vin-max	V
Logic Low (Module OFF)					
Input Low Current				1	mA
Input Low Voltage		-0.3		0.4	V
Negative Logic	On/Off pin is open collector/drain logic input with external pull-up resistor; signal reference to GND				
Logic High (Module OFF)					
Input High Current				1	mA
Input High Voltage		2		Vin-max	V
Logic Low (Module ON)					
Input Low Current				10	uA
Input Low Voltage		-0.2		0.4	V
Turn-On Delay Time	Full resistive load				
with Vin (module enabled, then Vin applied)	From Vin=Vin(min) to 0.1*Vout(nom)		1.1		ms
with Enable (Vin applied, then enabled)	From enable to 0.1*Vout(nom)		700		us
Rise Time (Full resistive load)	From 0.1*Vout(nom) to 0.9*Vout(nom)		1.5		ms
Output Voltage Overshoot	Ta = 25C, Vin = min to max, Iout = min to max, with or without external capacitance			3.0	%Vout

FGLS12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Feature Specifications (continued)

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Over Temperature Protection			145		C
Tracking Accuracy	(Power-Up: 0.5V/ms)			100	mV
	(Power-Down: 0.5V/ms)			100	mV
Input Under Voltage Lockout					
Turn-on Threshold			4.25		Vdc
Turn-off Threshold			3.96		Vdc
Hysteresis			0.25		Vdc
Power Good					
Overvoltage threshold for PGOOD ON			108		%Vout
Overvoltage threshold for PGOOD OFF			110		%Vout
Undervoltage threshold for PGOOD ON			92		%Vout
Undervoltage threshold for PGOOD OFF			90		%Vout
Pulldown resistance of PGOOD pin				50	Ω
Sink current capability into PGOOD pin				5	mA

FGLS12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Design Considerations

Input Filtering

The **FGLS12SR6040*A** converters should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Fig-1 shows the input ripple voltage for various output voltages at 40A of load current with 4x22uF, 6x22uF or 8x22uF ceramic capacitors and an input of 12V.

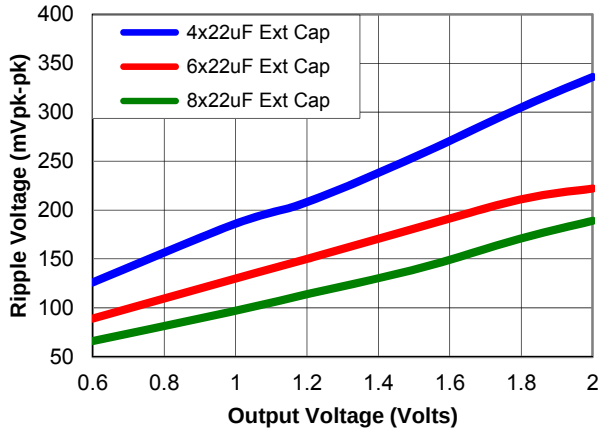

Fig-1: Input ripple voltage for various output voltages with various ceramic capacitors at the input (40A load). Input voltage is 12V. Scope bandwidth limited to 20MHz.

Output Filtering

The **FGLS12SR6040*A** is designed for low output ripple voltage and will meet the maximum output ripple specification with 0.1uF ceramic and 47uF ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. Fig-2 provides output ripple information for different external capacitance values at various Vo and a full load current of 40A. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table. Optimal performance of the module can be achieved by using the Tunable Loop™ feature described later in this data sheet.

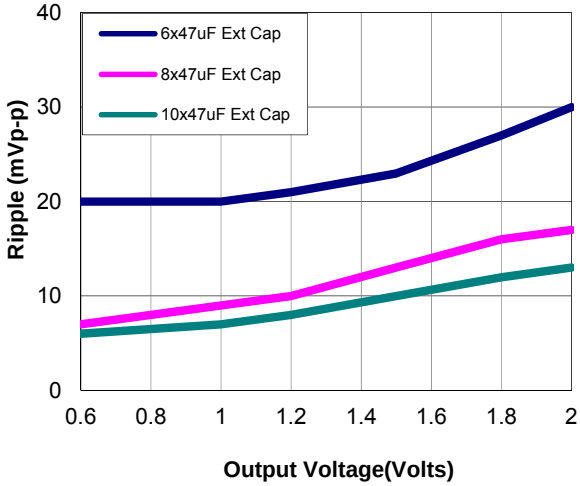

Fig-2: Output ripple voltage for various output voltages with external 6x47uF, 8x47uF or 10x47uF ceramic capacitors at the output (40A load). Input voltage is 12V. Scope bandwidth limited to 20MHz.

Safety Consideration

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL 60950-1 2nd, CSA C22.2 No. 60950-1-07, DIN EN 60950-1:2006 + A11 (VDE0805 Teil 1 + A11):2009-11; EN 60950-1:2006 + A11:2009-03.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The input to these units is to be provided with a fast-acting fuse with a maximum rating of 30A, 100V (for example, Littlefuse 456 series) in the positive input lead.

FGLS12SR6040*A

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Data Sheet

Feature Descriptions

Remote On/Off

The **FGLS12SR6040*A** power modules feature an On/Off pin for remote On/Off operation. Two On/Off logic options are available. In the Positive Logic On/Off option, (device code suffix “P” - see Part Number System), the module turns ON during a logic High on the On/Off pin and turns OFF during a logic Low. With the Negative Logic On/Off option, (device code suffix “N” - see Part Number System), the module turns OFF during logic High and ON during logic Low. The On/Off signal should be always referenced to ground. For either On/Off logic option, leaving the On/Off pin disconnected will turn the module ON when input voltage is present.

For positive logic modules, the circuit configuration for using the On/Off pin is shown in Fig-3. For negative logic On/Off modules, the circuit configuration is shown in Fig-4.

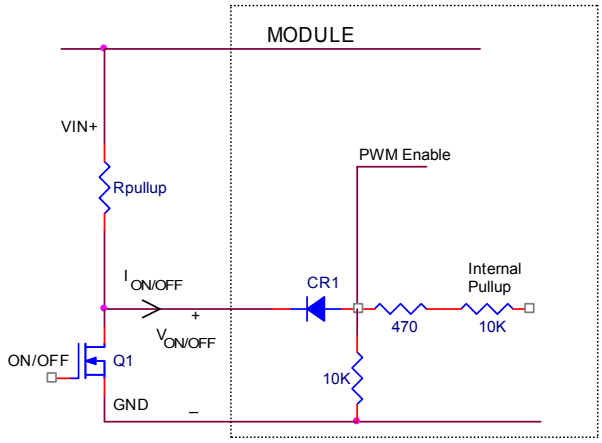

Fig-3: Circuit configuration for using positive On/Off logic.

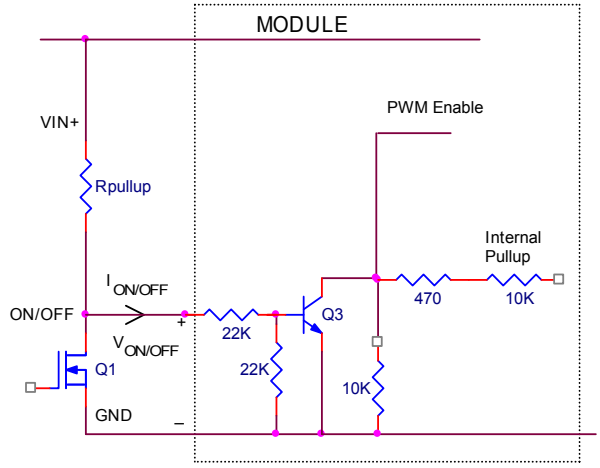

Fig-4: Circuit configuration for using negative On/Off logic.

Monotonic Start-up and Shut-down

The module has monotonic start-up and shutdown behavior for any combination of rated input voltage, output current and operating temperature range.

Startup into Pre-biased Output

The module can start into a prebiased output as long as the prebias voltage is 0.5V less than the set output voltage.

Output Voltage Programming

The output voltage of the module is programmable to any voltage from 0.6dc to 2.0Vdc by connecting a resistor between the Trim and SIG_GND pins of the module. Certain restrictions apply on the output voltage set point depending on the input voltage. These are shown in the Output Voltage vs. Input Voltage Set Point Area plot in Fig-5. The Upper Limit curve shows that for output voltages lower than 0.8V, the input voltage must be lower than the maximum of 14.4V. The Lower Limit curve shows that for output voltages higher than 0.6V, the input voltage needs to be larger than the minimum of 4.5V.

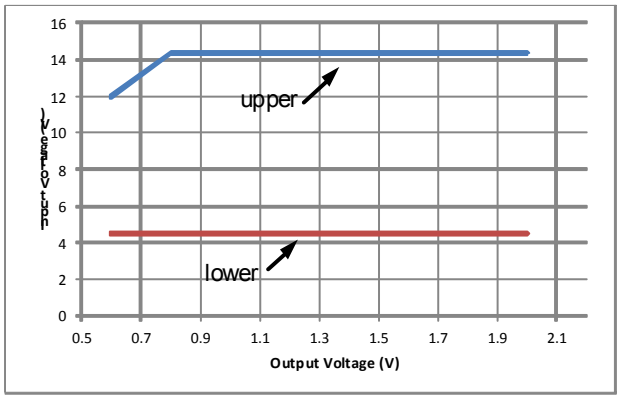

Fig-5: Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.

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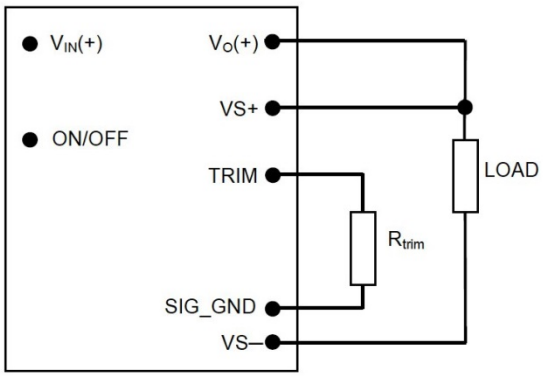
Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output



Caution *– Do not connect SIG_GND to GND elsewhere in the layout.*

Fig-6: Circuit configuration for programming output voltage using and external resistor.

Without an external resistor between Trim and SIG_GND pins, the output of the module will be 0.6Vdc. To calculate the value of the trim resistor, *Rtrim* for a desired output voltage, should be as per the following equation:

$$R_{TRIM} = \frac{12}{(V_{O\text{-}REQ} - 0.6)} \ [k\Omega]$$

Rtrim is the external resistor in kΩ
Vo-req is the desired output voltage

Note that the tolerance of a trim resistor will affect the tolerance of the output voltage. Standard 1% or 0.5% resistors may suffice for most applications; however, a tighter tolerance can be obtained by using two resistors in series instead of one standard value resistor.

Table 1 lists calculated values of R_{TRIM} for common output voltages.

Table 1: Trim Resistor Value

$V_{O\text{-}REG}$ [V]	R_{TRIM} [kΩ]
0.6	Open
0.9	40
1.0	30
1.2	20
1.5	13.33
1.8	10

Remote Sense

The power module has a Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the sense pins (VS+ and VS-). The voltage drop between the sense pins and the VOUT and GND pins of the module should not exceed 0.5V.

Voltage Margining

Output voltage margining can be implemented in the module by connecting a resistor, Rmargin-up, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, Rmargin-down, from the Trim pin to output pin for margining-down. Fig-7 shows the circuit configuration for output voltage margining. The POL Programming Tool, available at www.fdk.com under the Downloads section, also calculates the values of Rmargin-up and Rmargin-down for a specific output voltage and % margin. Please consult your local FDK FAE for additional details.

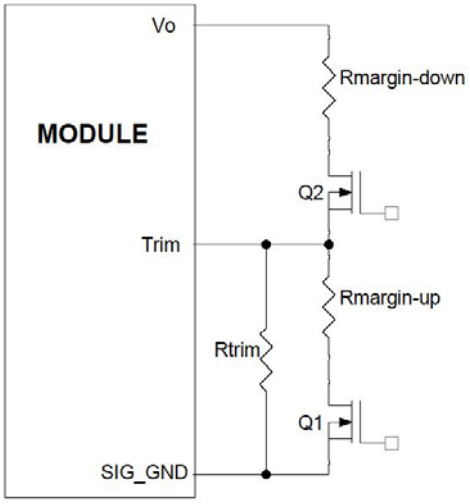


Fig-7: Circuit Configuration for margining Output Voltage.

Output Voltage Sequencing

The power module includes a sequencing feature, EZSEQUENCE that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, leave it unconnected.

The voltage applied to the SEQ pin should be scaled down by the same ratio as used to scale the output voltage down to the reference voltage of the module. This is accomplished by an external resistive divider connected across the sequencing voltage before it is fed to the SEQ pin as shown in Fig-8. In addition, a small capacitor (suggested value 100pF) should be connected across the lower resistor R1

For all Tomodachi modules, the minimum

recommended delay between the ON/OFF signal and the sequencing signal is 10ms to ensure that the module output is ramped up according to the sequencing signal. This ensures that the module soft-start routine is completed before the sequencing signal is allowed to ramp up.

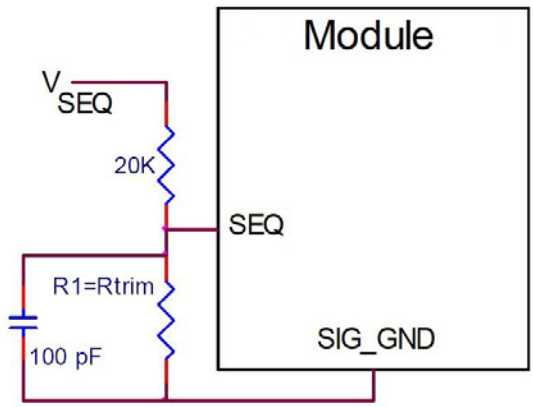


Fig-8: Circuit showing connection of the sequencing signal to the SEQ pin.

When the scaled down sequencing voltage is applied to the SEQ pin, the output voltage tracks this voltage until the output reaches the set-point voltage. The final value of the sequencing voltage must be set higher than the set-point voltage of the module. The output voltage follows the sequencing voltage on a one-to-one basis. By connecting multiple modules together, multiple modules can track their output voltages to the voltage applied on the SEQ pin.

The module's output can track the SEQ pin signal with slopes of up to 0.5V/msec during power-up or power-down.

To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. The output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage must be maintained until the tracking and output voltages reach ground potential.

Over-Current Protection

To provide protection in a fault (output overload) condition, the unit is equipped with internal current-limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates normally once the output current is brought back into its specified range.

Over-Temperature Protection

To provide protection in a fault condition, the unit is equipped with a thermal shutdown circuit. The unit will shut down if the over-temperature threshold of 145°C (typ) is exceeded at the thermal reference point Tref. Once the unit goes into thermal shutdown it will then wait to cool before attempting to restart.

Input Under-Voltage Lockout (UVLO)

At input voltages below the input under-voltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the under-voltage lockout turn-on threshold.

Synchronization

The module switching frequency can be synchronized to a signal with an external frequency within a specified range. Synchronization can be done by using the external signal applied to the SYNC pin of the module as shown in Fig-I, with the converter being synchronized by the rising edge of the external signal. The Electrical Specifications table specifies the requirements of the external SYNC signal. If the SYNC pin is not used, the module should free run at the default switching frequency.
If synchronization is not being used, connect the SYNC pin to GND.

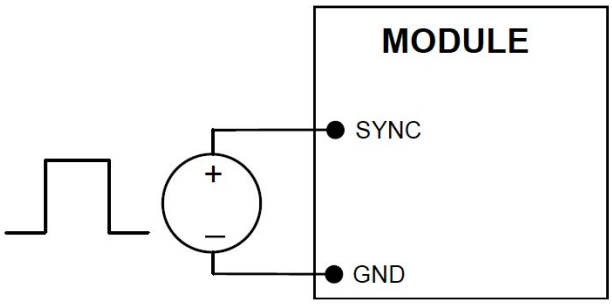


Fig-9: External source connections to synchronize switching frequency of the module.

Active Load Sharing (-P Option)

For additional power requirements, the FGLS power module is also equipped with paralleling capability. Up to five modules can be configured in parallel, with active load sharing.
To implement paralleling, the following conditions must be satisfied.

- All modules connected in parallel **must** be frequency synchronized where they are switching at the same frequency. This is done by using the SYNC function of the module and connecting to an external frequency source. Modules can be

interleaved to reduce input ripple/filtering requirements.
- The share pins of all units in parallel must be connected together. The path of these connections should be as direct as possible.
- The remote sense connections to all modules should be made that to the same points for the output, i.e. all VS+ and VS- terminals for all modules are connected to the power bus at the same points.

Some special considerations apply for design of converters in parallel operation:
- When sizing the number of modules required for parallel operation, take note of the fact that current sharing has some tolerance. In addition, under transient conditions such as a dynamic load change and during startup, all converter output currents will not be equal. To allow for such variation and avoid the likelihood of a converter shutting off due to a current overload, the total capacity of the paralleled system should be no more than 90% of the sum of the individual converters. As an example, for a system of four FGLS converters in parallel, the total current drawn should be less that 90% of (3 x 40A), i.e. less than 108 A.
- All modules should be turned ON and OFF together. This is so that all modules come up at the same time avoiding the problem of one converter sourcing current into the other leading to an overcurrent trip condition. To ensure that all modules come up simultaneously, the on/off pins of all paralleled converters should be tied together and the converters enabled and disabled using the on/off pin. Note that this means that converters in parallel cannot be digitally turned ON as that does not ensure that all modules being paralleled turn on at the same time.
- If digital trimming is used to adjust the overall output voltage, the adjustments need to be made in a series of small steps to avoid shutting down the output. Each step should be no more than 20mV for each module. For example, to adjust the overall output voltage in a setup with two modules (A and B) in parallel from 1V to 1.1V, module A would be adjusted from 1.0 to 1.02V followed by module B from 1.0 to 1.02V, then each module in sequence from 1.02 to 1.04V and so on until the final output voltage of 1.1V is reached.
- If the Sequencing function is being used to start-up and shut down modules and the module is being held to 0V by the tracking signal then there may be small deviations on the module output. This is due to controller duty cycle limitations encountered in trying to hold the voltage down near 0V.
- The share bus is not designed for redundant operation and the system will be non-functional upon failure of one of the units when multiple units are in parallel. In particular, if one of the converters shuts down during operation, the other converters may also shut down due to their outputs hitting current limit. In such a situation, unless a coordinated restart is ensured, the system may never properly restart since different converters will try to restart at different times causing an overload condition and subsequent shutdown. This situation can be avoided by having an external output voltage monitor circuit that detects a shutdown condition and forces all converters to shut down and restart together.

When not using the active load share feature, share pins should be left unconnected.

Power Good

The module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as over-temperature, overcurrent or loss of regulation occurs that would result in the output voltage going outside the specified thresholds.

The default value of PGOOD ON thresholds are set at ±8% of the nominal Vset value, and PGOOD OFF thresholds are set at ±10% of the nominal Vset. For example, if the nominal voltage (Vset) is set at 1.0V, then the PGOOD ON thresholds will be active anytime the output voltage is between 0.92V and 1.08V, and PGOOD OFF thresholds are active at 0.90V and 1.10V respectively.

The PGOOD terminal can be connected through a pull-up resistor (suggested value 100KΩ) to a source of 5VDC or lower.

Dual Layout

Identical dimensions and pin layout of Analog and Digital ***Tomodachi*** modules permit migration from one to the other without needing to change the layout. In both cases the trim resistor is connected between trim and signal ground SIG_GND.

Tunable Loop™

The module has a feature that optimizes transient response of the module called Tunable Loop™

External capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise and to reduce output voltage deviations

from the steady-state value in the presence of dynamic load current changes. Adding external capacitance however affects the voltage control loop of the module, typically causing the loop to slow down with sluggish response. Larger values of external capacitance could also cause the module to become unstable.

The Tunable Loop™ allows the user to externally adjust the voltage control loop to match the filter network connected to the output of the module. The Tunable Loop™ is implemented by connecting a series R-C between the SENSE and TRIM pins of the module, as shown in Fig-10. This R-C allows the user to externally adjust the voltage loop feedback compensation of the module.

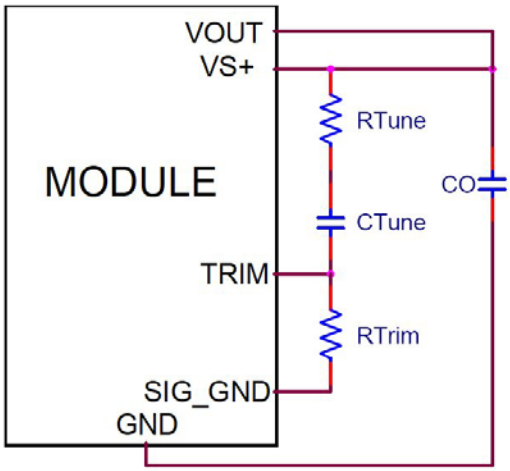


Fig-10: Circuit diagram showing connection of R_{TUNE} and C_{TUNE} to tune the control loop of the module.

Recommended values of R_{TUNE} and C_{TUNE} for different output capacitor combinations are given in Tables 2. Table 2 shows the recommended values of R_{TUNE} and C_{TUNE} for different values of ceramic output capacitors up to 1,000uF that might be needed for an application to meet output ripple and noise requirements. Selecting R_{TUNE} and C_{TUNE} according to Table 2 will ensure stable operation of the module.

In applications with tight output voltage limits in the presence of dynamic current loading, additional output capacitance will be required. Table 3 lists recommended values of R_{TUNE} and C_{TUNE} in order to meet 2% output voltage deviation limits for some common output voltages in the presence of a 20A to 40A step change (50% of full load), with an input voltage of 12V.

Please contact your FDK technical representative to obtain more details of this feature as well as for guidelines on how to select the right value of external R-C to tune the module for best transient performance and stable operation for other output capacitance values.

Table 2: General recommended value of R_{TUNE} and C_{TUNE} for Vin=12V and various external ceramic capacitor combinations.

Co	6x47uF	8x47uF	10x47uF	12x47uF	20x47uF
R_{TUNE}	330Ω	330Ω	330Ω	330Ω	2000Ω
C_{TUNE}	330pF	820pF	1200pF	1500pF	3300pF

Table 3: Recommended values of R_{TUNE} and C_{TUNE} to obtain transient deviation of 2% of Vout for a 10A step load with Vin=12V.

Vo	1.8V	1.2V	0.6V
Co	4x47uF+ 6x330uF Polymer	4x47uF+ 11x330uF Polymer	4x47uF+ 12x680uF Polymer
R_{TUNE}	220Ω	200Ω	180Ω
C_{TUNE}	5600pF	12nF	47nF
△V	34mV	22mV	12mV

Note: The capacitors used in the Tunable Loop tables are 47uF/3mΩ ESR ceramic, 330uF/12 mΩ ESR polymer capacitor and 680uF/12mΩ polymer capacitor.

FGLS12SR6040*A

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Data Sheet

Characterization

Overview

The converter has been characterized for several operational features, including efficiency, thermal derating (maximum available load current as a function of ambient temperature and airflow), ripple and noise, transient response to load step changes, start-up and shutdown characteristics.

Figures showing data plots and waveforms for different output voltages are presented in the following pages.

Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation.

Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Fig-11. The preferred airflow direction for the module is in Fig-12.

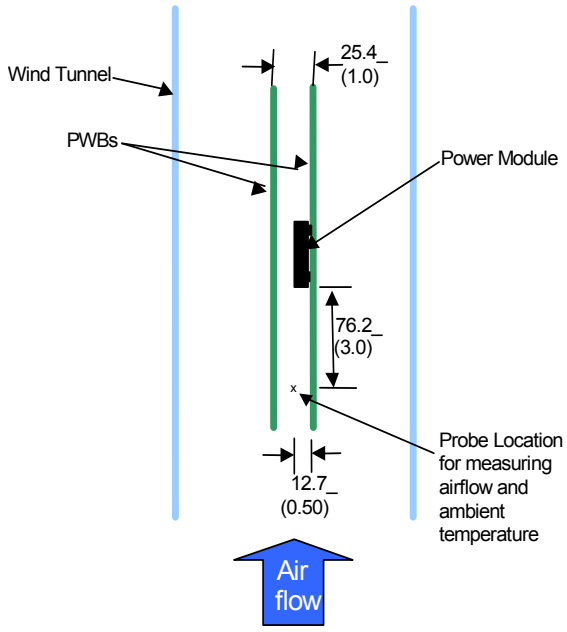


Fig-11: Thermal test set-up

The maximum available load current, for any given set of conditions, is defined as the lower of:
(i) The output current at which the temperature of any component reaches 130°C, or

(ii) The current rating of the converter (40A)
A maximum component temperature of 120°C should not be exceeded in order to operate within the derating curves. Thus, the temperature at the thermocouple location shown in Fig-12 should not exceed 130°C in normal operation.

Note that continuous operation beyond the derated current as specified by the derating curves may lead to degradation in performance and reliability of the converter and may result in permanent damage.

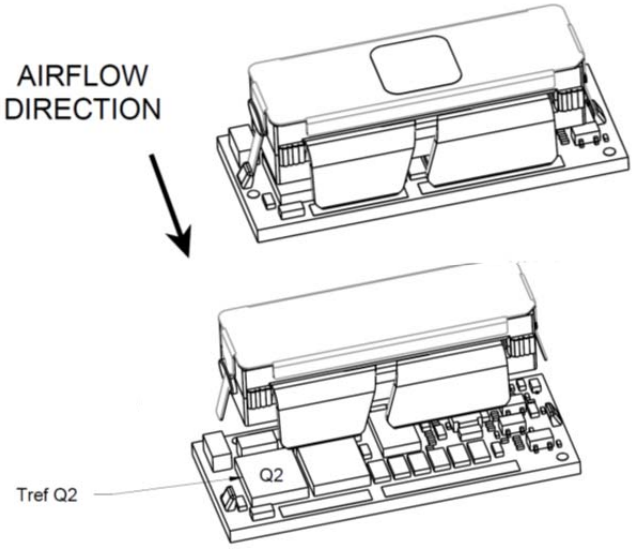


Fig-12: Preferred airflow direction and location of hot-spot of the module (Tref).

FGLS12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Characteristic Curves

The following figures provide typical characteristics for the 40A Analog Tomodachi at 1.8Vo and 25°C

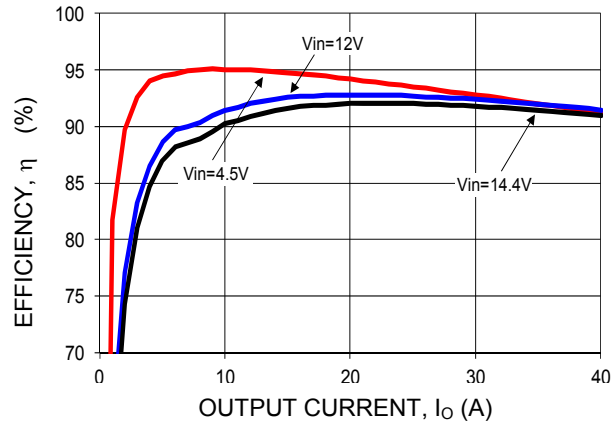


Fig-13. Converter Efficiency versus Output Current.

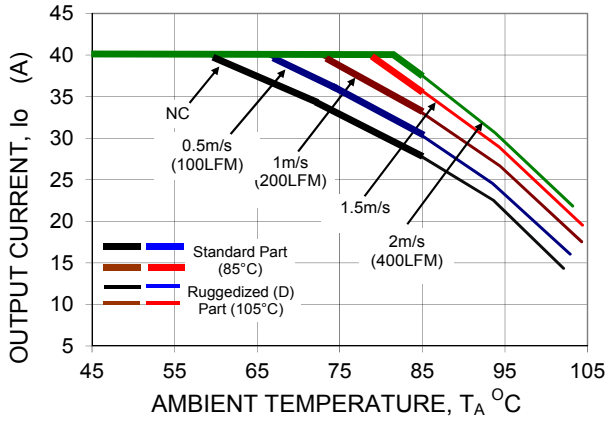


Fig-14. Derating Output Current versus Ambient Temperature and Airflow.

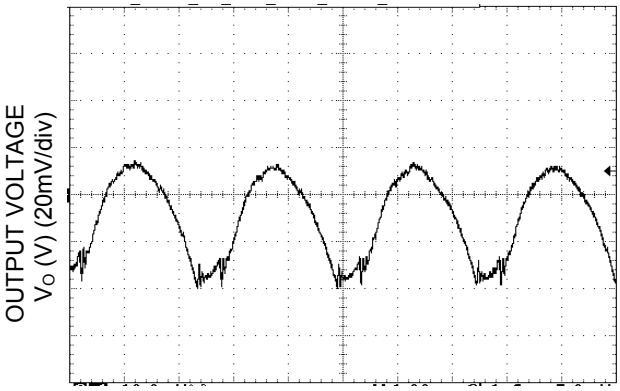


Fig-15. Typical output ripple and noise (CO=6X47µF ceramic, VIN = 12V, Io = Io,max,).

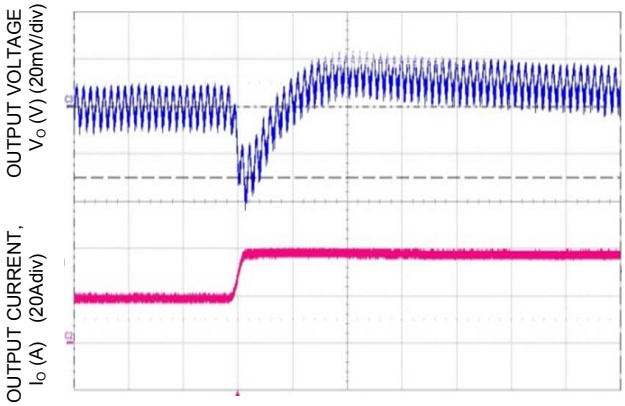


Fig-16. Transient Response to Dynamic Load Change from 50% to 100% at 12Vin, Cout= 6 x 330uF, CTune= 5.6nF & RTune= 220Ω

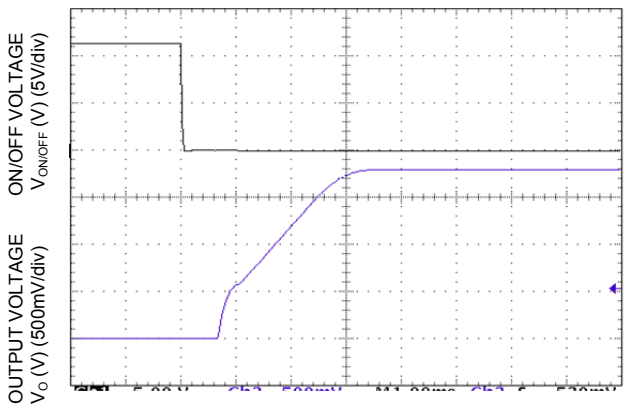


Fig-17. Typical Start-up Using On/Off Voltage (Io = Io,max).

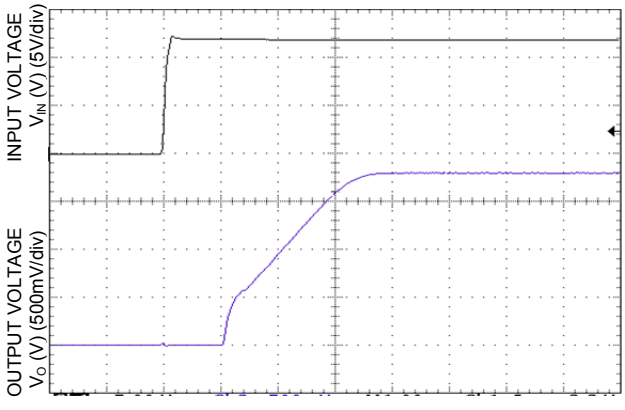


Fig-18. Typical Start-up Using Input Voltage (VIN = 12V, Io = Io,max).

FGLS12SR6040*A

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Data Sheet

Characteristic Curves

The following figures provide typical characteristics for the 40A Analog Tomodachi at 1.2Vo and 25°C

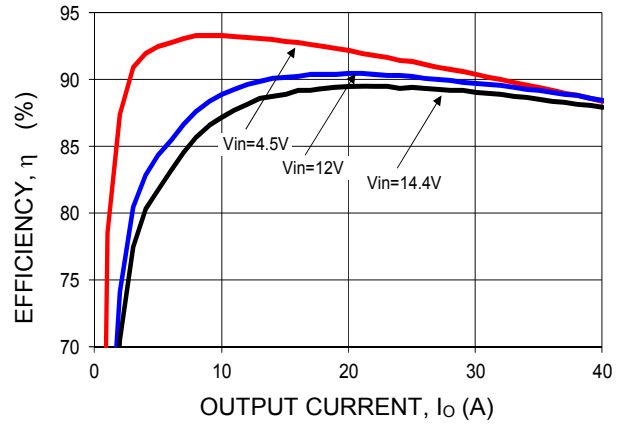


Fig-19. Converter Efficiency versus Output Current.

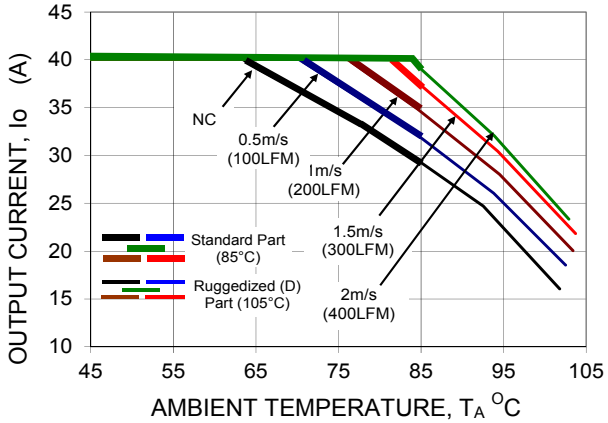


Fig-20. Derating Output Current versus Ambient Temperature and Airflow.

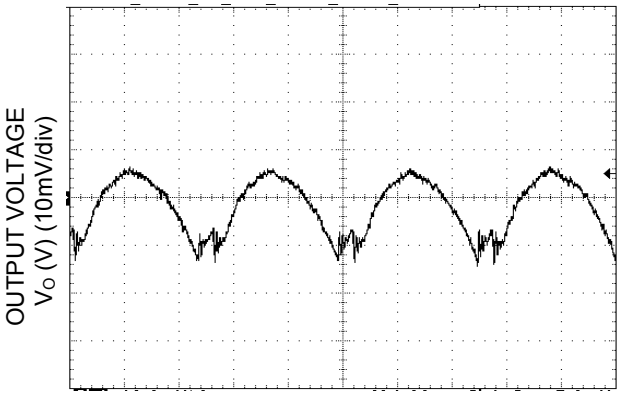


Fig-21. Typical output ripple and noise (CO=6x47µF ceramic, VIN = 12V, Io = Io,max,).

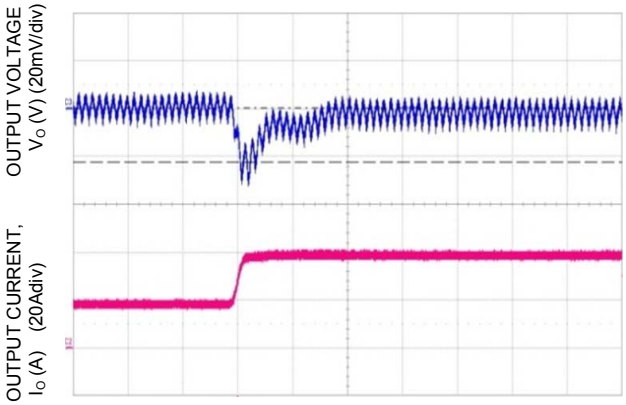


Fig-22. Transient Response to Dynamic Load Change from 50% to 100% at 12Vin, Cout= 6x330uF, CTune= 12nF & RTune= 200Ω

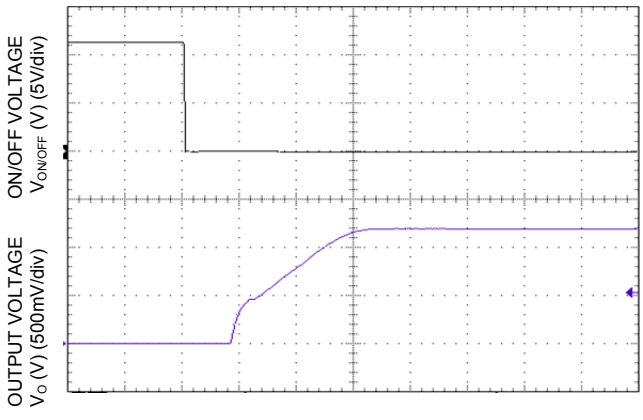


Fig-23. Typical Start-up Using On/Off Voltage (Io = Io,max).

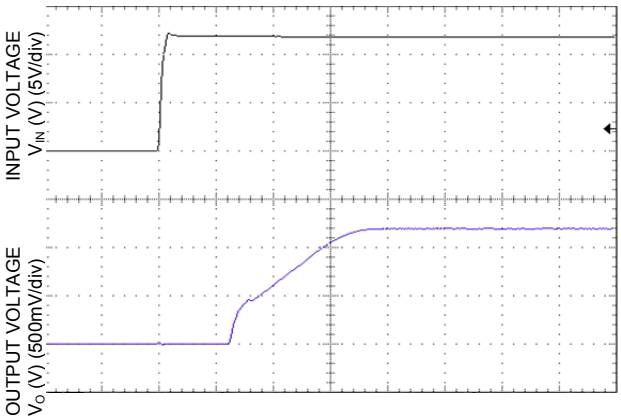


Fig-24. Typical Start-up Using Input Voltage (VIN = 12V, Io = Io,max).

FGLS12SR6040*A

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Data Sheet

Characteristic Curves

The following figures provide typical characteristics for the 40A Analog Tomodachi at 0.6Vo and 25°C

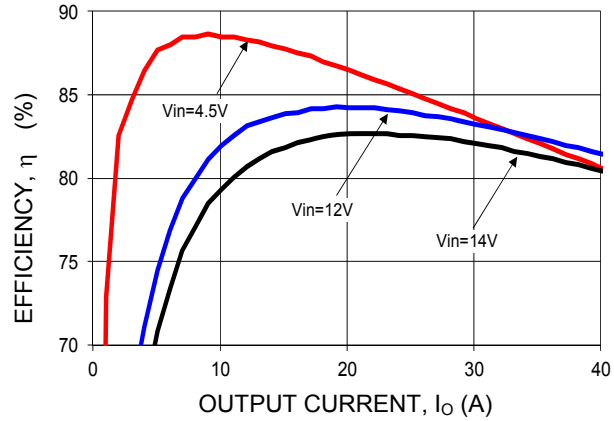


Fig-25. Converter Efficiency versus Output Current.

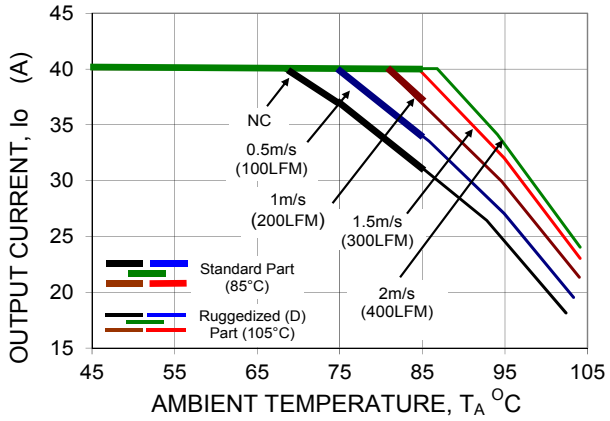


Fig-26. Derating Output Current versus Ambient Temperature and Airflow.

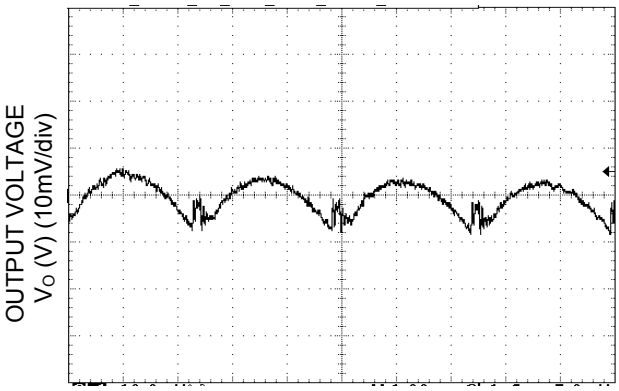


Fig-27. Typical output ripple and noise (CO=6x47uF ceramic, VIN = 12V, Io = Io,max,).

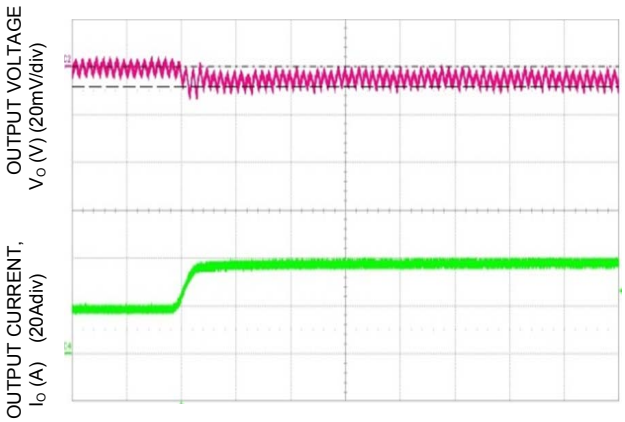


Fig-28. Transient Response to Dynamic Load Change from 50% to 100% at 12Vin, Cout= 12 x 680uF+6x47uF, CTune= 47nF & RTune= 180Ω

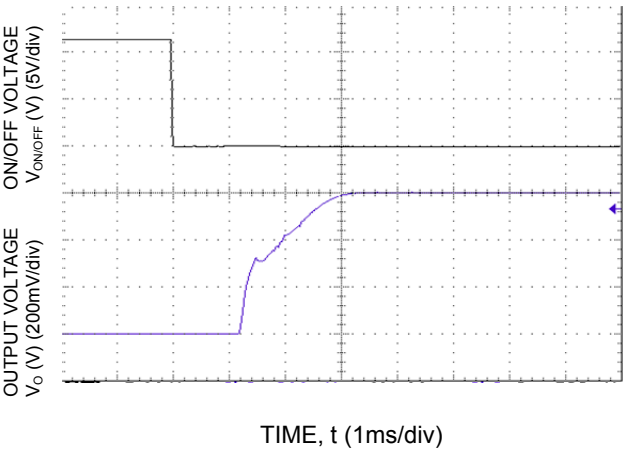


Fig-29. Typical Start-up Using On/Off Voltage (Io = Io,max).

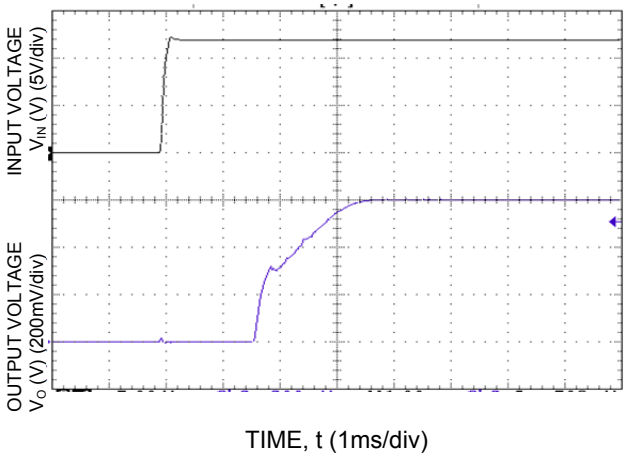


Fig-30. Typical Start-up Using Input Voltage (VIN = 12V, Io = Io,max).

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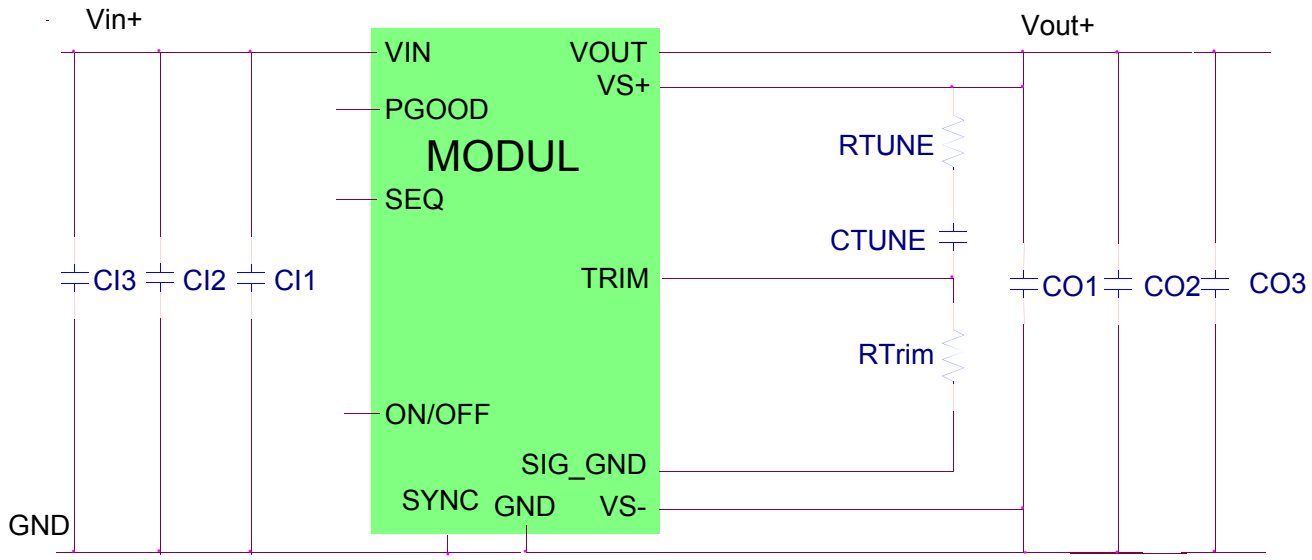
Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Example Application Circuit

Requirements:

Vin:	12V
Vout:	1.8V
Iout:	30A max., worst case load transient is from 20A to 30A
ΔVout:	1.5% of Vout (27mV) for worst case load transient
Vin, ripple	1.5% of Vin (180mV, p-p)



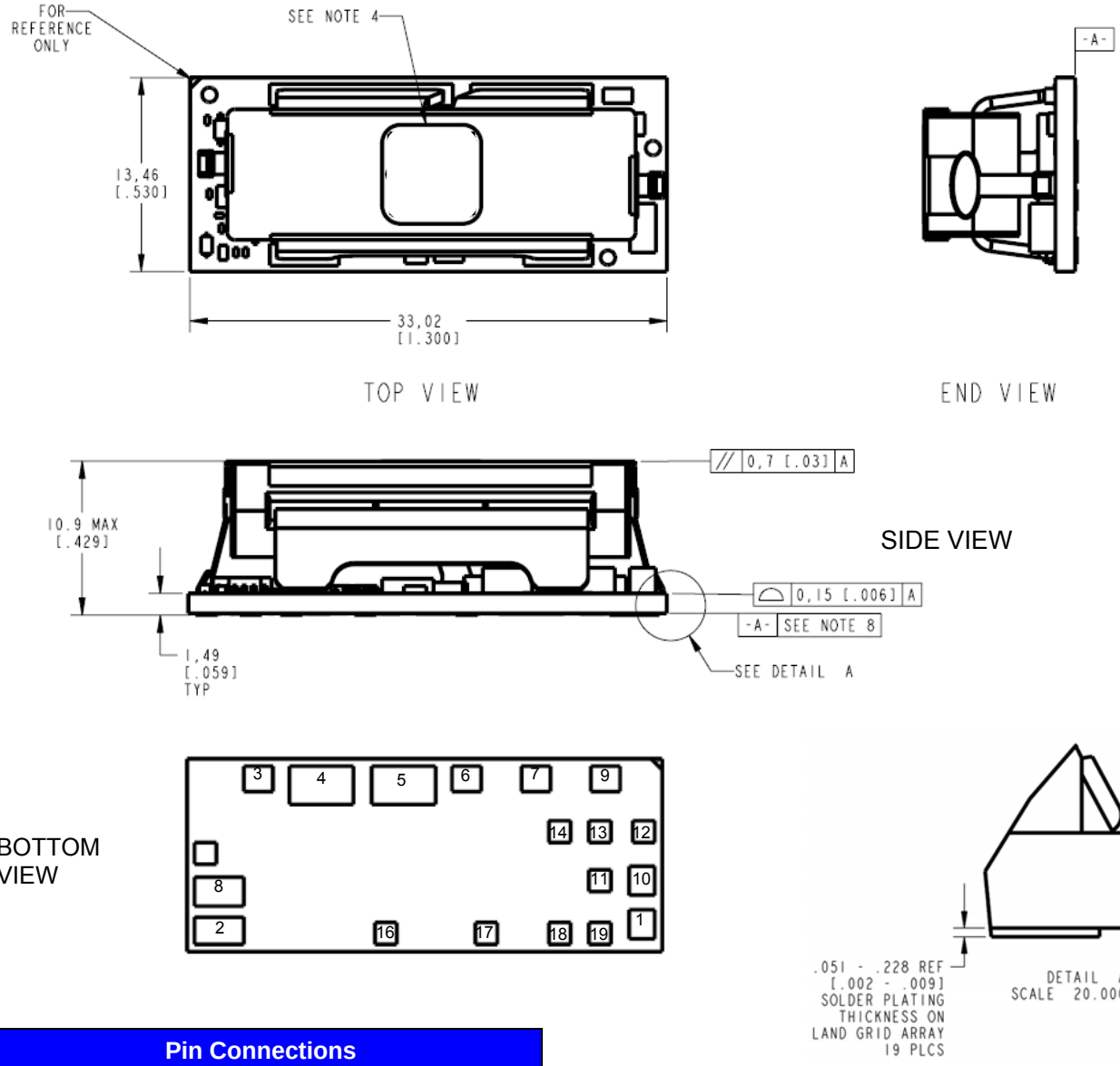
CI1	Decoupling cap - 1x0.01uF/16V ceramic capacitor (e.g. Murata LLL185R71E103MA01)
CI2	3x22uF/16V ceramic capacitor (e.g. Murata GRM32ER61C226KE20)
CI3	470uF/16V bulk electrolytic
CO1	Decoupling cap - 1x0.01uF/16V ceramic capacitor (e.g. Murata LLL185R71E103MA01)
CO2	4 x 47uF/6.3V ceramic capacitor (e.g. Murata GRM31CR60J476ME19)
CO3	6 X330uF/6.3V Polymer (e.g. Sanyo Poscap)
CTune	5600pF ceramic capacitor (can be 1206, 0805 or 0603 size)
RTune	220Ω SMT resistor (can be 1206, 0805 or 0603 size)
RTrim	10kΩ SMT resistor (can be 1206, 0805 or 0603 size, recommended tolerance of 0.1%)

FGLS12SR6040*A

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Data Sheet

Mechanical Drawing



Pin Connections			
Pin #	Function	Pin #	Function
1	ON/OFF	11	SIG_GND
2	Vin	12	VS-
3	SEQ	13	NC
4	GND	14	NC
5	Vout	15	SYNC *
6	TRIM	16	PG
7	VS+	17	NC
8	GND	18	NC
9	SHARE	19	NC
10	GND		

Notes

- All dimensions are in millimeters (inches)
- Tolerances:
  x.x mm ± 0.5 mm (x.xx in. ± 0.02 in.)
  [unless otherwise indicated]
  x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in.)

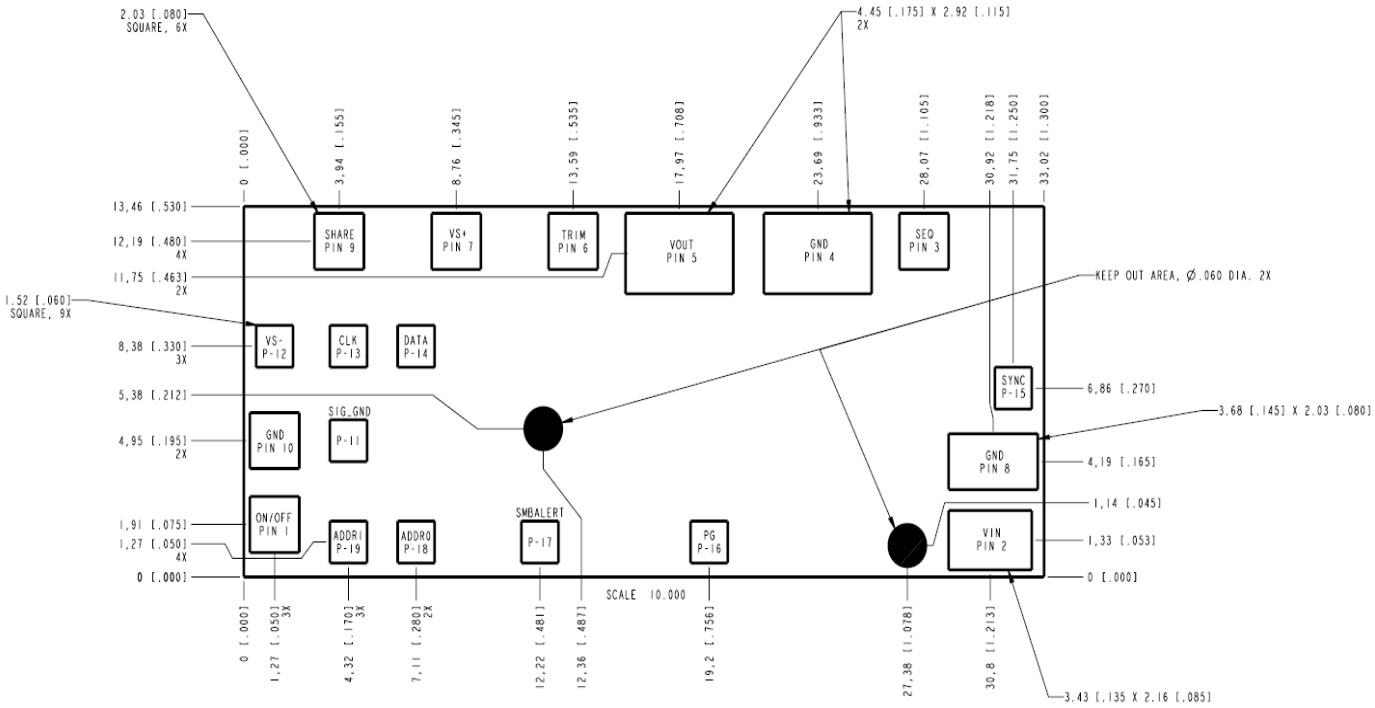
* If unused, connect to Ground

FGLS12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Recommended Pad Layout



Pin Connections			
Pin #	Function	Pin #	Function
1	ON/OFF	11	SIG_GND
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3	SEQ	13	NC
4	GND	14	NC
5	Vout	15	SYNC *
6	TRIM	16	PG
7	VS+	17	NC
8	GND	18	NC
9	SHARE	19	NC
10	GND		

Notes

- All dimensions are in millimeters (inches)
- Tolerances:
  x.x mm ± 0.5 mm (x.xx in. ± 0.02 in.)
  [unless otherwise indicated]
  x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in.)

* If unused, connect to Ground

FGLS12SR6040*A

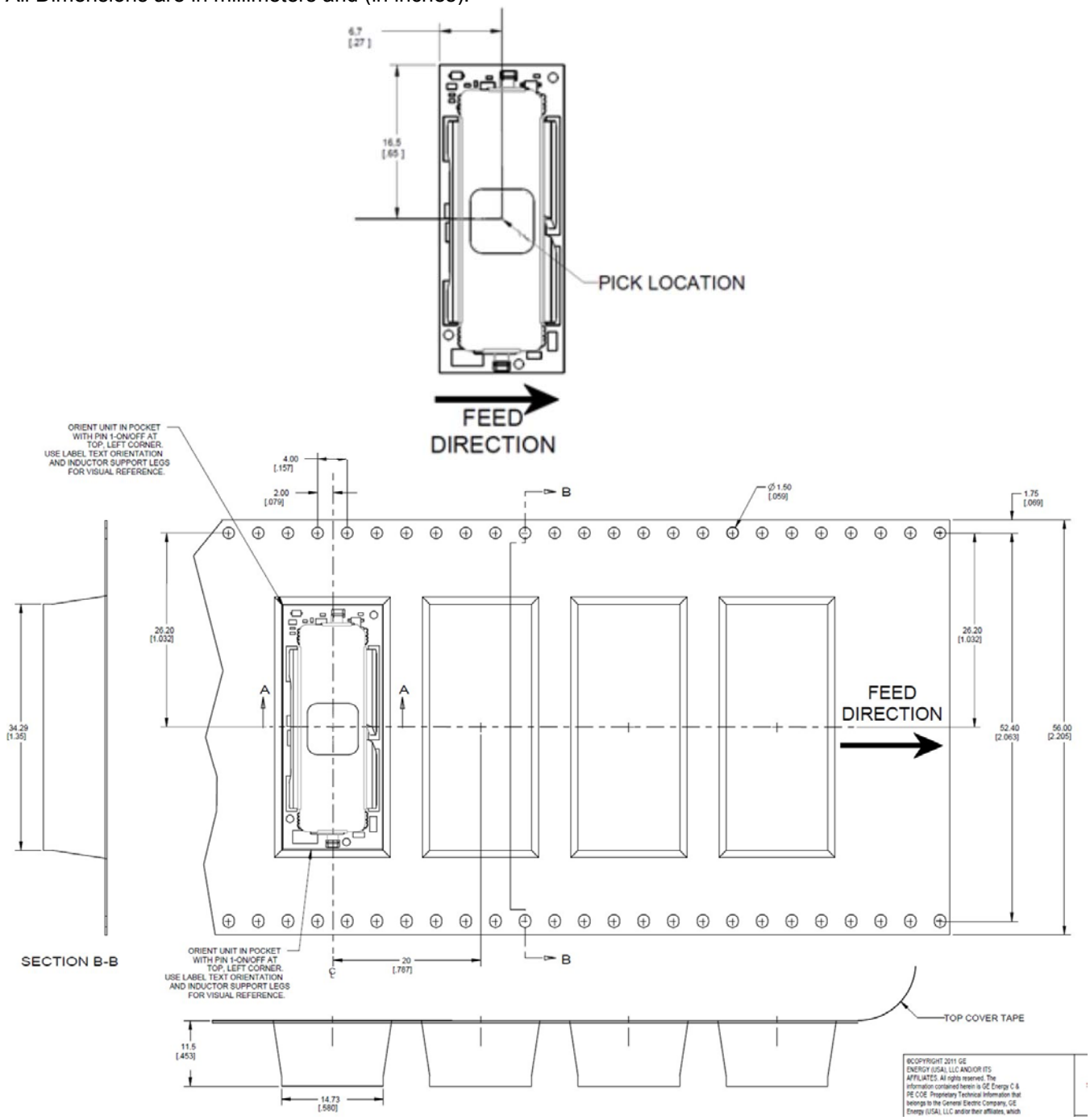
Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Packaging Details

The FGLS modules are supplied in tape & reel as standard. Modules are shipped in quantities of 140 modules per reel.

All Dimensions are in millimeters and (in inches).



Reel Dimensions:

Outside Dimensions:	330.2 mm (13.00)
Inside Dimensions:	177.8 mm (7.00”)
Tape Width:	56.00 mm (2.205”)

FGLS12SR6040*A

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Data Sheet

Surface Mount Information

Pick and Place

The 40A Analog ***Tomodachi*** modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300°C. The label also carries product information such as product code, serial number and the location of manufacture.

Nozzle Recommendations

The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7mm.

Bottom Side / First Side Assembly

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Lead Free Soldering

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. C (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). For questions regarding Land grid array (LGA) soldering, solder volume; please contact FDK for special manufacturing process instructions. The recommended linear reflow profile using Sn/Ag/Cu solder is shown in Fig-31. Soldering outside of the recommended profile requires testing to verify results and performance.

MSL Rating

The 40A Analog ***Tomodachi*** modules have a MSL rating of 2a.

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture / Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of ≤ 30°C and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40°C, < 90% relative humidity.

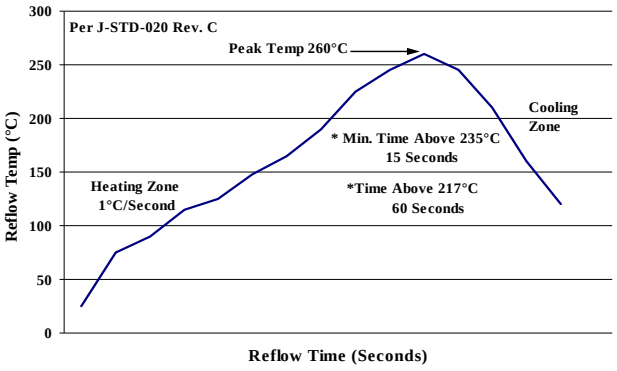


Fig-31: Recommended linear reflow profile using Sn/Ag/Cu solder.

Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to *Board Mounted Power Modules: Soldering and Cleaning Application Note (AN04-001).*

FGLS12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.6-2.0Vdc Output

Part Number System

Product Series	Shape	Regulation	Input Voltage	Mounting Scheme	Output Voltage	Rated Current	ON/OFF Logic	Pin Shape
FG	**L**	**S**	**12**	**S**	**R60**	**40**	*****	**A**
Series Name	Large	S: With tracking	Typ=12V	Surface Mount	0.60V (Programmable: See page 7)	40A	N: Negative P: Positive	Standard

Cautions

NUCLEAR AND MEDICAL APPLICATIONS: FDK Corporation products are not authorized for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems without the written consent of FDK Corporation.

SPECIFICATION CHANGES AND REVISIONS: Specifications are version-controlled, but are subject to change without notice.