Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

NXP Semiconductors
MC33390D

For any questions, you can email us directly:
sales@integrated-circuit.com

escale Semiconductor
Technical Data

Document Number: MC33390
Rev 7.0, 11/2006

Class B Serial Transceiver

33390

J-1850 SERIAL TRANSCEIVER

D SUFFIX
EF SUFFIX (PB-FREE)
98ASB42564B
8-LEAD SOICN

The 33390 is a serial transceiver designed to provide bi-directional half-duplex communication meeting the automotive SAE Standard J-1850 Class B Data Communication Network Interface specification. It is designed to interface directly to on-board vehicle microcontrollers and serves to transmit and receive data on a single-wire bus at data rates of 10.4 kbps using Variable Pulse Width Modulation (VPWM). The 33390 operates directly from a vehicle's 12 V battery system and functions in a logic fashion as an I/O interface between the microcontroller's 5.0 V CMOS logic level swings and the required 0 V to 7.0 V waveshaped signal swings of the bus. The bus output driver is short circuit current limited.

Features

- Designed for SAE J-1850 Class B Data Rates
- Full Operational Bus Dynamics Over a Supply Voltage of 9.0 to 16 V
- Ambient Operating Temperature of -40°C to 125°C
- Interfaces Directly to Standard 5.0 V CMOS Microcontroller
- BUS Pin Protected Against Shorts to Battery and Ground
- Thermal Shutdown with Hysteresis
- Voltage Waveshaping of Bus Output Driver
- 40 V Max V_{BAT} Capability
- Pb-Free Packaging Designated by Suffix Code EF

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33390D/DR2	-40°C to 125°C	8 SOICN
MCZ33390EF/R2		

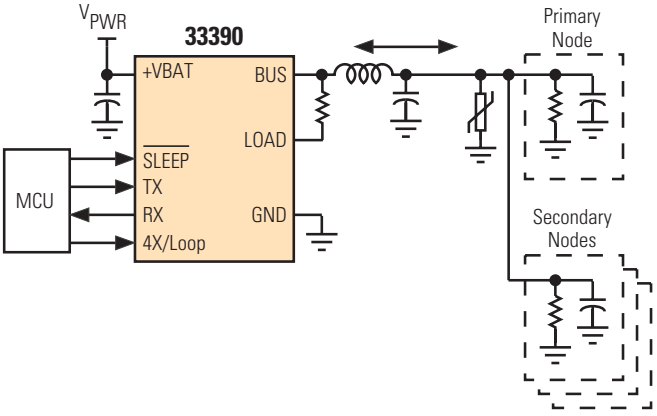
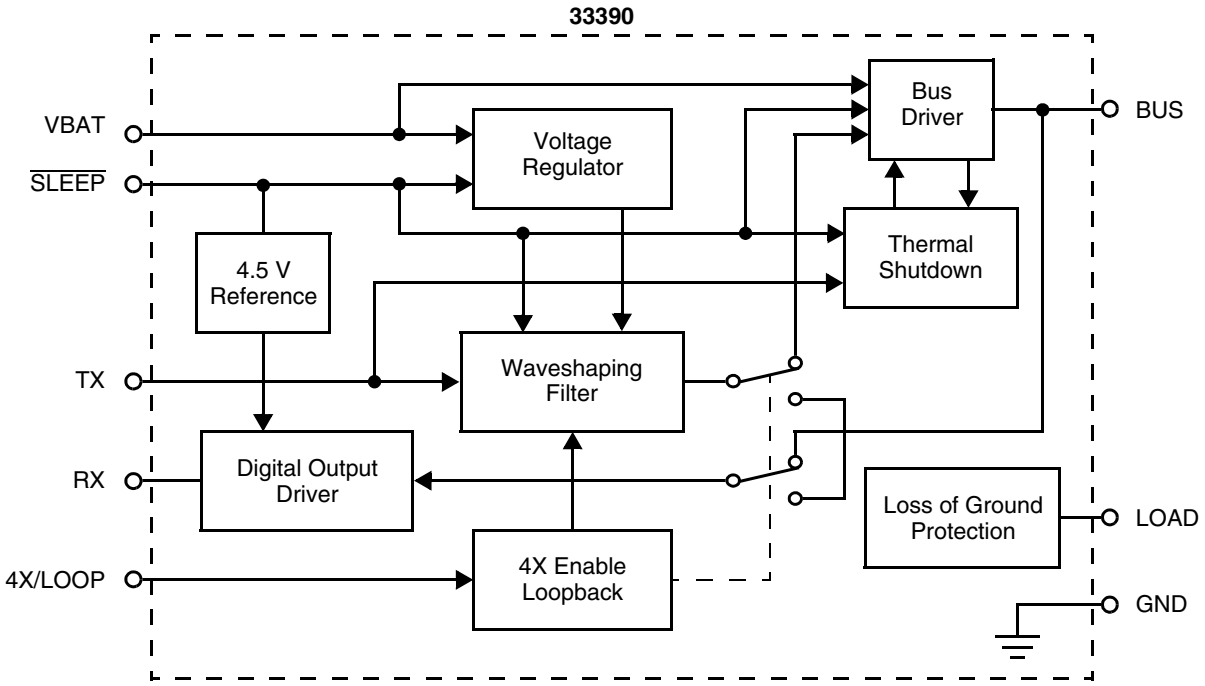


Figure 1. 33390 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM



Note This device contains approximately 400 active transistors and 250 gates.

Figure 2. 33390 Simplified Internal Block Diagram

PIN CONNECTIONS

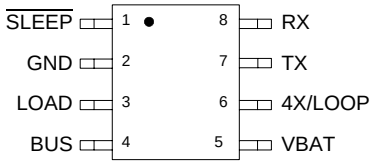


Figure 3. 33390 Pin Connections

Table 1. 33390 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 9.

Pin Number	Pin Name	Definition
1	$\overline{\text{SLEEP}}$	Enables the transceiver when Logic 1 and disables the transceiver when Logic 0.
2	GND	Device ground pin.
3	LOAD	Accommodates an external pull-down resistor to ground to provide loss of ground protection.
4	BUS	Waveshaped SAE Standard J-1850 Class B transmitter output and receiver input.
5	VBAT	Provides device operating input power.
6	4X/LOOP	Tristate input mode control; Logic 0 = normal waveshaping, Logic 1 = waveshaping disabled for 4X transmitting, high impedance = loopback mode.
7	TX	Serial data input (DI) from the microcontroller to be transmitted onto Bus.
8	RX	Bus received serial data output (DO) sent to the microcontroller.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
VBAT DC Supply Voltage (1)	V_{BAT}	-0.3 to 40	V
Input I/O Pins (2)	$V_{I/O(CPU)}$	-0.3 to 7.0	V
BUS and LOAD Outputs	V_{BUS}	-2.0 to 16	V
ESD Voltage (3) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Ambient Temperature	T_A	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Peak Package Reflow Temperature During Reflow (4), (5)	T_{PPRT}	Note 5.	°C
Thermal Resistance (Junction-to-Ambient)	$R_{\theta J-A}$	180	°C/W

Notes

1. An external series diode must be used to provide reverse battery protection of the device.
2. $\overline{SLEEP}$, TX, RX, and 4X/LOOP are normally connected to a microcontroller.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).
4. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
5. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions of 7.0 V ≤ V_{BAT} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, SLEEP = 5.0 V unless otherwise noted. Typical values reflect the parameter's approximate midpoint average value with V_{BAT} = 13 V, T_A = 25°C. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER CONSUMPTION					
Operational Battery Current (RMS with Tx = 7.812 kHz Square Wave)					mA
BUS Load = 1380 Ω to GND, 3.6 nF to GND	$I_{BAT(OP1)}$	–	3.0	11.5	
BUS Load = 257 Ω to GND, 20.2 nF to GND	$I_{BAT(OP2)}$	–	22.4	32	
Battery Bus Low Input Current					mA
After $\overline{SLEEP}$ Toggle Low to High; Prior to Tx Toggling	$I_{BAT(BUS\ L1)}$	–	1.1	3.0	
After Tx Toggle High to Low	$I_{BAT(BUS\ L2)}$	–	6.4	8.5	
Sleep State Battery Current	$I_{BAT(\overline{SLEEP})}$				µA
$V_{\overline{SLEEP}}$ = 0 V		–	38.2	65	
BUS					
BUS Input Receiver Threshold [6]					V
Threshold High (Bus Increasing until Rx ≥ 3.0 V)	$V_{BUS(IH)}$	4.25	3.9	–	
Threshold Low (Bus Decreasing until Rx ≤ 3.0 V)	$V_{BUS(IL)}$	–	3.7	3.5	
Threshold in Sleep State ($\overline{SLEEP}$ = 0 V)	$BUS_{TH(SLEEP)}$	2.4	3.0	3.4	
Hysteresis ($V_{BUS(IH)}$ - $V_{BUS(IL)}$, $\overline{SLEEP}$ = 0 V)	$V_{BUS(HYST)}$	0.1	0.2	0.6	
BUS-Out Voltage (257 Ω ≤ $R_{BUS(L)}$ to GND ≤ 1380 Ω)					V
8.2 V ≤ V_{BAT} ≤ 16 V, Tx = 5.0 V	$V_{BUS(OUT1)}$	6.25	6.9	8.0	
4.25 V ≤ V_{BAT} ≤ 8.2 V, Tx = 5.0 V	$V_{BUS(OUT2)}$	V_{BAT} - 1.6	–	V_{BAT}	
Tx = 0 V	$V_{BUS(OUT3)}$	–	0.27	0.7	
BUS Short Circuit Output Current	$I_{BUS(SHORT)}$				mA
Tx = 5.0 V, -2.0 V ≤ V_{BUS} ≤ 4.8 V		60	129	170	
BUS Leakage Current					µA
-2.0 V ≤ V_{BUS} ≤ 0 V	$I_{BUS(LEAK1)}$	-500	-55	–	
0 V ≤ V_{BUS} ≤ V_{BAT}	$I_{BUS(LEAK2)}$	–	189	500	
BUS Thermal Shutdown [7] (Tx = 5.0 V, I_{BUS} = -0.1 mA)	$T_{BUS(LIM)}$				°C
Increase Temperature until V_{BUS} ≤ 2.5 V		150	170	190	
BUS Thermal Shutdown Hysteresis [8]	$T_{BUS(LIMHYS)}$				°C
$T_{BUS(LIM)}$ - $T_{BUS(REEN)}$		10	12	15	
BUS and LOAD Current with Loss of V_{BAT} or GND (I_{BAT} = 0 µA) (see Figure 4)					mA
-18 V ≤ V_{BUS} ≤ 9.0 V	$I_{BUS(LOSS)}$	–	0.00	0.1	
-18 V ≤ V_{LOAD} ≤ 9.0 V	$I_{LOAD(LOSS)}$	–	0.00	0.1	

Notes
6. Typical threshold value is the approximate actual occurring switch point value with V_{BAT} = 13 V, T_A = 25°C.
7. Device characterized but not production tested for thermal shutdown.
8. Device characterized but not production tested for thermal shutdown hysteresis.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions of 7.0 V ≤ V_{BAT} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, SLEEP = 5.0 V unless otherwise noted. Typical values reflect the parameter's approximate midpoint average value with V_{BAT} = 13 V, T_A = 25°C. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS (CONTINUED)					
LOAD Output I_L = 6.0 mA	L_{ON}	–	0.07	0.2	V
Unpowered LOAD Output V_{BAT} = 0 V, I_L = 6.0 mA	L_{DIO}	0.3	0.56	0.9	V
TX					
Tx Input Voltage Tx Input Logic Low Level Tx Input Logic High Level	 $V_{Tx(IL)}$ $V_{Tx(IH)}$	 – 3.5	 – –	 0.8 –	V
Tx Input Current V_{Tx} = 5.0 V V_{Tx} = 0 V	 $I_{Tx(IH)}$ $I_{Tx(IL)}$	 50 -2.0	 106 0.23	 200 2.0	µA
LOOP					
4X/LOOP Input Current $V_{4X/LOOP}$ = 0 V (Normal Mode) $V_{4X/LOOP}$ = 5.0 V (4X Mode)	 $I_{4X/LOOP(IL)}$ $I_{4X/LOOP(IH)}$	 -200 -200	 -60 110	 200 200	µA
4X/LOOP Input Threshold (Tx = 4096 Hz Square Wave) Normal Mode to Loopback Mode Loopback Mode to 4X Mode	 $V_{4X/LOOP(IL)}$ $V_{4X/LOOP(IH)}$	 1.1 3.2	 1.31 3.43	 1.5 3.6	V
RX					
Rx Output Voltage Low V_{BUS} = 0 V, I_{Rx} = 1.6 mA	$V_{Rx(LOW)}$	0.01	0.18	0.4	V
Rx Output Voltage High V_{BUS} = 7.0 V, I_{Rx} = -200 µA	$V_{Rx(HIGH)}$	4.25	4.58	4.75	V
Rx Output Current V_{Rx} = High; Short Circuit Protection Limits	I_{Rx}	2.0	3.67	8.0	mA
SLEEP					
$\overline{SLEEP}$ Input Current V_{SLEEP} = 0 V V_{SLEEP} = 5.0 V	 $I_{SLEEP(IL)}$ $I_{SLEEP(IH)}$	 – 1.0	 -0.23 6.21	 -2.0 20	µA

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions of 7.0 V ≤ V_{BAT} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, $\overline{SLEEP}$ = 5.0 V unless otherwise noted. Typical values reflect the parameter's approximate midpoint average value with V_{BAT} = 13 V, T_A = 25°C. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS					
BUS Voltage Rise Time [9] (9.0 V ≤ V_{BAT} ≤ 16 V, Tx = 7.812 kHz Square Wave) (see Figure 5)	$t_{RISE(BUS)}$				µs
BUS Load = 3,300 pF and 1.38 kΩ to GND		9.0	11.15	15	
BUS Load = 16,500 pF and 300 Ω to GND		9.0	11.86	15	
BUS Voltage Fall Time [9] (9.0 V ≤ V_{BAT} ≤ 16 V, Tx = 7.812 kHz Square Wave) (see Figure 5)	$t_{FALL(BUS)}$				µs
BUS Load = 3,300 pF and 1.38 kΩ to GND		9.0	10.50	15	
BUS Load = 16,500 pF and 300 Ω to GND		9.0	11.17	15	
Pulse Width Distortion Time (9.0 V ≤ V_{BAT} ≤ 16 V, Tx = 7.812 kHz Square Wave) (see Figure 6)	$t_{PWD(BUS)}$				µs
BUS Load = 3,300 pF and 1.38 kΩ to GND		35	62	93	
Propagation Delay	$t_{PD(BUS)}$				µs
Tx Threshold to Rx Threshold		–	17.7	25	
TX					
Tx to BUS Delay Time (Tx = 2.5 V to V_{BUS} = 3.875 V) (see Figure 7)	$t_{TXDELAY}$				µs
4X Mode		–	2.6	4.0	
Normal Mode		13	17.3	24	
$\overline{SLEEP}$ to Tx Setup Time (see Figure 7)	$t_{\overline{SLEEP}TXSU}$	80	40	–	µs
RX					
Rx Output Delay Time (Tx = 2.5 V to V_{BUS} = 3.875 V) (see Figure 8)					µs
Low-to-Output High	$T_{RXDELAY/L–H}$	–	0.11	2.0	
High-to-Output Low	$T_{RXDELAY/H–L}$	–	0.38	2.0	
Rx Output Transition Time (C_{Rx} = 50 pF to GND, 10% and 90% Points) (see Figure 9)					µs
Low-to-Output High	$t_{RXTRANS/L–H}$	–	0.34	1.0	
High-to-Output Low	$t_{RXTRANS/H–L}$	–	0.08	1.0	
Rx Output Transition Time [10] (C_{Rx} = 50 pF to GND, $\overline{SLEEP}$ = 0 V, 10% and 90% Points) (see Figure 9)					µs
Low-to-Output High	$t_{RXTRANS/L–H}$	–	0.32	5.0	
High-to-Output Low	$t_{RXTRANS/H–L}$	–	0.08	5.0	

Notes
9. Typical is the parameter's approximate average value with V_{BAT} = 13 V, T_A = 25°C.
10. Rx Output Transition Time from a sleep state.

ELECTRICAL PERFORMANCE CURVES

TEST FIGURES

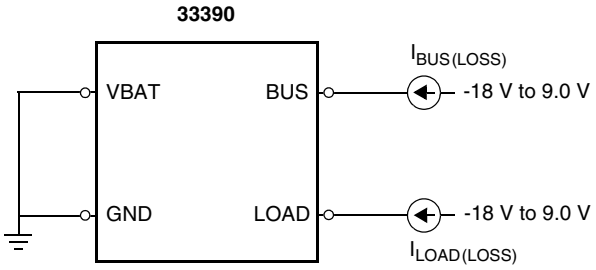


Figure 4. Loss of Ground or V_{BAT} Test Circuit

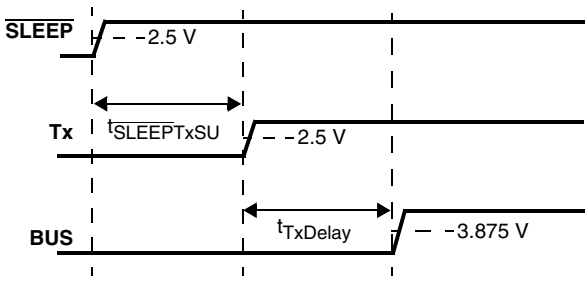


Figure 7. SLEEP to Tx Delay Times

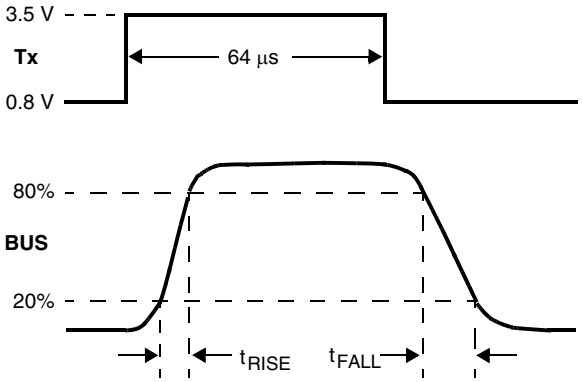


Figure 5. BUS Rise and Fall Times

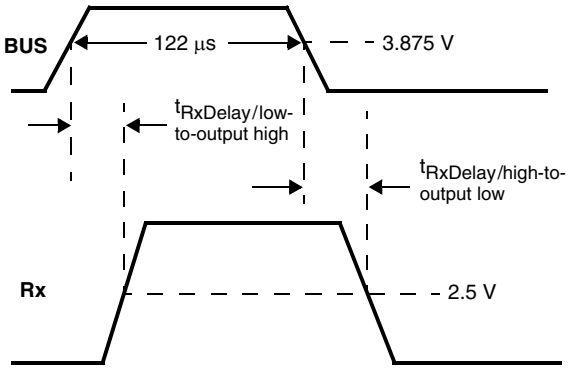


Figure 8. BUS-to-Rx Delay Time

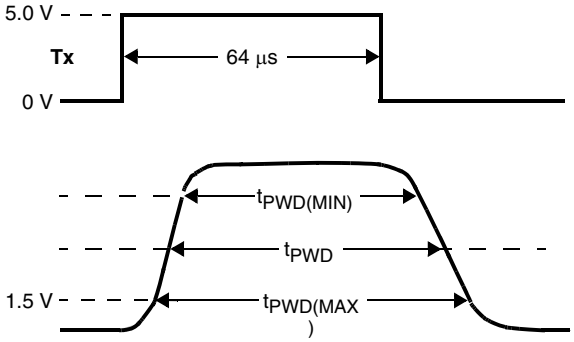


Figure 6. Pulse Width Distortion

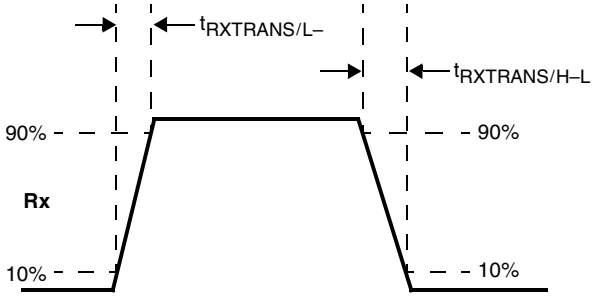


Figure 9. Rx Rise and Fall Time

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33390 is a serial transceiver device designed to meet the SAE Standard J-1850 Class B performance for bi-directional half-duplex communication. The device is packaged in an economical surface-mount SOIC plastic package. An internal block diagram of the device is shown in Figure 2.

The 33390 derives its robustness to temperature and voltage extremes from being built on a SMARTMOS process, incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Though the 33390 was principally designed for automotive applications requiring SAE J-1850 Class B standards, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of -40°C ≤ T_A ≤ 125°C and 7.0 V ≤ V_{BAT} ≤ 16 V supply. The economical 8-pin SOICN surface mount plastic package makes the device a cost-effective solution.

FUNCTIONAL PIN DESCRIPTION

Input Power (VBAT)

This is the only required input power source necessary to operate the 33390. The internal voltage reference of the 33390 will remain fully operational with a minimum of 9.0 V on this pin. Bus transmissions can continue with battery voltages down to 5.0 V. The bus output voltage will follow the battery voltage down and, in doing so, track approximately 1.6 V below the battery voltage. The device will continue to receive and transmit bus data to the microcontroller with battery voltages as low as 4.25 V. The pin can withstand voltages from -0.3 V to 40 V. If reverse battery protection is required, an appropriate diode must be placed in series with this pin to protect the IC.

Sleep Input ($\overline{\text{SLEEP}}$)

This input is used to enable and disable the Class B transmitter. The Class B receiver is always enabled so long as adequate V_{BAT} pin voltage is applied. When the $\overline{\text{SLEEP}}$ pin voltage is 5.0 V, the Class B transmitter is enabled. If this input is 0 V, the Class B transmitter will be disabled and less than 65 µA of current will be drawn by the V_{BAT} pin. The pin also provides a 5.0 V reference, internal to the device, used to establish the Rx output level and slew rate times.

Class B Functional Description

The transmitter provides an analog waveshaped 0 V to 7.0 V waveform on the BUS output. It also receives waveforms and transmits a digital level signal back to a logic IC. The transmitter can drive up to 32 secondary Class B transceivers (see Figures 10 and 11). These secondary nodes may be at ground potentials that are ±2.0 V relative to the control assembly. Waveshaping will only be maintained during 2 of the 4 corners when the 0 to ±2.0 V ground potential difference condition exists. The 33390 is a secondary node on the Class B bus. Each secondary transceiver has a 470 ±10% pF capacitor on its output for EMI suppression purposes, as well as a 10.6 kΩ ±5% pull-down resistor to ground. The primary node has a 3300 ±10% pF capacitor on its output for EMI suppression, as well as a 1.5 kΩ ±5% pull-down resistor to ground. With more than 26 nodes, there is no primary node (see Figure 12). All nodes will have a 470 ±10% pF capacitor and a 10.6 kΩ ±5% pull-down resistor. No matter how many secondary nodes are on the Class B bus, the RC time constant of the Class B bus is maintained at approximately 5.0 µs. The minimum and maximum capacitance and resistance on the Class B bus is given by the expressions shown in Table 5, page 10.

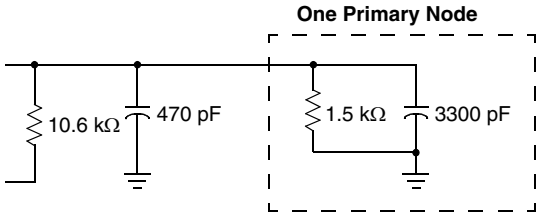


Figure 10. Minimum Bus Load

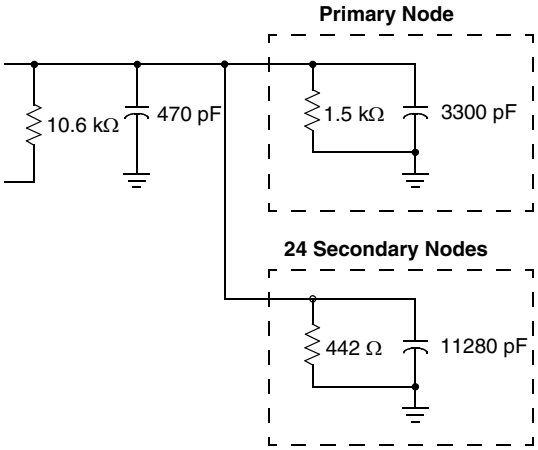


Figure 11. Maximum Number of Nodes

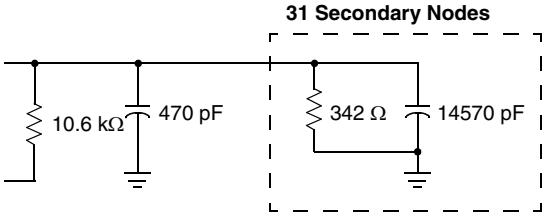


Figure 12. Maximum Bus Load

Table 5. Class B Bus Capacitance and Resistance Expressions

Level	Capacitance	Resistance to Ground
Minimum	(3.3 x 0.9) + (0.47 x 0.9) = 3.39 nF	(1.5 x 0.95) || (10.6 x 0.95) / 25 = 314 Ω
Maximum	(3.3 x 1.1) + 25(0.47 x 1.1) = 16.55 nF	(1.5 x 1.05) || (10.6 x 1.05) = 1.38 kΩ

TYPICAL APPLICATIONS

Class B Module Inputs

Transmitter Data from the MCU (Tx)

The Tx input is a push-pull (N-channel/P-channel FETs) buffer with hysteresis for noise immunity purposes. This pin is a 5.0 V CMOS logic level input from the MCU following a true logic protocol. A logic [0] input drives the BUS output to 0 V (via the external pull-down resistor to ground on each node), while a logic [1] input produces a high voltage at the BUS output. A logic [0] input level is guaranteed when the Tx input pin is open-circuited by virtue of an internal 40 kΩ pull-down resistor. No external resistor is required for its operation.

Waveshaping and 4X/Loop

This input is a tristateable input: 0 V = normal waveshaping, 5.0 V = waveshaping is disabled for 4X transmitting, and high impedance = loopback mode of operation. This is a logic level input used to select whether waveshaping for the Class B output is enabled or disabled. A logic [0] enables waveshaping, while a logic [1] disables waveshaping. In the 4X mode, the BUS output rise time is less than 2.0 µs and the fall time is less than 5.0 µs (owing to the external RC pull-down to ground). In the loopback condition, the Tx signal is fed back to the Rx output *after* waveshaping *without* being transmitted onto the BUS. This mode of operation is useful for system diagnostic purposes.

Class B Module Outputs

Transceiver Output (BUS)

This is the output driver stage that sources current to the bus. Its output follows the waveshaped waveform input. Its output voltage is limited to 6.25 V to 8.0 V under normal battery level conditions. The limited level is controlled by an internal regulator/clamp circuit. Once the battery voltage drops below 9.0 V, the regulator/clamp circuit saturates, causing the bus voltage to track the battery voltage. A 1.5 kΩ ±5% external resistor (as well as any 10.6 kΩ pull-down resistors of any secondary nodes) sinks the current to discharge the capacitors during high-to-low transitions. This sourcing output is short circuit-protected (60 mA to 170 mA) against a short to -2.0 V and sinks less than 1.0 mA when shorted to VBAT. If a short occurs, the overtemperature shutdown circuit protects the source driver of the device. In the event battery power is lost to the assembly, the bus transmitter's output stage will be disabled and the leakage current from the BUS output will not source or sink more than 100 µA of current. The transceiver will operate with a remote ground offset of ±2.0 V, but the lower corners of transmission will *not* be rounded during this condition.

Receiver Output to the Microcontroller (Rx)

This is a 5.0 V CMOS compatible push-pull output used to send received data to the microcontroller. It does not require an external pull-up resistor to be used. The receiver is always enabled and draws less than 65 µA of current from V_{BAT}. The receive threshold is dependent on the state of the $\overline{SLEEP}$ pin. The receiver circuitry is able to operate with V_{BAT} voltages as low as 4.25 V and still remains capable of “waking up” the 33390 when remote Class B activity is detected.

When the $\overline{SLEEP}$ pin is 0 V and message activity occurs on the bus, the receiver passes the bus message through to the microcontroller. The 33390 does not automatically “wake up” from a sleep state when bus activity occurs: the microcontroller must tell it to do so.

In the Static Electrical Characteristics table, the maximum voltage for Rx is specified as 4.75 V over an operating range of -40°C to 125°C temperature and 7.0 V to 16 V V_{BAT}. This maximum Rx voltage is compatible with the minimum V_{DD} voltage of microcontrollers to prevent the 33390 from sourcing current to the microcontroller's output.

Switched Ground Output (LOAD)

Normally this output is a saturated switch to ground, which pulls down the external resistor between the BUS and LOAD outputs. In the event ground is lost to the assembly, the LOAD output will bias itself “off” and will not leak more than 100 µA of current out of this pin.

Overtemperature Shutdown

If the BUS output becomes shorted to ground for any duration, an overtemperature shutdown circuit “latches off” the output source transistor whenever the die temperature exceeds 150°C to 190°C. The output transistor remains latched off until the Tx input is toggled from a logic [0] to a logic [1]. The rising edge provides the clearing function, provided the locally sensed temperature is 10°C to 15°C below the latch-off temperature trip temperature.

Waveshaping

Waveshaping is incorporated into the 33390 to minimize radiated EMI emissions.

Receiver Protocol

The Class B communication scheme uses a variable pulse width (VPW) protocol. The microcontroller provides the VPW decoding function. Once the receiver detects a transition on Rx, it starts an internal counter. The initial “start of frame” bit is a logic [1] and lasts 200 µs. For subsequent bits, if there is a bus transition before 96 µs, one logic state is inferred. If there is a bus transition after 96 µs, the other logic state is inferred. The “end of data” bit is a logic [0] and lasts 200 µs. If there is no activity on the bus for 280 µs to 320 µs following a broadcast message, multiple unit nodes may arbitrate for control of the next message. During an arbitration, after the

"start of frame" bit has been transmitted, the secondary node transmitting the most consecutive logic [0] bits will be granted sole transmission access to the bus for that message.

Loss of Assembly Ground Connection

The definition of a loss of assembly ground condition at the device level is that all pins of the 33390, with the exception of BUS and LOAD, see a very low impedance to VBAT.

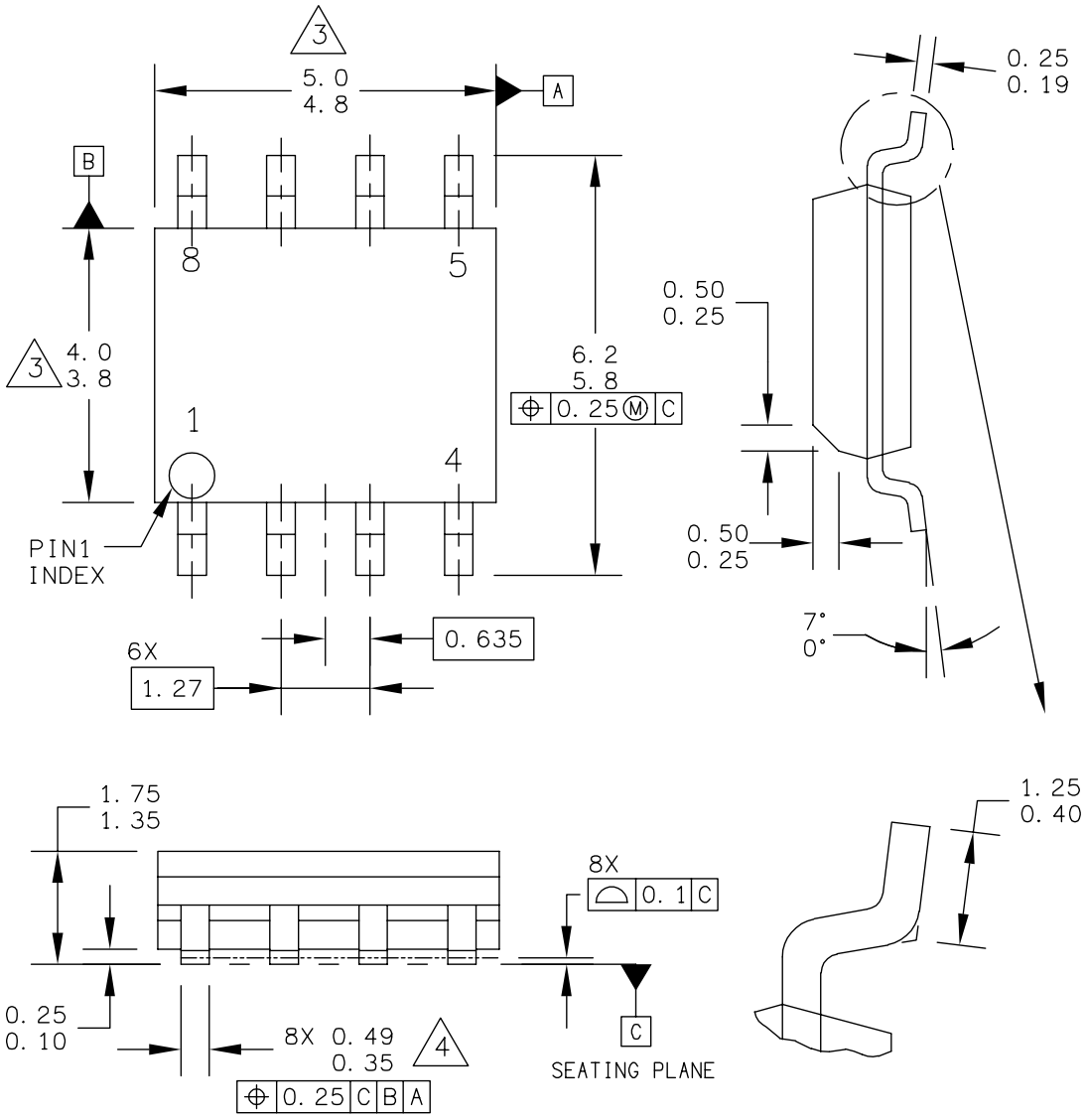
The LOAD pin of the device has an internal transistor switch connected to it that is normally saturated to ground. This pulls the LOAD-side of the external resistor (tied from BUS to LOAD) to ground under normal conditions. The LOAD pin switch is essentially that of an "upside down" FET, which is normally biased "on" so long as module ground is present and biased "off" when loss-of-ground occurs. When a loss of assembly ground occurs, the load transistor switch is self-biased "off", allowing no more than 100 µA of leakage current to flow in the LOAD pin. During such a loss of assembly ground condition, the BUS and LOAD pins exhibit a high impedance to VBAT; all other pins will exhibit a low impedance to V_{BAT}. During this condition the BUS pin is prevented from sourcing any current or loading the bus, which would cause a corruption of any data being transmitted on the bus. While a particular assembly is experiencing a loss of ground, all other assembly nodes are permitted to function normally. It should be noted that with other nodes existing on the bus, the bus will always have some minimum/maximum impedance to ground as shown in Table 5, page 10.

Loss of Assembly Battery Connection

The definition of a loss of assembly battery condition at the device level is that the VBAT pin of the 33390 sees an infinite impedance to VBAT, but there is some undefined impedance between these pins and ground.

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the 98A listed below.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: U
	CASE NUMBER: 751-07	07 APR 2005
	STANDARD: JEDEC MS-012AA	

EF SUFFIX (PB-FREE)
8-LEAD SOIC NARROW BODY
PLASTIC PACKAGE
98ASB42564B
ISSUE U

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
5.0	4/2006	• Converted to Freescale format • Implemented revision history page. • Added Part Numbers MC33390EF/EFR2 to Ordering Information on Page 1.
6.0	10/2006	• Updates document form and style • Removed MC33390EF and replaced with MCZ33390EF in the number Ordering Information
7.0	11/2006	• Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 4. Added note with instructions to obtain this information from www.freescale.com.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to http://www.freescale.com/epp.

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

MC33390
Rev 7.0
11/2006

freescale™ semiconductor