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[Pericom Semiconductor Corp.](#)  
[PI90LVB16L](#)

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## PI90LVB16

### 3V Bus LVDS 1-to-6 Clock Buffer/Bus Transceiver

#### Features

- Master/Slave clock selection in a backplane application
- 160 MHz operation (typical)
- 100ps duty cycle distortion (typical)
- 50ps channel to channel skew (typical)
- 3.3V power supply design
- Glitch-free power on at CLKI/O pins
- Low Power design (16mA @ 3.3V static)
- Accepts small swing (300mV typical) differential signal levels
- Industrial temperature operating range (-40°C to +85°C)
- Packaging: (Pb-free & Green available)
  - 24-pin TSSOP (L)

#### General Description

PI90LVB16 is a six-channel LVTTTL clock distribution driver with 50 picosecond channel-to-channel skew. It translates one BLVDS (Bus Low-Voltage Differential Signaling) input signal into six LVTTTL-compatible output signals for distribution to adjacent chips on the same board. The PI90LVB16 accepts BLVDS (300mV typical) differential input levels, and translates them to 3V CMOS output levels. The 160MHz PI90LVB16 can be the master clock, driving inputs of other clock I/O pins in a multipoint environment. It can also drive the BLVDS backplane with a separate channel acting as a return/source LVTTTL clock source. The master/slave clock selection of the driving source is controlled by the CrdCLK<sub>IN</sub> and the  $\overline{DE}$  pins. An output enable pin  $\overline{OE}$ , when high, forces all CLK<sub>OUT</sub> pins high.

A backplane clock distribution network must be able to drive many transmission line stubs. The Bus LVDS feature of the PI90LVB16 is ideal for driving data transfers in large, high-performance backplane system applications. The device can be used as a source synchronous driver to distribute clock signals within data and telecommunications systems.

#### Driver Mode Truth Table

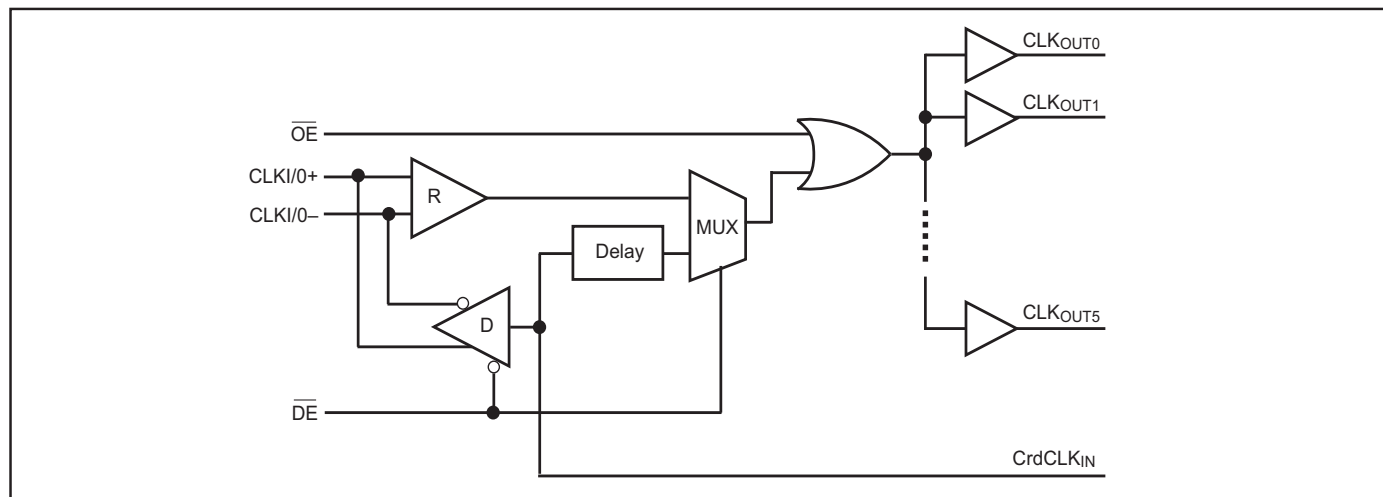
Input			Output		
$\overline{OE}$	$\overline{DE}$	CrdCLK <sub>IN</sub>	CLKI/O+	CLKI/O-	CLK <sub>OUT</sub>
L	L	L	L	H	L
L	L	H	H	L	H
H	L	L	L	H	H
H	L	H	H	L	H
H	H	X	Z	Z	H

#### Receive Mode Truth Table

Input				Output
$\overline{OE}$	$\overline{DE}$	CrdCLK <sub>IN</sub>	(CLKI/O+)-(CLKI/O-)	CLK <sub>OUT</sub>
H	H	X	X	H
L	H	X	VID ≥ 0.07V	H
L	H	X	VID ≤ -0.07V	L

L = Low Logic State; H = High Logic State; X = Irrelevant  
 Z = High Impedance

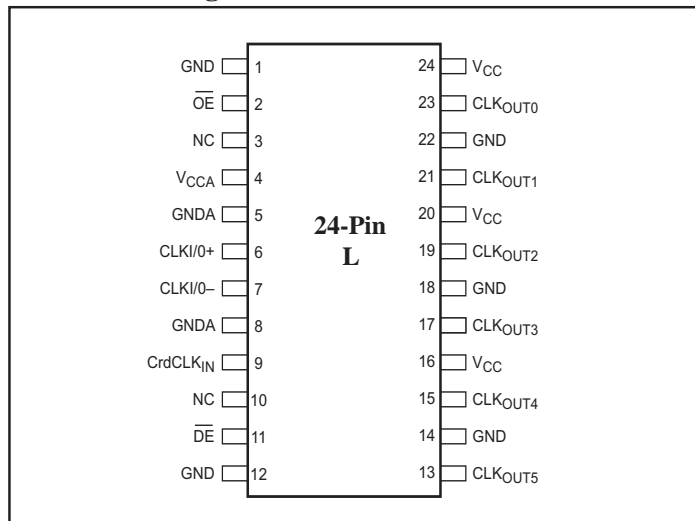
#### Function Diagram





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### Connection Diagram



### TSSOP Package Pin Description

Pin Name	Pin #	Type	Description
CLKI/O+	6	I/O	True (Positive) side of the differential clock input.
CLKI/O-	7	I/O	Complementary (Negative) side of the differential clock input.
$\overline{OE}$	2	I	$\overline{OE}$ ; this pin is active Low. When High, this pin forces all CLK <sub>OUT</sub> pin High. When Low, CLK <sub>OUT</sub> pins logic state is determined by either the CrdCLK <sub>IN</sub> or VID at the CLKI/O pins with respect to the logic level at the $\overline{DE}$ pin. This pin has a weak pullup device to V <sub>CC</sub> . If $\overline{OE}$ is floating, then all CLK <sub>OUT</sub> pins will be High.
$\overline{DE}$	11	I	$\overline{DE}$ ; this pin is active Low. When Low, this pin enables the CardCLK <sub>IN</sub> signal to the CLKI/O pins and CLK <sub>OUT</sub> . When High the Driver is 3-State, the CLKI/O pins are inputs and determine the state of the CLK <sub>OUT</sub> pins. This pin has a weak pullup device to V <sub>CC</sub> . If $\overline{DE}$ is floating, then all CLKI/O pins are 3-State.
CLK <sub>OUT</sub>	13,15,17,19,21,23	O	Six Buffered clock (CMOS) outputs.
CrdCLK <sub>IN</sub>	9	I	Input clock from Card (CMOS level or TTL level).
V <sub>CC</sub>	16,20,24	Power	V <sub>CC</sub> ; Analog V <sub>CCA</sub> (Internally separate from V <sub>CC</sub> , connect externally or use separate power supplies). No special power sequencing required. Either V <sub>CCA</sub> or V <sub>CC</sub> can be applied first, or simultaneously apply both power supplies.
GND	1,12,14,18,22	Ground	GND
V <sub>CCA</sub>	4	Power	Analog V <sub>CCA</sub> (Internally separate from V <sub>CC</sub> , connect externally or use separate power supplies). No special power sequencing required. Either V <sub>CCA</sub> or V <sub>CC</sub> can be applied first, or simultaneously apply both power supplies.
GNDA	5,8	Ground	Analog Ground (Internally separate from Ground must be connected externally).
NC	3,10		No Connects.



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### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage Range, $V_{CC}$ .....	-0.3V to +4V
Enable Input Voltage (DE, OE, CrdCLK <sub>IN</sub> ) .....	-0.3V to +4V
Voltage (CLK <sub>OUT</sub> ) .....	-0.3V to ( $V_{CC} + 0.3V$ )
Voltage (CLKI/O $\pm$ ) .....	-0.3V to ( $V_{CC} + 0.3V$ )
Driver Short Circuit Current .....	momentary
Receiver Short Circuit Current .....	momentary
Maximum Package Power Dissipation at +25°C	
TSSOP Package .....	1500mW
Derate TSSOP Package .....	8.2mW/°C above +25°C
$\theta_{JA}$ .....	95°C/W
$\theta_{JC}$ .....	30°C/W
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature Range (Soldering, 4s) .....	260°C
ESD Ratings: HBM <sup>(2)</sup> .....	9kV
CLK <sub>OUT(0-5)</sub> .....	$\geq 2kV$
CDM <sup>(2)</sup> .....	>1000V
Machine Model <sup>(2)</sup> .....	>200V

### Recommended Operating Conditions

	Min.	Typ.	Max	Units
Supply Voltage ( $V_{CC}$ )	+3.0	+3.3	+3.6	V
CrdCLK <sub>IN</sub> , $\overline{DE}$ , $\overline{OE}$ Input Voltage	0		$V_{CC}$	V
Operating Free Air Temperature ( $T_A$ )	-40	24	+85	°C



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### DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(3,4)</sup>

Symbol	Parameter	Conditions	Pin	Min.	Typ.	Max.	Units
V <sub>TH</sub>	Input Threshold High		CLKI/O+, CLKI/O-		25	75	mV
V <sub>TL</sub>	Input Threshold Low			-70	-35		
V <sub>CMR</sub>	Common Mode Voltage Range <sup>(5)</sup>	VID = 250mV peak-to-peak			V <sub>ID</sub>  /2		2.8 –  V <sub>ID</sub>  /2
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> , $\overline{DE} = V_{CC}$ , $\overline{OE} = V_{CC}$ , Other Input = 1.2V ±50mV		-10	±5	+10	µA
V <sub>OH1R</sub>	Output High Voltage	VID =250mV, I <sub>OH</sub> = -1.0mA	CLK <sub>OUT</sub>	V <sub>CC</sub> -0.2	2.9		V
V <sub>OH2R</sub>	Output High Voltage	VID =250mV, I <sub>OH</sub> = -6mA		V <sub>CC</sub> -0.6	2.5		
V <sub>OL1R</sub>	Output Low Voltage	I <sub>OL</sub> =1.0mA, VID = -250mV			0.04	0.1	
V <sub>OL2R</sub>	Output Low Voltage	I <sub>OL</sub> =6mA, VID = -250mV		0	0.22	0.4	
I <sub>ODHR</sub>	CLK <sub>OUT</sub> Dynamic Output Current <sup>(6)</sup>	VID = +250mV, V <sub>OUT</sub> = V <sub>CC</sub> -1V		-16	-24	-34	mA
I <sub>ODLR</sub>		VID = -250mV, V <sub>OUT</sub> = 1V		14	25	37.5	
V <sub>IH</sub>	Input High Voltage		$\overline{DE}$ , $\overline{OE}$ , CrdCLK <sub>IN</sub>	2.0		V <sub>CC</sub>	V
V <sub>IL</sub>	Input Low Voltage			GND		0.8	
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = V <sub>CC</sub> or 2.4V	$\overline{OE}$ , $\overline{DE}$	-6	4	6	µA
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = GND or 0.4V		-20	11	+20	
I <sub>INCRD</sub>	Input Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> , $\overline{OE} = V_{CC}$	CrdCLK <sub>IN</sub>	-5		5	
V <sub>CL</sub>	Input Voltage Clamp	I <sub>OUT</sub> = -1.5mA	$\overline{OE}$ , $\overline{DE}$ , CrdCLK <sub>IN</sub>	-0.8			V
I <sub>CC</sub>	No Load Supply Current Outputs Enabled, No VID Applied	$\overline{OE} = \overline{DE} = 0V$ , CrdCLK <sub>IN</sub> = V <sub>CC</sub> or GND, CLKI/O(±) = Open CLK <sub>OUT</sub> (0:5) = Open Circuit	V <sub>CC</sub>			10	mA
I <sub>CC1</sub>	No Load Supply Current Outputs Enabled, VID over Common Voltage Range	$\overline{OE} = GND$ , $\overline{DE} = V_{CC}$ , CrdCLK <sub>IN</sub> = V <sub>CC</sub> or GND, VID = 250mV (0.125V VCM 2.275V) CLK <sub>OUT</sub> (0:5) = Open Circuit				6	
I <sub>CCD</sub>	Driver Loaded Supply Current	$\overline{DE} = \overline{OE} = 0V$ , CrdCLK <sub>IN</sub> = V <sub>CC</sub> or GND, R <sub>L</sub> = 37.5Ω between CLKI/O+ and CLKI/O-, CLK <sub>OUT</sub> (0:5) = Open Circuit			16		



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**DC Electrical Characteristics** (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(3,4)</sup>

Symbol	Parameter	Conditions	Pin	Min.	Typ.	Max.	Units
V <sub>OD</sub>	Driver Output Differential Voltage	$R_L = 37.5\Omega$ , Figure 5 $\overline{DE} = 0V$	CLKI/O+, CLKI/O-	250	350	450	mV
$\Delta V_{OD}$	Driver V <sub>OD</sub> Magnitude Change				2	20	
V <sub>OS</sub>	Driver Offset Voltage			1.1	1.25	1.5	V
$\Delta V_{OS}$	Driver Offset Voltage Multitude Change				1	20	mV
V <sub>OHD</sub>	Driver Output High				1.4	1.8	V
V <sub>OLD</sub>	Driver Output Low				0.8	1.05	
I <sub>OS1D</sub>	Driver Differential Short Circuit Current <sup>(6)</sup>	CrdCLK <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>OD</sub> = 0V, (outputs shorted together), $\overline{DE} = 0V$			$\pm 13$	$\pm 17$	mA
I <sub>OS2D</sub>	Driver Differential Short Circuit Current to V <sub>CC</sub> <sup>(6)</sup>	CrdCLK <sub>IN</sub> = GND, $\overline{DE} = 0V$ , CLKI/O+ = V <sub>CC</sub>			11	17	
I <sub>OS3D</sub>		CrdCLK <sub>IN</sub> = V <sub>CC</sub> , $\overline{DE} = 0V$ , CLKI/O- = V <sub>CC</sub>			10	17	
I <sub>OS4D</sub>	Driver Differential Short Circuit Current to GND <sup>(6)</sup>	CrdCLK <sub>IN</sub> = V <sub>CC</sub> , $\overline{DE} = 0V$ , CLKI/O+ = 0V			-15	-17	
I <sub>OS5D</sub>		CrdCLK <sub>IN</sub> = GND, $\overline{DE} = 0V$ , CLKI/O- = 0V			-15	-17	
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>CC</sub> = 0V or Open, V <sub>APPLIED</sub> = 3.6V			$\pm 20$	$\mu A$	

**Switching Characteristics**

**Differential Receiver Characteristics**

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(7,8)</sup>

Symbol	Parameter	Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units	
t <sub>PHLDR</sub>	Differential Propagation Delay High to Low. CLK <sub>I/O</sub> to CLK <sub>OUT</sub>	$C_L = 15pF$ VID = 250mV Figures 1 & 2	1.3	2.6	3.8	ns	
t <sub>PLHDR</sub>	Differential Propagation Delay Low to High. CLK <sub>I/O</sub> to CLK <sub>OUT</sub>		1.3	2.6	3.8		
t <sub>SK1R</sub>	Duty Cycle Distortion <sup>(10)</sup> pulse skew,  t <sub>PLH</sub> - t <sub>PHL</sub>			5	400	ps	
t <sub>SK2R</sub>	Channel-to-Channel Skew; Same Edge <sup>(11)</sup>			5	80		
t <sub>SK3R</sub>	Part-to-Part Skew <sup>(12)</sup>				TBD	ns	
t <sub>TLHR</sub>	Transition Time Low-to-High <sup>(9)</sup> , (20% to 80%)			1.0	1.4		2.4
t <sub>THLR</sub>	Transition Time High-to-Low <sup>(9)</sup> , (80% to 20%)			1.0	1.3		2.4
t <sub>PLHOER</sub>	Propagation Delay Low-to-High ( $\overline{OE}$ to CLK <sub>OUT</sub> )	$C_L = 15pF$ Figures 3 & 4	1.0	2.1	3.2		
t <sub>PHLOER</sub>	Propagation Delay High-to-Low ( $\overline{OE}$ to CLK <sub>OUT</sub> )		1.0	2.1	3.2		
f <sub>MAX</sub>	Maximum Operating Frequency <sup>(15)</sup>		100	160		MHz	



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### Switching Characteristics

#### Differential Driver Timing Requirements

(Over supply voltage and operating temperature ranges, unless otherwise specified<sup>(7,8)</sup>)

Symbol	Parameter	Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units
t <sub>PHLDD</sub>	Differential Propagation Delay High to Low. CrdCLK <sub>IN</sub> to CLKI/O	C <sub>L</sub> = 15pF R <sub>L</sub> = 37.5Ω Figures 6 & 7	1.0	1.5	2.2	ns
t <sub>PLHDD</sub>	Differential Propagation Delay Low to High. CrdCLK <sub>IN</sub> to CLKI/O		1.0	1.3	2.2	
t <sub>PHLCrd</sub>	CrdCLK <sub>IN</sub> to CLK <sub>OUT</sub> Propagation Delay High to Low	C <sub>L</sub> = 15pF Figures 8 & 9	2.0	2.8	4.5	ns
t <sub>PLHCrd</sub>	CrdCLK <sub>IN</sub> to CLK <sub>OUT</sub> Propagation Delay Low to High		2.0	2.8	4.5	
t <sub>SK1D</sub>	Differential Skew  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>(13)</sup>	C <sub>L</sub> = 15pF Figures 6 & 7			600	ps
t <sub>SK2D</sub>	Differential Part-to-Part Skew <sup>(14)</sup>				TBD	ns
t <sub>TLHD</sub>	Differential Transition Time <sup>(9)</sup> , (20% to 80%)		0.2	0.35	0.65	
t <sub>THLD</sub>	Differential Transition Time <sup>(9)</sup> , (80% to 20%)		0.2	0.35	0.65	
t <sub>PHZD</sub>	Transition Time Low to 3-State. $\overline{DE}$ to CLKI/O	V <sub>IN</sub> = 0V to V <sub>CC</sub> C <sub>L</sub> = 15pF R <sub>L</sub> = 37.5Ω Figures 10 & 11			2.6	ns
t <sub>PLZD</sub>	Transition Time Low to 3-State. $\overline{DE}$ to CLKI/O				2.6	
t <sub>PZHD</sub>	Transition Time 3-State-to-High. $\overline{DE}$ to CLKI/O				4.3	
t <sub>PZLD</sub>	Transition Time 3-State-to-Low. $\overline{DE}$ to CLKI/O				3.6	
f <sub>MAX</sub>	Maximum Operating Frequency <sup>(15)</sup>		100	160		MHz

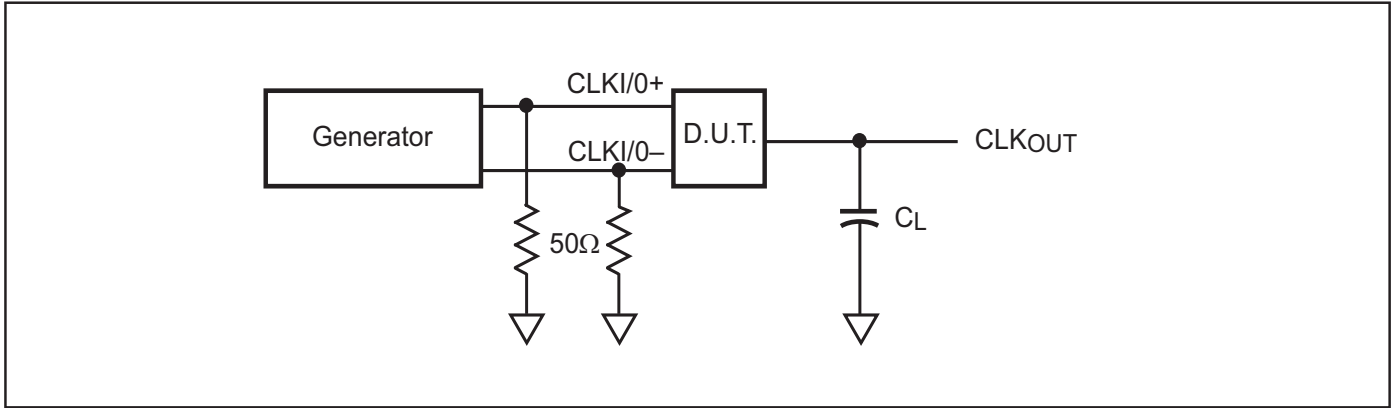
#### Notes:

- “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. These ratings are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
- ESD Rating: ESD qualification is performed per the following: HBM (1.5kΩ, 100pF), Machine Model (250V, 0Ω), IEC 1000-4-2. All V<sub>CC</sub> pins connected together, all ground pins connected together.
- Current into device pins are defined as positive. Current out of device pins defined as negative. All voltages are referenced to ground except VID, VOD, VTH, and VTL
- All typicals are given for: V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C.
- The VCMR range is reduced for larger VID. Example: If VID=400 mV, then VCMR is 2V to 2.2V<sub>AVID</sub> up to |V<sub>CC</sub>-0V| may be applied between the CLKI/O+ and CLKI/O- inputs, with the Common Mode set to V<sub>CC</sub>/2.
- Only one output should be momentarily shorted at a time. Do not exceed package power dissipation rating.
- C<sub>L</sub> includes probe and fixture capacitance.
- Generator waveform for all tests unless otherwise specified: f = 25 MHz, Z<sub>o</sub> = 50Ω, t<sub>r</sub> = 1ns, t<sub>f</sub> = 1ns (10%–90%). To ensure fastest propagation delay and minimum skew, clock input edge rates should not be slower than 1ns/V; control signals not slower than 3ns/V. In general, the faster the input edge rate, the better the AC performance,
- All device output transition times are based on characterization measurements and are guaranteed by design.
- t<sub>SK1R</sub> is the difference in receiver propagation delay |t<sub>PLH</sub>-t<sub>PHL</sub>| of one device, and is the duty cycle distortion of the output at any given temperature and V<sub>CC</sub>. The propagation delay specification is a device-to-device worst case over process, voltage and temperature.
- t<sub>SK2R</sub> is the difference in receiver propagation delay between channels in the same device of any outputs switching in the same direction. This parameter is guaranteed by design and characterization.
- t<sub>SK3R</sub> part-to-part skew, is the difference in receiver propagation delay between devices of any outputs switching in the same direction. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t<sub>SK3R</sub> is defined as Max-Min differential propagation delay. This parameter is guaranteed by design and characterization.
- t<sub>SK1D</sub> is the difference in driver propagation delay |t<sub>PLH</sub>-t<sub>PHL</sub>| and is the duty cycle distortion of the CLKI/O outputs.
- t<sub>SK2D</sub> part-to-part skew, is the difference in driver propagation delay between devices of any outputs switching in the same direction. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t<sub>SK2D</sub> is defined as Max-Min differential propagation delay.
- Generator input conditions: t<sub>r</sub>t<sub>f</sub> < 1ns, 50% duty cycle, differential (1.10V to 1.35V pk-pk). Output Criteria: 60%/40% duty cycle, V<sub>OL</sub>(max) 0.4V, V<sub>OH</sub>(min) 2.7V, Load - 7pF (stray plus probes).

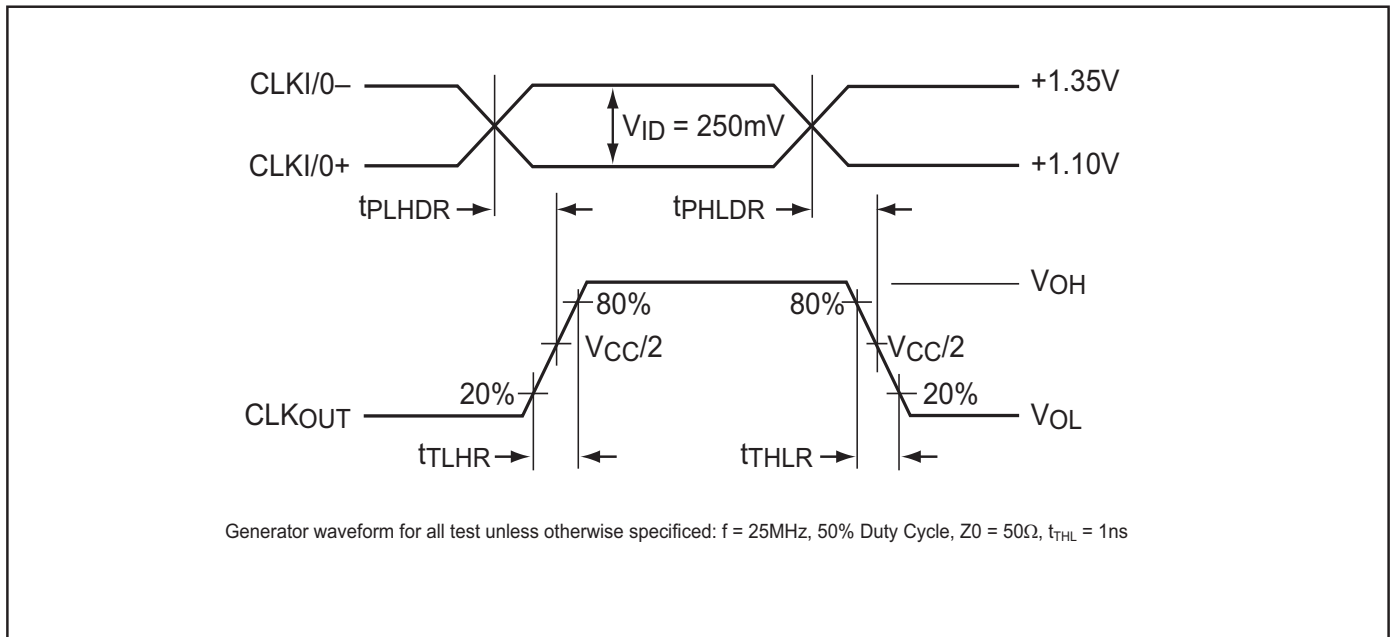


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**Parameter Measurement Information**



**Figure 1. Receiver Propagation Delay and Transition Time Test Circuit**



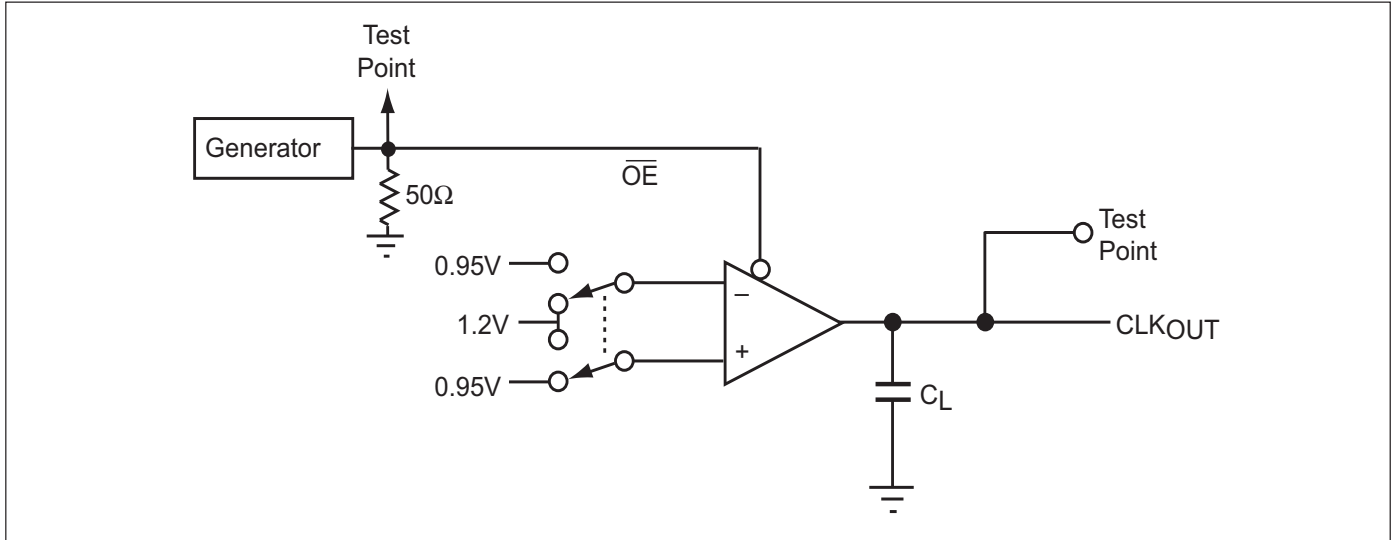
**Figure 2. Receiver Propagation Delay and Transition Time Waveforms**



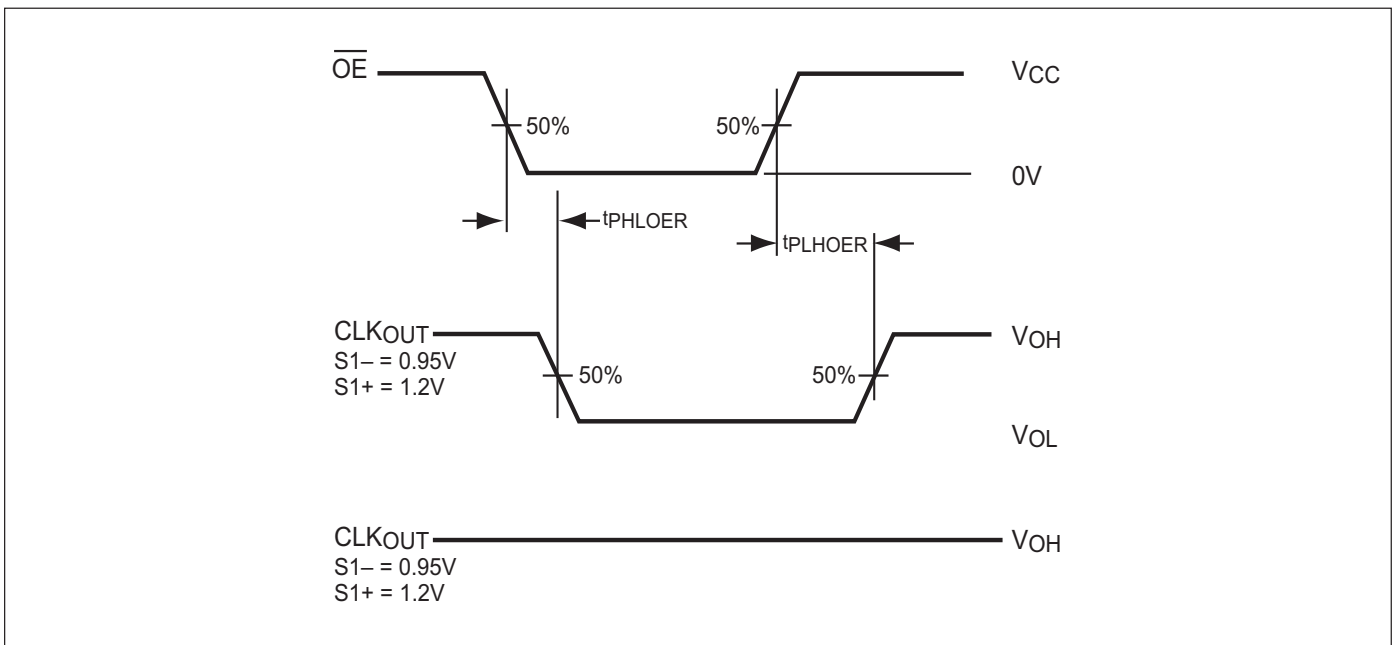


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**Parameter Measurement Information**



**Figure 3. Output Enable ( $\overline{OE}$ ) Test Circuit**

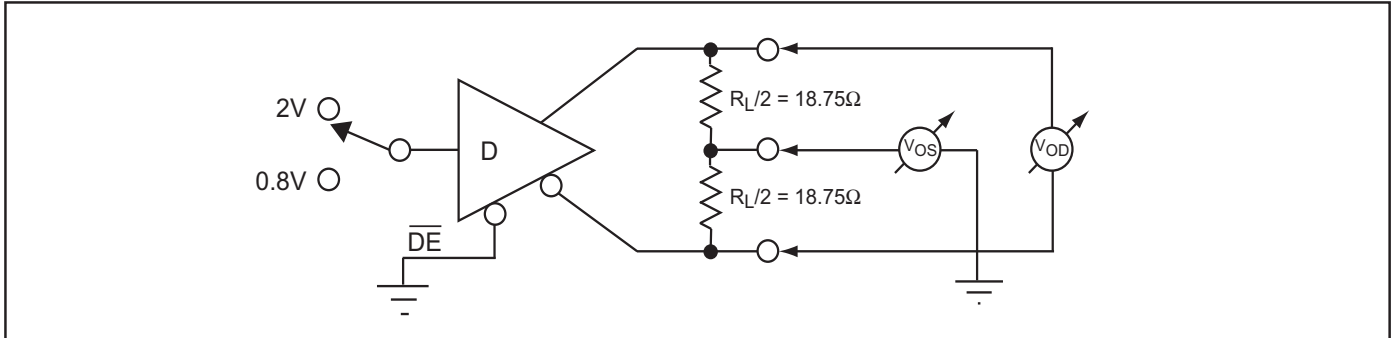


**Figure 4. Output Enable ( $\overline{OE}$ ) Delay Waveforms**

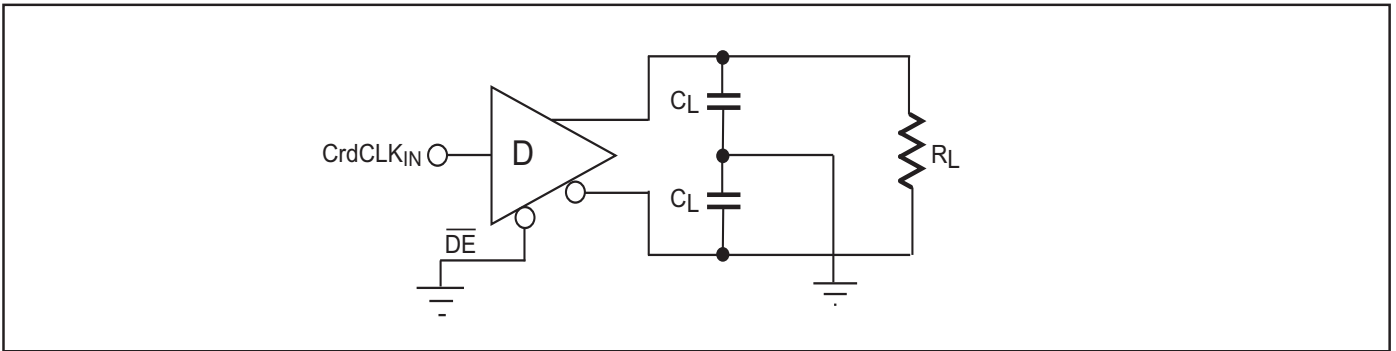


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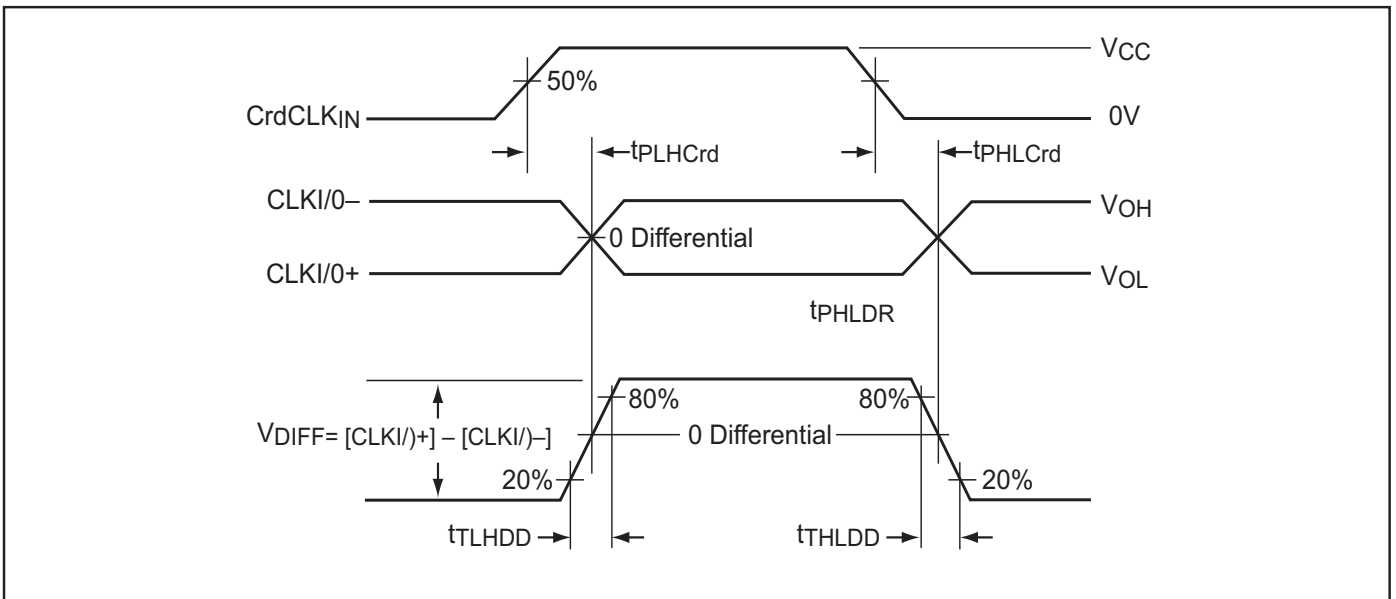
**Parameter Measurement Information**



**Figure 5. Differential Driver DC Test**



**Figure 6. Driver Propagation Delay Test Circuit**

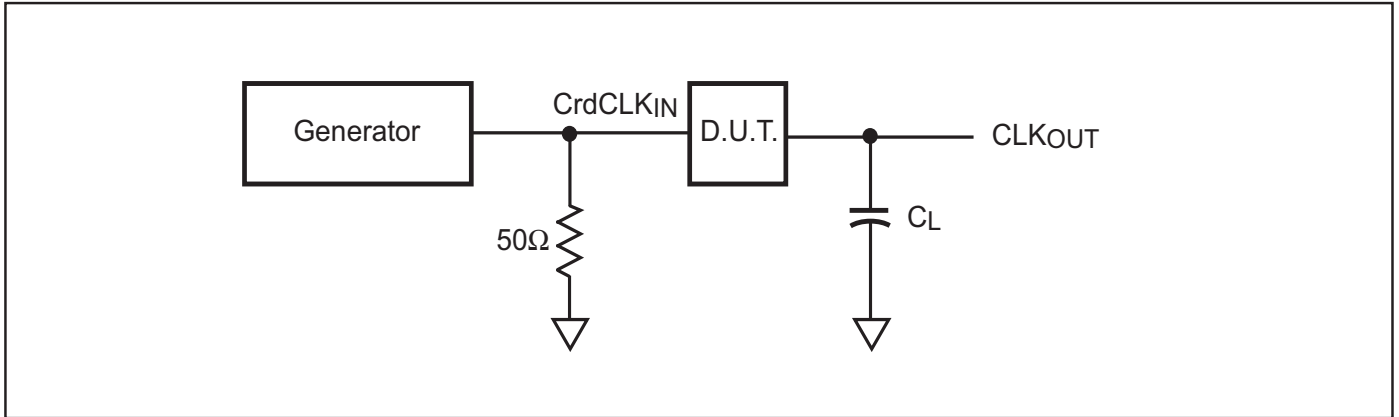


**Figure 7. Driver Propagation Delay and Transition Time Waveforms**

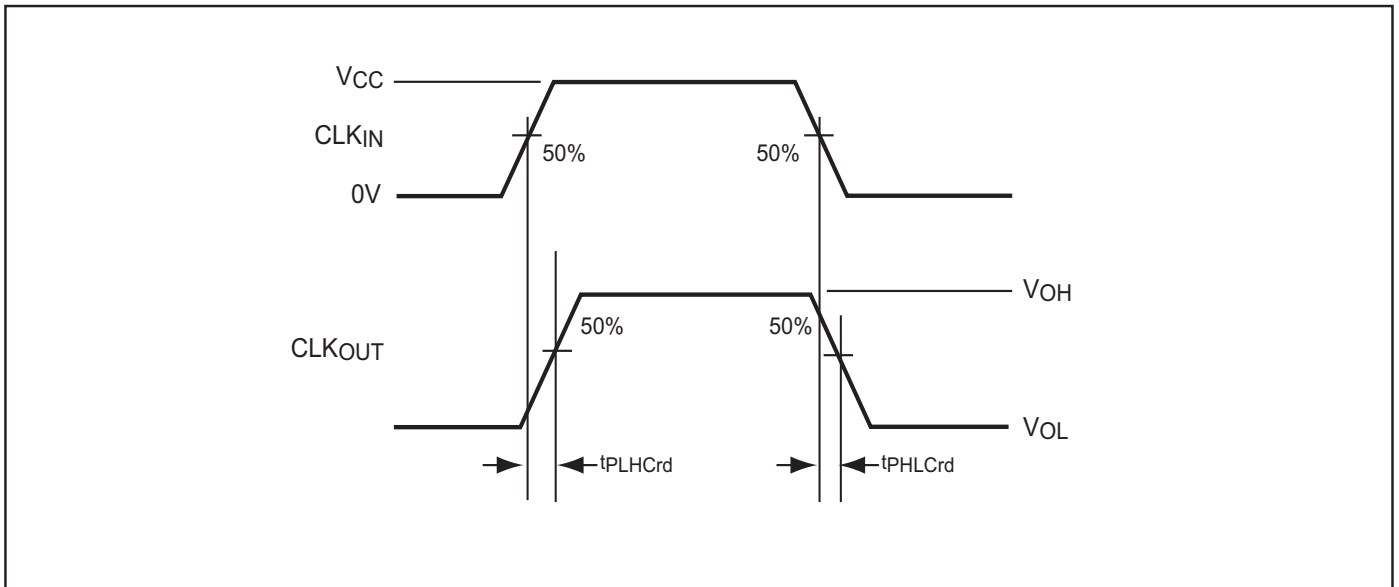


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**Parameter Measurement Information**



**Figure 8. CrdCLK<sub>IN</sub> Propagation Delay Time Test Circuit**

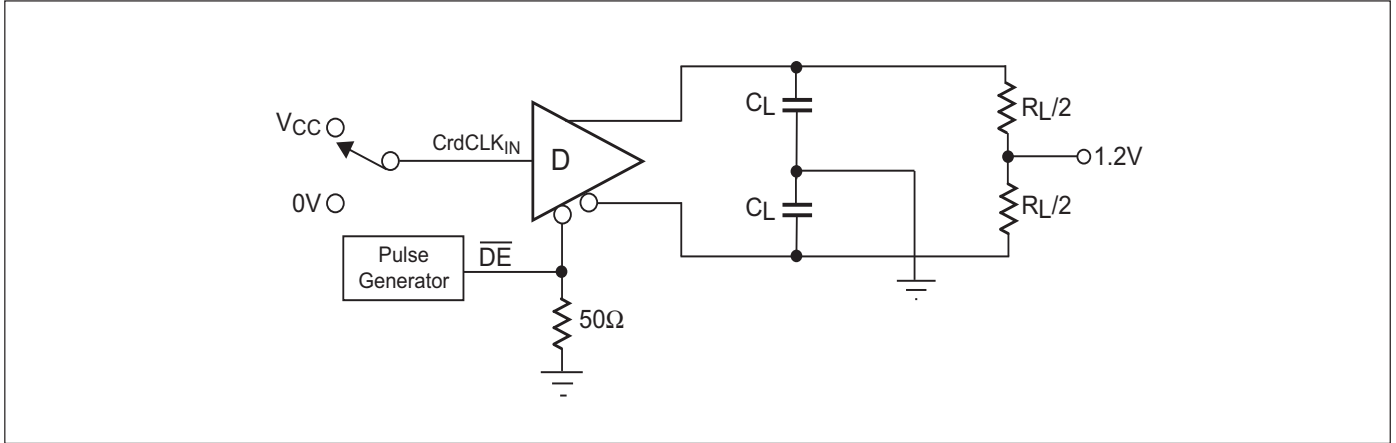


**Figure 9. CrdCLK<sub>IN</sub> Propagation Delay Time Waveforms**

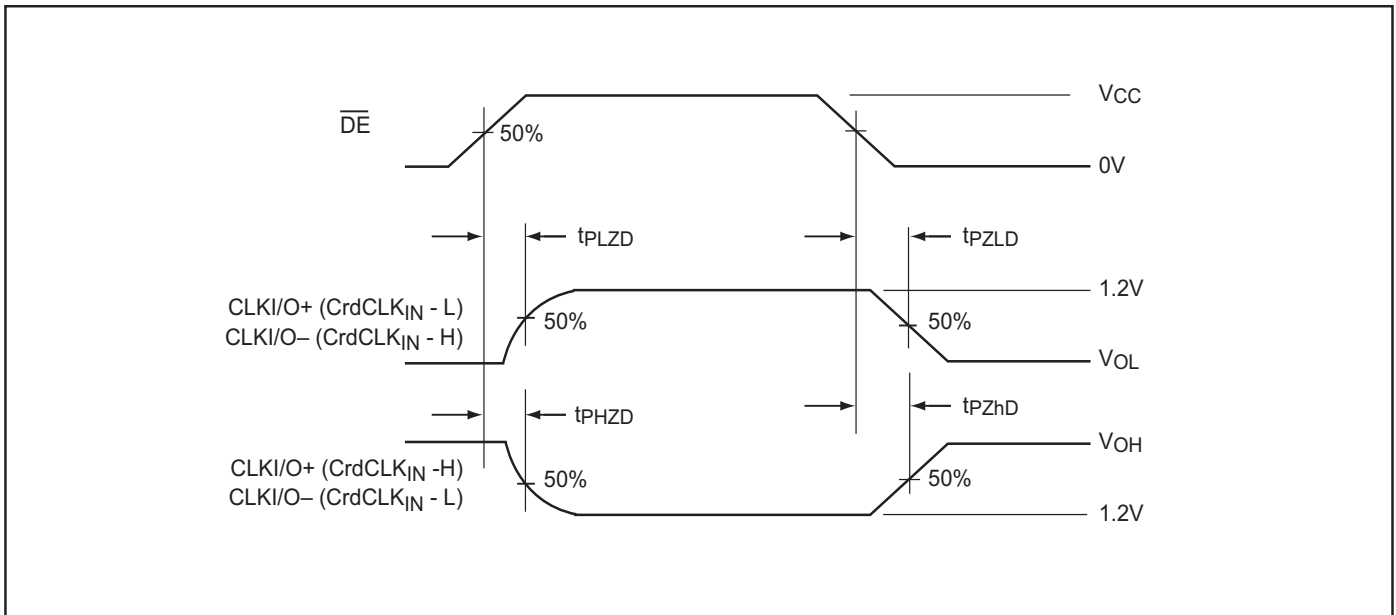


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**Parameter Measurement Information**



**Figure 10. Driver 3-State Test Circuit**

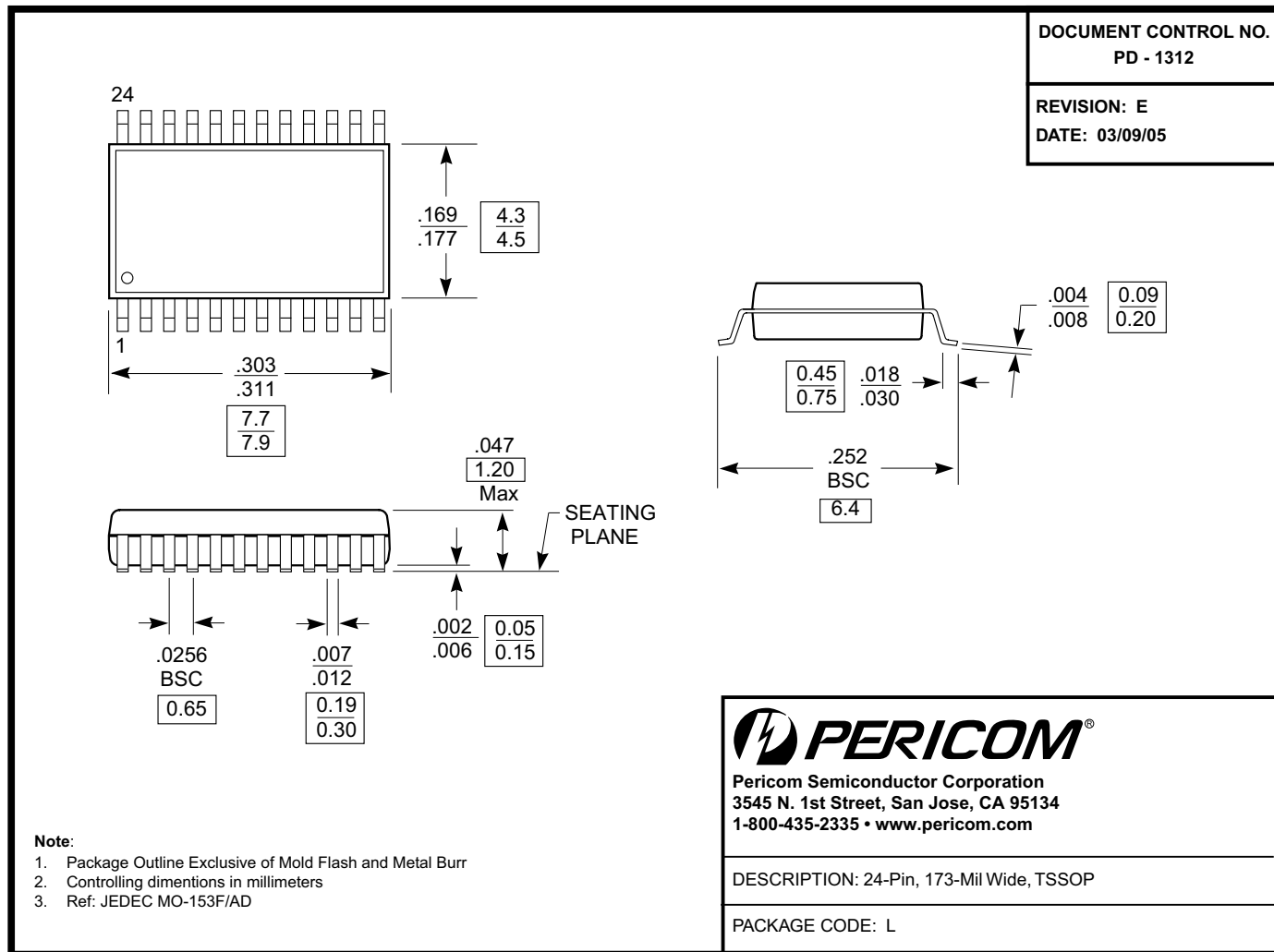


**Figure 11. Driver 3-State Waveforms**



**PI90LVB16**  
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**24-Pin TSSOP (L) Package**



**Ordering Information**

Ordering Code	Package Code	Package Type	Operating Range
PI90LVB16LE	L	Pb-free & Green, 24-pin TSSOP	-40°C to 85°C