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DS1609S-50

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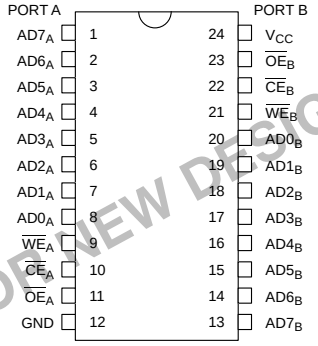
DALLAS SEMICONDUCTOR

DS1609
Dual Port RAM

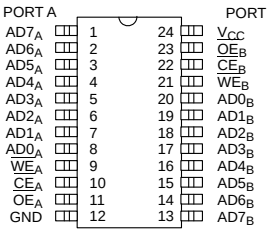
FEATURES

- Totally asynchronous 256–byte dual port memory
- Multiplexed address and data bus keeps pin count low
- Dual port memory cell allows random access with minimum arbitration
- Each port has standard independent RAM control signals
- Fast access time
- Low power CMOS design
- 24–pin DIP or 24–pin SOIC surface mount package
- Both CMOS and TTL compatible
- Operating temperature of –40°C to +85°C
- Standby current of 100 nA @ 25°C makes the device ideal for battery backup or battery operate applications.

PIN ASSIGNMENT



DS1609
24–PIN DIP (600 MIL)
See Mech. Drawings Section



DS1609S
24–PIN SOIC (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

AD0–AD7	–	Port address/data
$\overline{CE}$	–	Port enable
$\overline{WE}$	–	Write enable
$\overline{OE}$	–	Output enable
V_{CC}	–	+5 volt supply
GND	–	Ground

DESCRIPTION

The DS1609 is a random access 256–byte dual port memory designed to connect two asyncronous address/data buses together with a common memory element. Both ports have unrestricted access to all 256 bytes of memory, and with modest system discipline no arbitration is required. Each port is controlled by three control signals: output enable, write enable, and port enable. The device is packaged in plastic 24–pin DIP and 24–pin SOIC. Output enable access time of 50 ns is available when operating at 5 volts.

OPERATION – READ CYCLE

The main elements of the dual port RAM are shown in Figure 1.

A read cycle to either port begins by placing an address on the multiplexed bus pins AD0 – AD7. The port enable control ($\overline{CE}$) is then transitioned low. This control signal causes address to be latched internally. Addresses can be removed from the bus provided address hold time is met. Next, the output enable control ($\overline{OE}$) is transitioned low, which begins the data access portion of the read cycle. With both $\overline{CE}$ and $\overline{OE}$ active low, data will appear valid after the output enable access time t_{OEA}. Data will remain valid as long as both port enable and output enable remains low. A read cycle is terminated with the first occurring rising edge of either $\overline{CE}$ or $\overline{OE}$. The address/data bus will return to a high impedance state after time t_{CEZ} or t_{OEZ} as referenced to the first occurring rising edge. $\overline{WE}$ must remain high during read cycles.

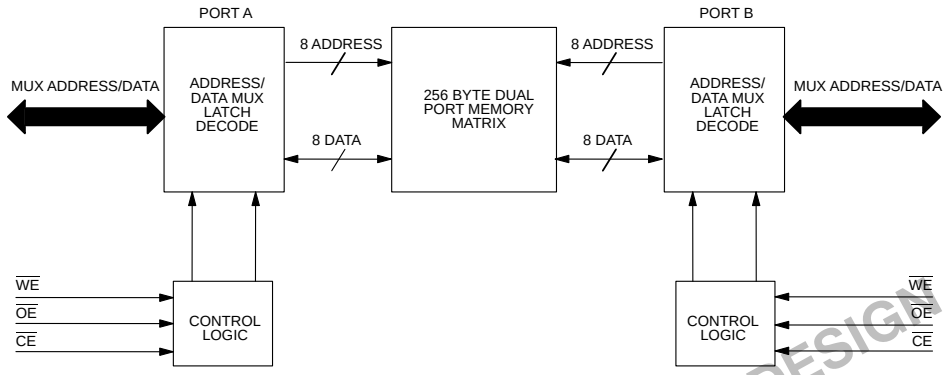
OPERATION – WRITE CYCLE

A write cycle to either port begins by placing an address on the multiplexed bus pins AD0 – AD7. The port enable control ($\overline{CE}$) is then transitioned low. This control signal causes address to be latched internally. As with a read cycle, the address can be removed from the bus provided address hold time is met. Next the write enable control signal ($\overline{WE}$) is transitioned low which begins the write data portion of the write cycle. With both $\overline{CE}$ and $\overline{WE}$ active low the data to be written to the selected memory location is placed on the multiplexed bus. Provided that data setup (t_{DS}) and data hold (t_{DH}) times are met, data is written into the memory and the write cycle is terminated on the first occurring rising edge of either $\overline{CE}$ or $\overline{WE}$. Data can be removed from the bus as soon as the write cycle is terminated. $\overline{OE}$ must remain high during write cycles.

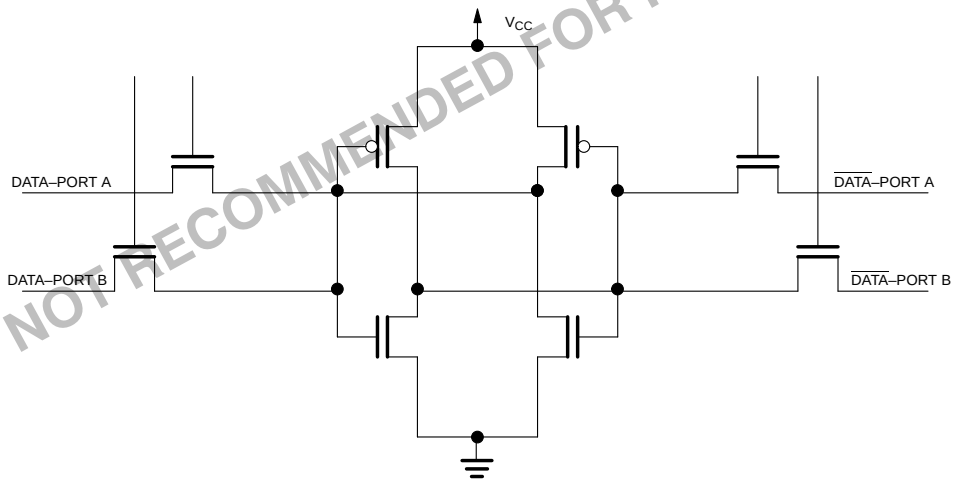
ARBITRATION

The DS1609 dual port RAM has a special cell design that allows for simultaneous accesses from two ports (see Figure 2). Because of this cell design, no arbitration is required for read cycles occurring at the same instant. However, an argument for arbitration can be made for reading and writing the cell at the exact same instant or for writing from both ports at the same instant. A simple way to assure that read/write conflicts don't occur is to perform redundant read cycles. Write/write arbitration needs can be avoided by assigning groups of addresses for write operation to one port only. Groups of data can be assigned check sum bytes which would guarantee correct transmission. A software arbitration system using a "mail box" to pass status information can also be employed. Each port could be assigned a unique byte for writing status information which the other port would read. The status information could tell the reading port if any activity is in progress and indicate when activity is going to occur.

BLOCK DIAGRAM: DUAL PORT RAM Figure 1



DUAL PORT MEMORY CELL Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC} + 0.3	V	1
Input Logic 0	V_{IL}	–0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Impedance	Z_{IN}	50K			Ω	2
$\overline{CE}$, $\overline{WE}$, $\overline{OE}$ Leakage	I_{LO}	–1.0		+1.0	µA	
Standby Current	I_{CCS1}		3.0	5.0	mA	3, 4, 13
Standby Current	I_{CCS2}		50	300	µA	3, 5, 13
Standby Current	I_{CCS3}		100		nA	3, 6, 13
Operating Current	I_{CC}		18	30	mA	7, 13
Logic 1 Output	V_{OH}	2.4			V	8
Logic 0 Output	V_{OL}			0.4	V	9

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
I/O Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS (–40°C to +85°C; V_{CC} = 5V ± 10%)

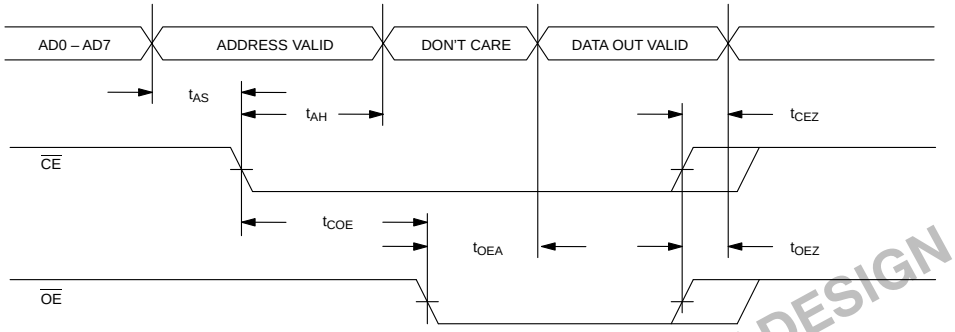
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	5			ns	
Address Hold Time	t_{AH}	25			ns	
Output Enable Access	t_{OEA}	0		50	ns	10
$\overline{OE}$ to High Z	t_{OEZ}	0		20	ns	
$\overline{CE}$ to High Z	t_{CEZ}	0		20	ns	
Data Setup Time	t_{DS}	0			ns	
Data Hold Time	t_{DH}	10			ns	
Write Pulse Width	t_{WP}	50			ns	11
$\overline{CE}$ Recovery Time	t_{CER}	20			ns	12
$\overline{WE}$ Recovery Time	t_{WER}	20			ns	12
$\overline{OE}$ Recovery Time	t_{OER}	20			ns	12
$\overline{CE}$ to $\overline{OE}$ Setup Time	t_{COE}	25			ns	
$\overline{CE}$ to $\overline{WE}$ Setup Time	t_{CWE}	25			ns	

AC ELECTRICAL CHARACTERISTICS (–40°C to +85°C; V_{CC} = 2.5V – 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	5			ns	
Address Hold Time	t_{AH}	25			ns	
Output Enable Access	t_{OEA}	0		100	ns	10
$\overline{OE}$ to High Z	t_{OEZ}	0		20	ns	
$\overline{CE}$ to High Z	t_{CEZ}	0		20	ns	
Data Setup Time	t_{DS}	0			ns	
Data Hold Time	t_{DH}	10			ns	
Write Pulse Width	t_{WP}	100			ns	11
$\overline{CE}$ Recovery Time	t_{CER}	20			ns	12
$\overline{WE}$ Recovery Time	t_{WER}	20			ns	12
$\overline{OE}$ Recovery Time	t_{OER}	20			ns	12
$\overline{CE}$ to $\overline{OE}$ Setup Time	t_{COE}	25			ns	
$\overline{CE}$ to $\overline{WE}$ Setup Time	t_{CWE}	25			ns	

DUAL PORT RAM TIMING: READ CYCLE

DURING READ CYCLE $\overline{WE}$ = V_{IH}

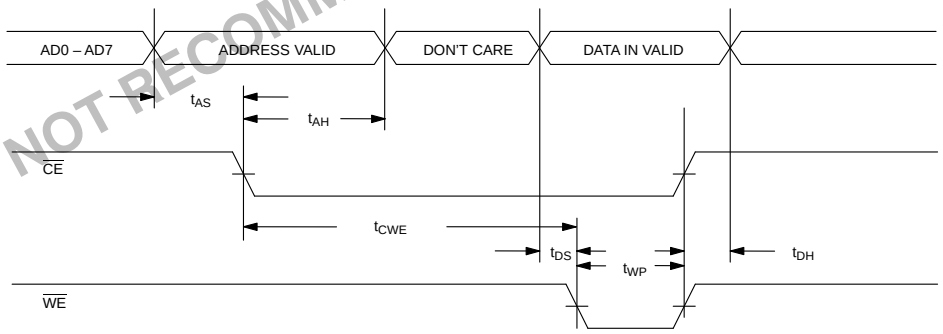


NOTES:

1. During read cycle the address must be off the bus prior to t_{OEA} minimum to avoid bus contention.
2. Read cycles are terminated by the first occurring rising edge of $\overline{OE}$ or $\overline{CE}$.

DUAL PORT RAM TIMING: WRITE CYCLE

DURING WRITE CYCLE $\overline{OE}$ = V_{IH}



NOTE:

1. Write cycles are terminated by the first occurring edge of $\overline{WE}$ or $\overline{CE}$.

NOTES:

1. All Voltages are referenced to ground.
2. All pins other than $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, V_{CC} and ground are continuously driven by a feedback latch in order to hold the inputs at one power supply rail or the other when an input is tristated. The minimum driving impedance presented to any pin is 50KΩ. If a pin is at a logic low level, this impedance will be pulling the pin to ground. If a pin is at a logic high level, this impedance will be pulling the pin to V_{CC}.
3. Standby current is measured with outputs open circuited.
4. I_{CCS1} is measured with all pins within 0.3V of V_{CC} or GND and with $\overline{CE}$ at a logic high or logic low level.
5. I_{CCS2} is measured with all pins within 0.3V of V_{CC} or ground and with $\overline{CE}$ within 0.3V of V_{CC}.
6. I_{CCS3} is measured with all pins at V_{CC} or ground potential and with $\overline{CE}$ = V_{CC}. Note that if a pin is floating, the internal feedback latches will pull all the pins to one power supply rail or the other.
7. Active current is measured with outputs open circuited, and inputs swinging full supply levels with one port reading and one port writing at 100 ns cycle time. Active currents are a DC average with respect to the number of 0's and 1's being read or written.
8. Logic one voltages are specified at a source current of 1 mA.
9. Logic zero voltages are specified at a sink current of 4 mA.
10. Measured with a load as shown in Figure 3.
11. t_{WP} is defined as the time from $\overline{WE}$ going low to the first of the rising edges of $\overline{WE}$ and $\overline{CE}$.
12. Recovery time is the amount of time control signals must remain high between successive cycles.
13. Typical values are at 25°C.

LOAD SCHEMATIC Figure 3