

## Excellent Integrated System Limited

Stocking Distributor

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[IXYS Corporation](#)  
[MMIX1F420N10T](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)



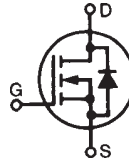
Advance Technical Information

**GigaMOS™ Trench™  
 HiperFET™  
 Power MOSFET**

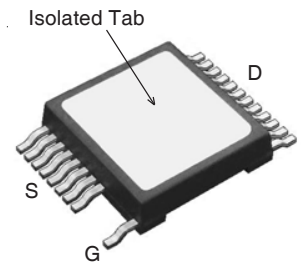
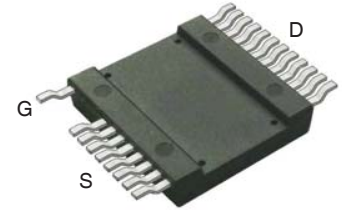
**MMIX1F420N10T**

**V<sub>DSS</sub> = 100V**  
**I<sub>D25</sub> = 334A**  
**R<sub>DS(on)</sub> ≤ 2.6mΩ**  
**T<sub>rr</sub> ≤ 140ns**

**(Electrically Isolated Tab)**



N-Channel Enhancement Mode  
 Avalanche Rated  
 Fast Intrinsic Diode



G = Gate    D = Drain  
 S = Source

Symbol	Test Conditions	Maximum Ratings	
V <sub>DSS</sub>	T <sub>J</sub> = 25°C to 175°C	100	V
V <sub>DGR</sub>	T <sub>J</sub> = 25°C to 175°C, R <sub>GS</sub> = 1MΩ	100	V
V <sub>GSS</sub>	Continuous	±20	V
V <sub>GSM</sub>	Transient	±30	V
I <sub>D25</sub>	T <sub>C</sub> = 25°C	334	A
I <sub>DM</sub>	T <sub>C</sub> = 25°C, Pulse Width Limited by T <sub>JM</sub>	1000	A
I <sub>A</sub>	T <sub>C</sub> = 25°C	200	A
E <sub>AS</sub>	T <sub>C</sub> = 25°C	5	J
P <sub>D</sub>	T <sub>C</sub> = 25°C	680	W
dv/dt	I <sub>S</sub> ≤ I <sub>DM</sub> , V <sub>DD</sub> ≤ V <sub>DSS</sub> , T <sub>J</sub> ≤ 175°C	20	V/ns
T <sub>J</sub>		-55 ... +175	°C
T <sub>JM</sub>		175	°C
T <sub>stg</sub>		-55 ... +175	°C
T <sub>L</sub>	1.6mm (0.062 in.) from Case for 10s	300	°C
T <sub>SOLD</sub>	Plastic Body for 10s	260	°C
V <sub>ISOL</sub>	50/60 Hz, 1 Minute	2500	V~
F <sub>C</sub>	Mounting Force	50..200 / 11..45	N/lb.
<b>Weight</b>		8	g

**Features**

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Substrate
  - Excellent Thermal Transfer
  - Increased Temperature and Power Cycling Capability
  - High Isolation Voltage (2500V~)
- 175°C Operating Temperature
- Very High Current Handling Capability
- Fast Intrinsic Diode
- Avalanche Rated
- Very Low R<sub>DS(on)</sub>

**Advantages**

- Easy to Mount
- Space Savings
- High Power Density

**Applications**

- DC-DC Converters and Off-Line UPS
- Primary-Side Switch
- High Speed Power Switching Applications

Symbol	Test Conditions (T <sub>J</sub> = 25°C, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 3mA	100		V
V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 8mA	2.5		V
I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±200 nA
I <sub>DSS</sub>	V <sub>DS</sub> = V <sub>DSS</sub> , V <sub>GS</sub> = 0V T <sub>J</sub> = 150°C			50 μA 5 mA
R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 60A, Note 1			2.6 mΩ



# MMIX1F420N10T

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 10\text{V}$ , $I_D = 60\text{A}$ , Note 1	110	185	S
$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$		47	nF
$C_{oss}$			4390	pF
$C_{rss}$			530	pF
$R_{GI}$	Gate Input Resistance		1.46	$\Omega$
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 100\text{A}$ $R_G = 1\Omega$ (External)		47	ns
$t_r$			155	ns
$t_{d(off)}$			115	ns
$t_f$			255	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 210\text{A}$		670	nC
$Q_{gs}$			170	nC
$Q_{gd}$			195	nC
$R_{thJC}$				0.22 $^\circ\text{C/W}$
$R_{thCS}$		0.05		$^\circ\text{C/W}$

## Source-Drain Diode

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$I_S$	$V_{GS} = 0\text{V}$			420 A
$I_{SM}$	Repetitive, Pulse Width Limited by $T_{JM}$			1680 A
$V_{SD}$	$I_F = 60\text{A}$ , $V_{GS} = 0\text{V}$ , Note 1			1.2 V
$t_{rr}$	$I_F = 150\text{A}$ , $V_{GS} = 0\text{V}$ $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 60\text{V}$			140 ns
$I_{RM}$			7	A
$Q_{RM}$			380	nC

Note 1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .

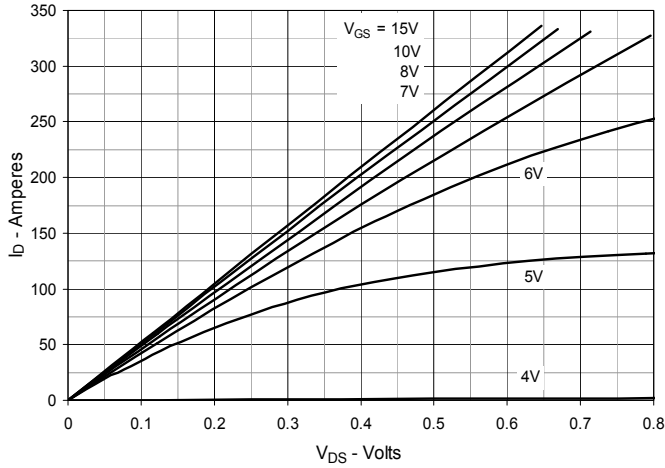
### ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

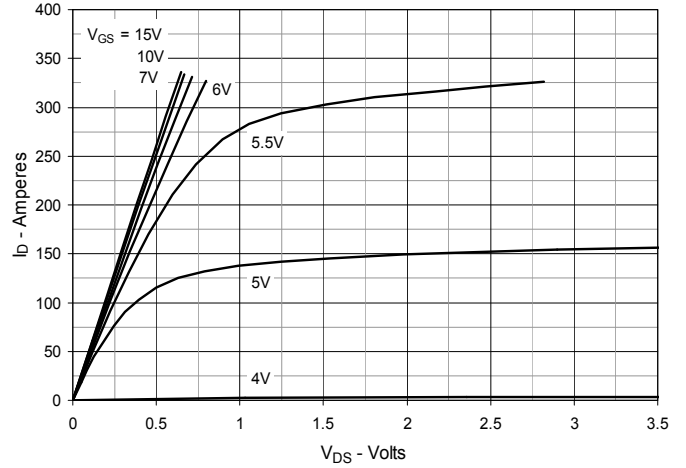
IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2  
 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2  
 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

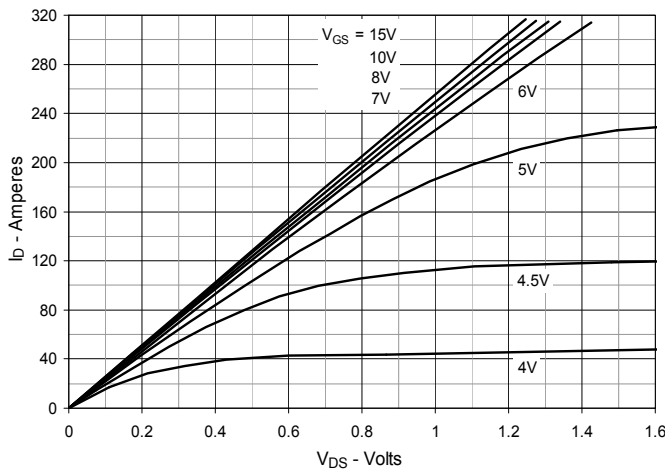
**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$**



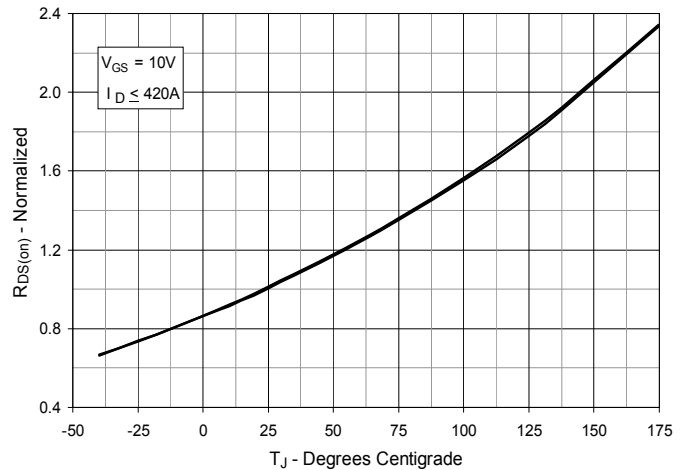
**Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$**



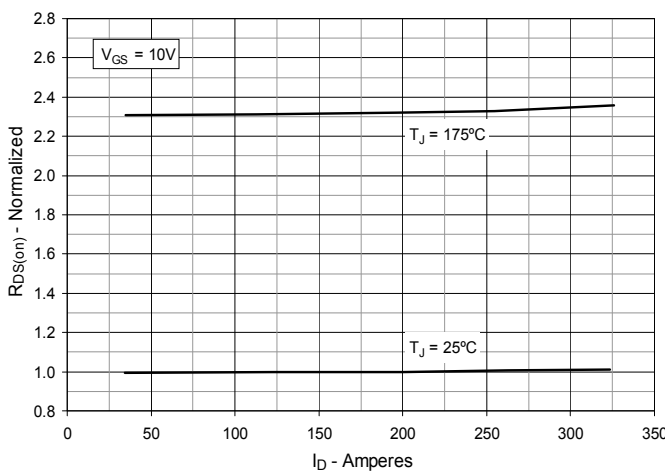
**Fig. 3. Output Characteristics @  $T_J = 150^\circ\text{C}$**



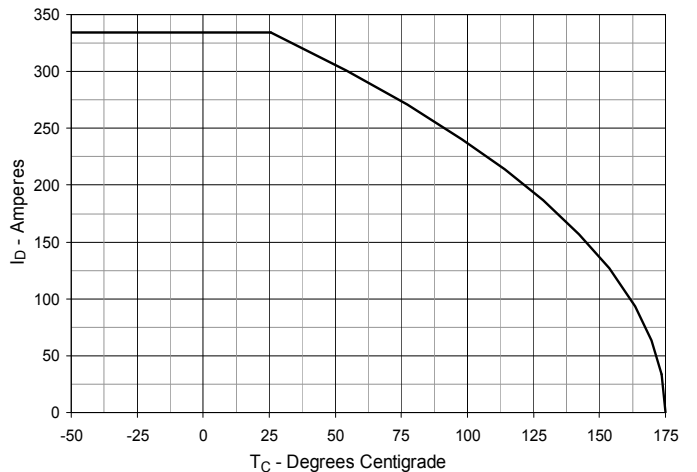
**Fig. 4. Normalized  $R_{DS(on)}$  vs. Junction Temperature**



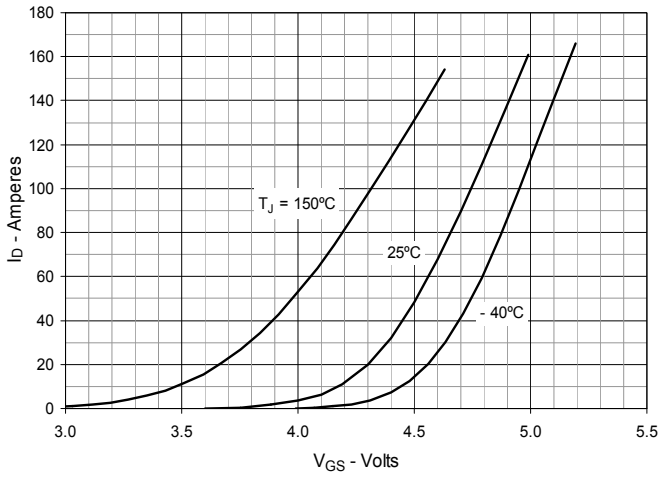
**Fig. 5. Normalized  $R_{DS(on)}$  vs. Drain Current**



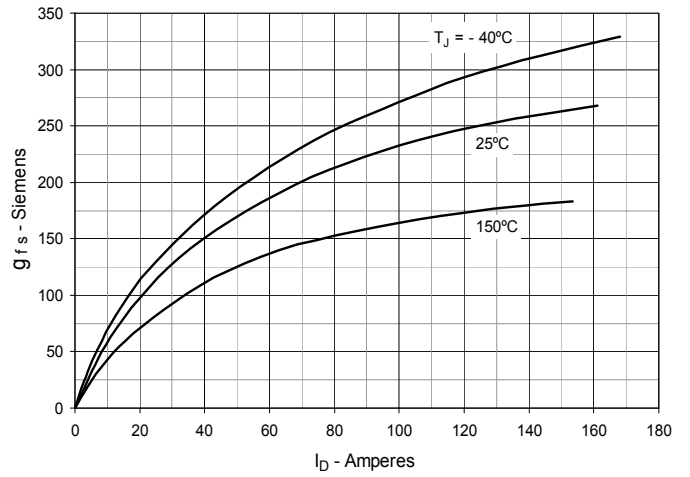
**Fig. 6. Drain Current vs. Case Temperature**



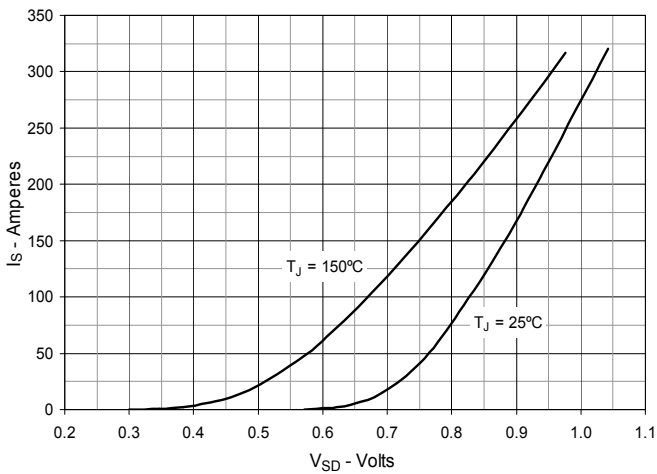
**Fig. 7. Input Admittance**



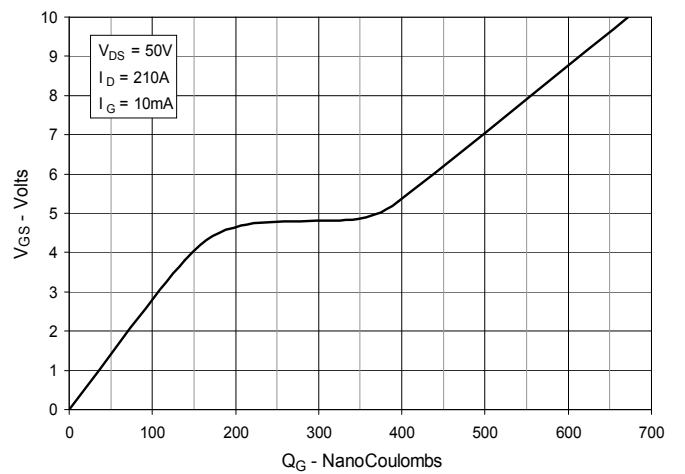
**Fig. 8. Transconductance**



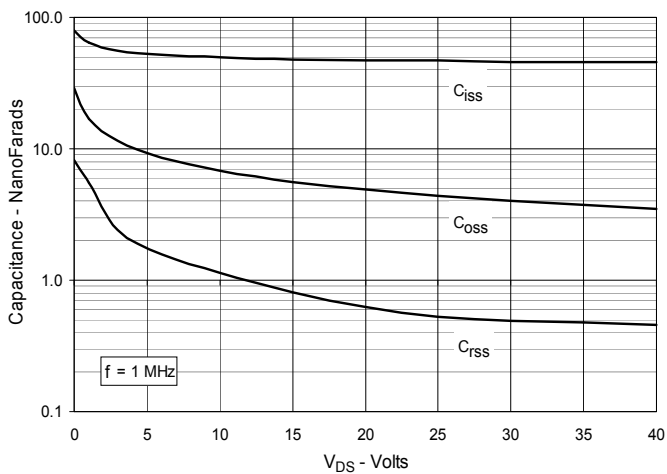
**Fig. 9. Forward Voltage Drop of Intrinsic Diode**



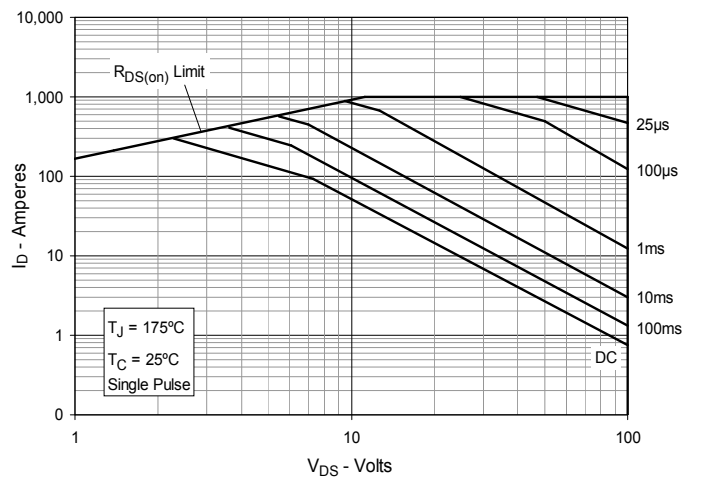
**Fig. 10. Gate Charge**



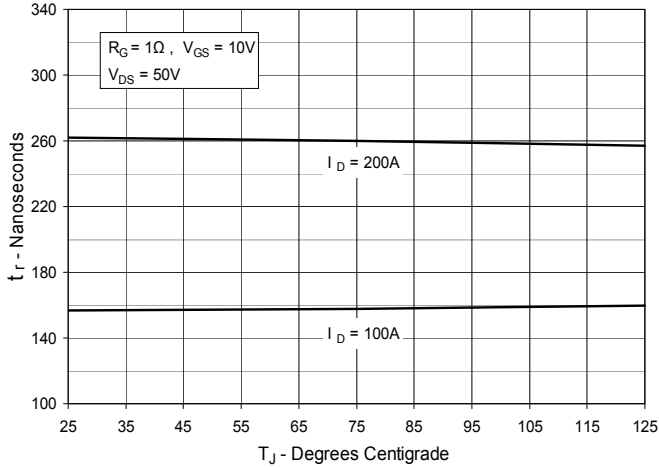
**Fig. 11. Capacitance**



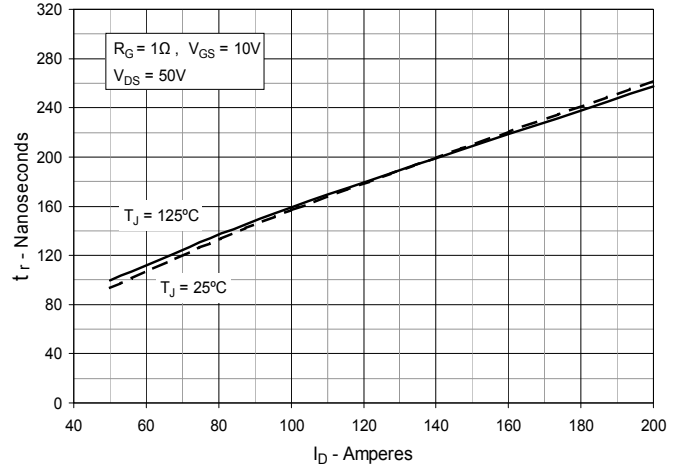
**Fig. 12. Forward-Bias Safe Operating Area**



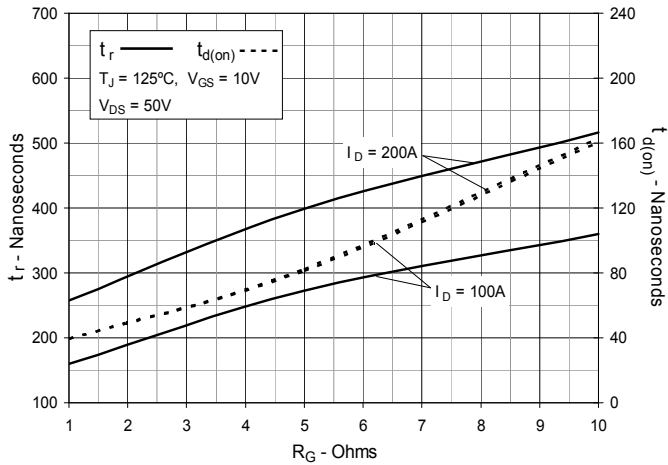
**Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature**



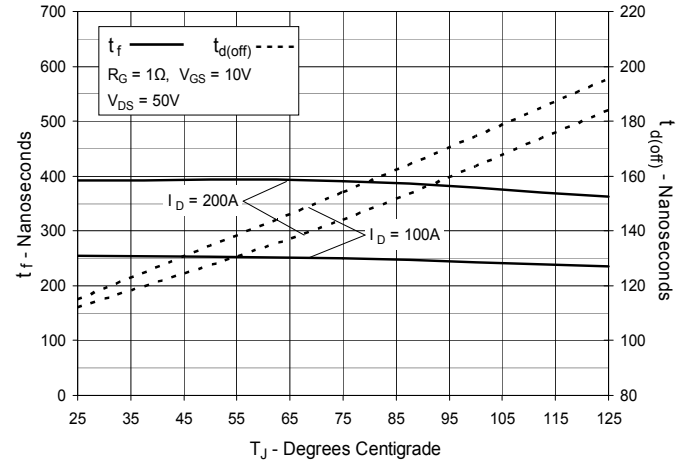
**Fig. 14. Resistive Turn-on Rise Time vs. Drain Current**



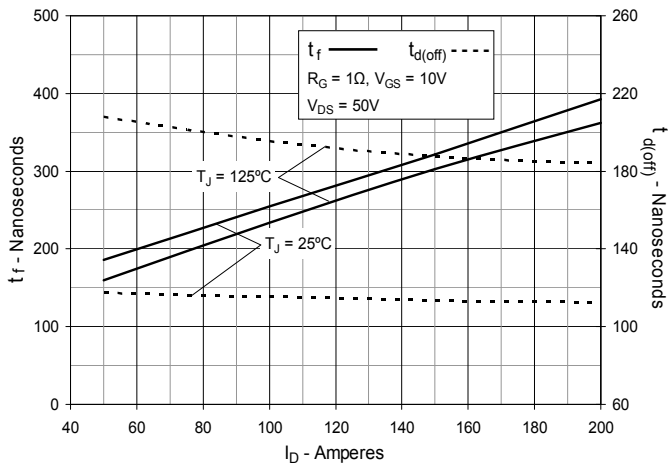
**Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance**



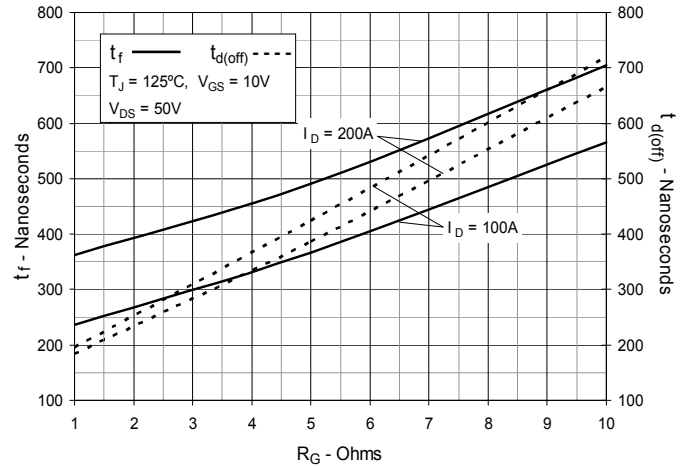
**Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature**



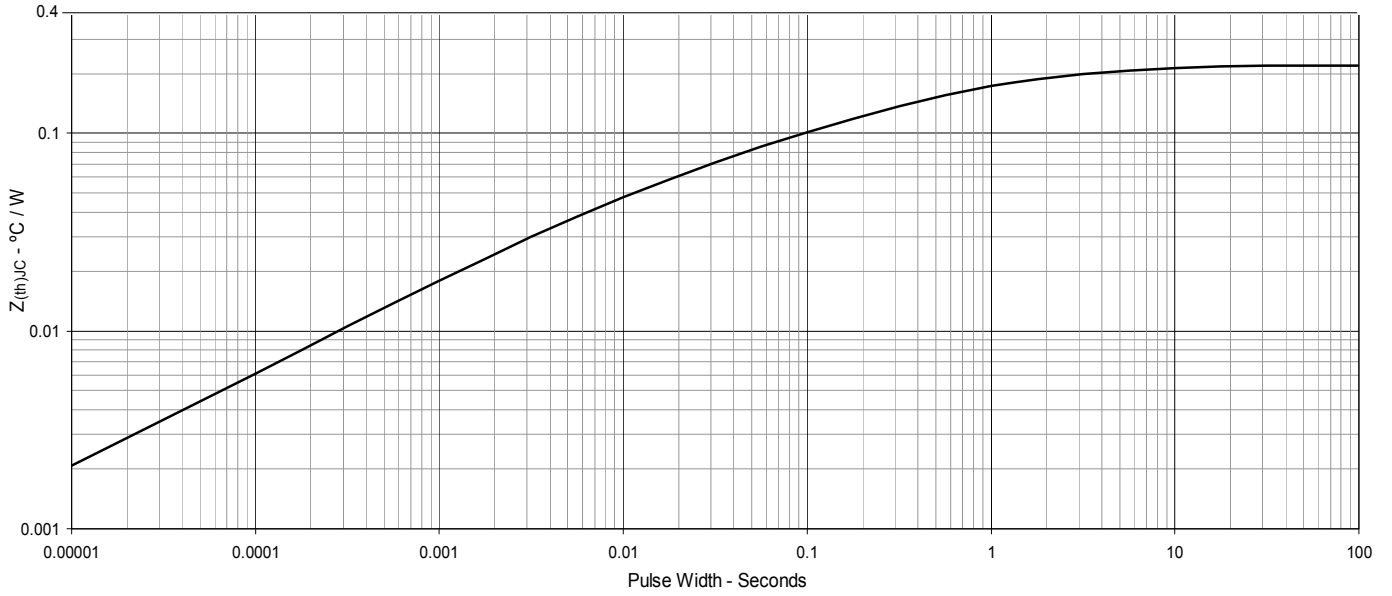
**Fig. 17. Resistive Turn-off Switching Times vs. Drain Current**



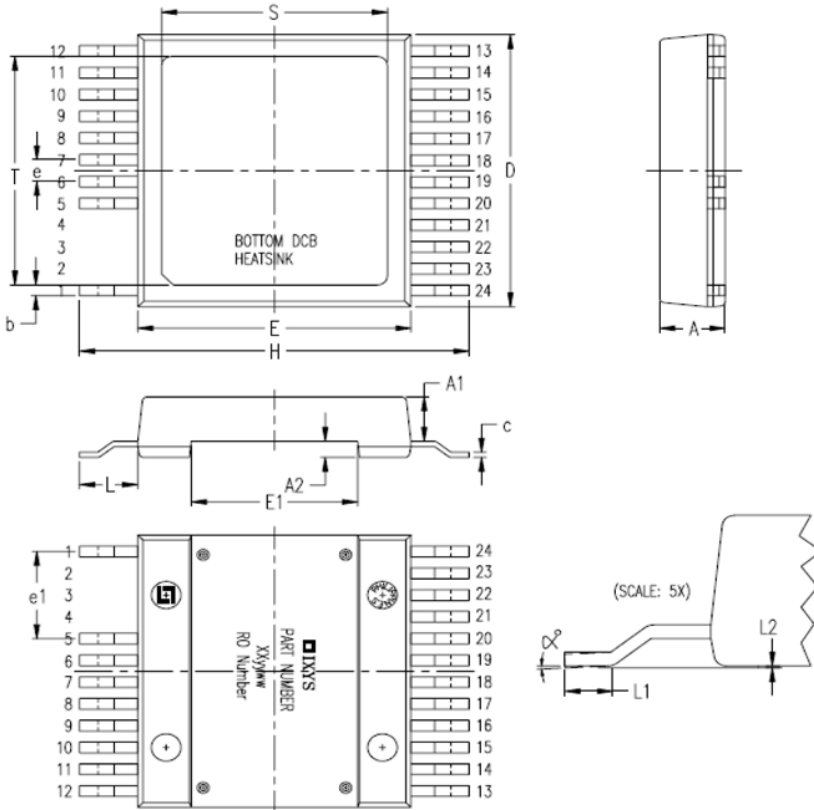
**Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance**



**Fig. 19. Maximum Transient Thermal Impedance**



**Package Outline**



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079 BSC		2.00 BSC	
e1	.315 BSC		8.00 BSC	
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
α	0	4°	0	4°

**PIN: 1 = Gate**  
**5-12 = Source**  
**13-24 = Drain**