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[IRFPS40N50L](#)

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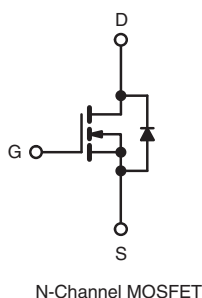
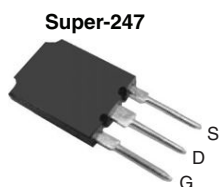


# IRFPS40N50L, SiHFPS40N50L

Vishay Siliconix

## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.087
$Q_g$ (Max.) (nC)	380	
$Q_{gs}$ (nC)	80	
$Q_{gd}$ (nC)	190	
Configuration	Single	



### FEATURES

- Superfast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhanced  $dV/dt$  Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Compliant to RoHS Directive 2002/95/EC


**RoHS\***  
COMPLIANT

### APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION	
Package	Super-247
Lead (Pb)-free	IRFPS40N50LPbF
	SiHFPS40N50L-E3
SnPb	IRFPS40N50L
	SiHFPS40N50L

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	500	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	46	A
		$T_C = 100\text{ }^\circ\text{C}$	29	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	180		
Linear Derating Factor		4.3	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	920	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	46	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	54	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	540	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$	34	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>		

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 0.86\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 46\text{ A}$  (see fig. 12).
- $I_{SD} \leq 46\text{ A}$ ,  $dI/dt \leq 550\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

# IRFPS40N50L, SiHFPS40N50L


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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain) <sup>a</sup>	$R_{thJC}$	-	0.23	

**Note**

a.  $R_{th}$  is measured at  $T_J$  approximately 90 °C.

SPECIFICATIONS ( $T_J = 25\text{ °C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1\text{ mA}$	-	0.60	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	$\mu\text{A}$	
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$	-	-	2.0	mA	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 28\text{ A}^b$	-	0.087	0.100	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 46\text{ A}$	21	-	-	S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	8110	-	pF	
Output Capacitance	$C_{oss}$		-	960	-		
Reverse Transfer Capacitance	$C_{rss}$		-	130	-		
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	11200	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	240	-	
Effective Output Capacitance (Energy Related)	$C_{oss\text{ eff. (ER)}}$		$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	310	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 46\text{ A}, V_{DS} = 400\text{ V}$ , see fig. 7 and 15 <sup>b</sup>	-	-	380	nC
Gate-Source Charge	$Q_{gs}$			-	-	80	
Gate-Drain Charge	$Q_{gd}$			-	-	190	
Internal Gate Resistance	$R_G$	$f = 1\text{ MHz}$ , open drain		-	0.90	-	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 46\text{ A}, R_G = 0.85\text{ }\Omega, V_{GS} = 10\text{ V}$ , see fig. 14a and 14b <sup>b</sup>	-	27	-	ns	
Rise Time	$t_r$		-	170	-		
Turn-Off Delay Time	$t_{d(off)}$		-	50	-		
Fall Time	$t_f$		-	69	-		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	46	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	180		
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ °C}, I_S = 46\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ °C}, I_F = 46\text{ A}$	-	170	250	ns	
		$T_J = 125\text{ °C}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	220	330		
Body Diode Reverse Recovery Charge	$Q_{rr}$	$T_J = 25\text{ °C}, I_S = 46\text{ A}, V_{GS} = 0\text{ V}^b$	-	705	1060	nC	
		$T_J = 125\text{ °C}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	1.3	2.0		
Reverse Recovery Current	$I_{RRM}$	$T_J = 25\text{ °C}$	-	9.0	-	A	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

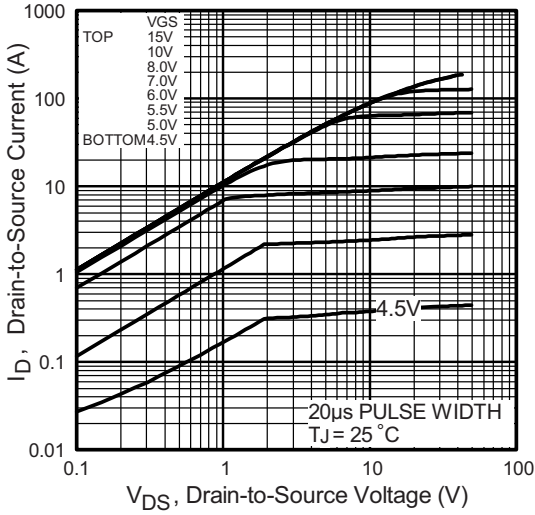
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 400\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .  
 $C_{oss\text{ eff. (ER)}}$  is a fixed capacitance that stores the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .



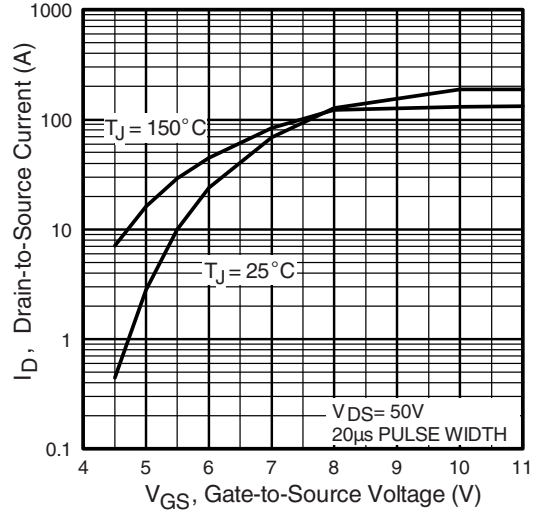
**IRFPS40N50L, SiHFPS40N50L**

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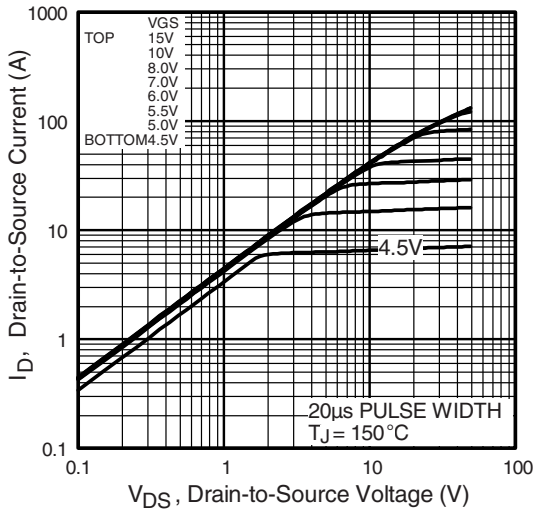
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



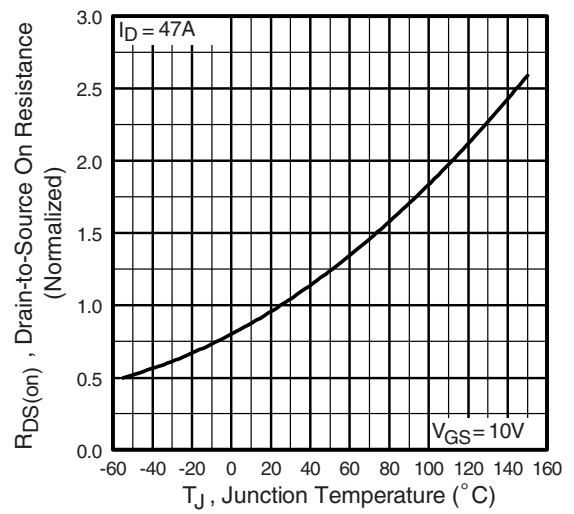
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

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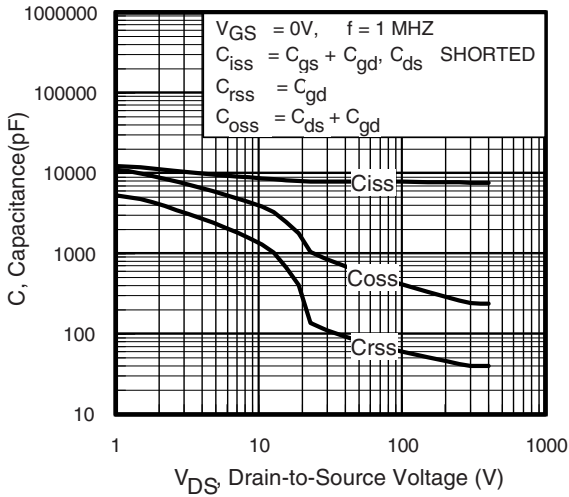


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

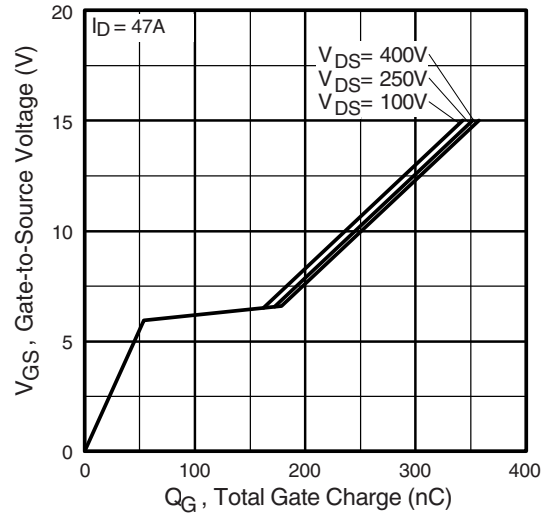


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

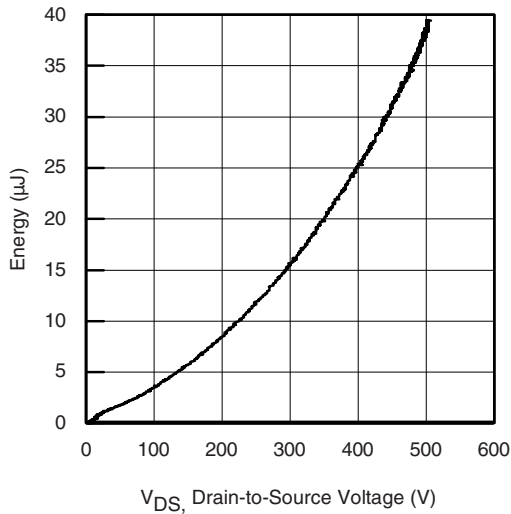


Fig. 6 - Typical Output Capacitance Stored Energy vs.  $V_{DS}$

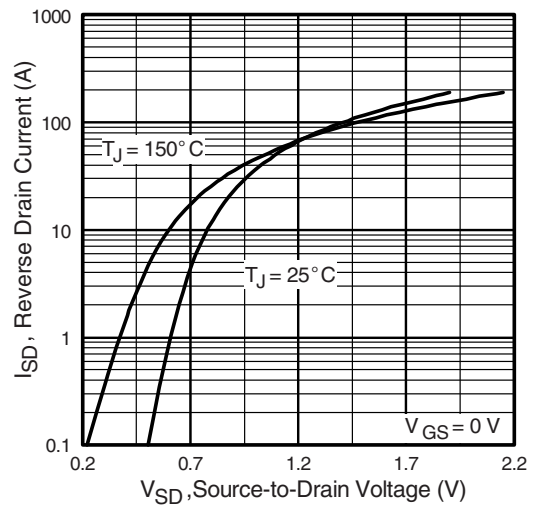
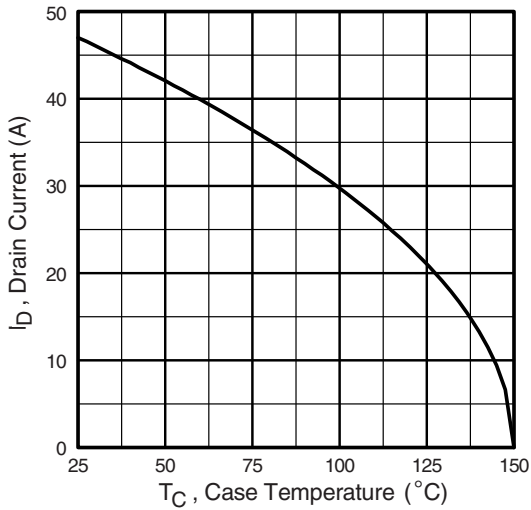


Fig. 8 - Typical Source Drain Diode Forward Voltage

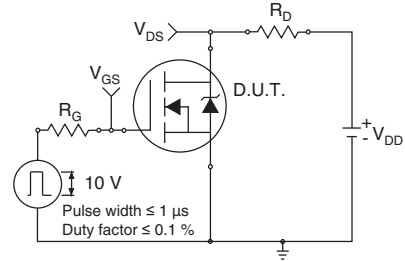


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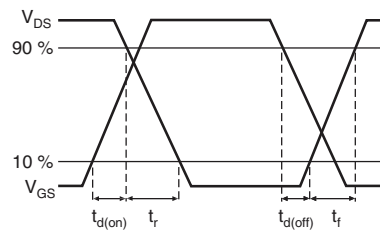
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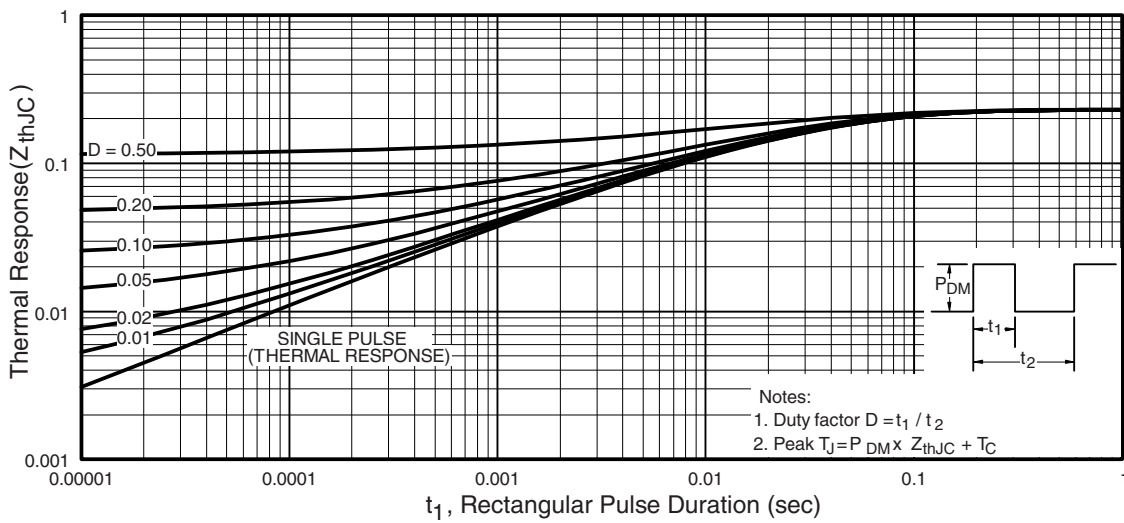
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**



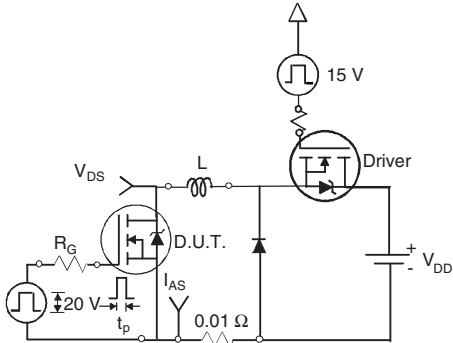
**Fig. 10b - Switching Time Waveforms**



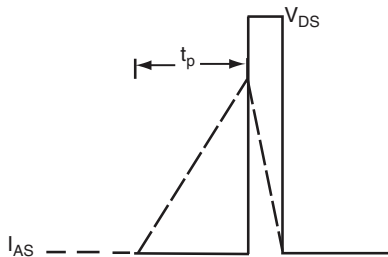
**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

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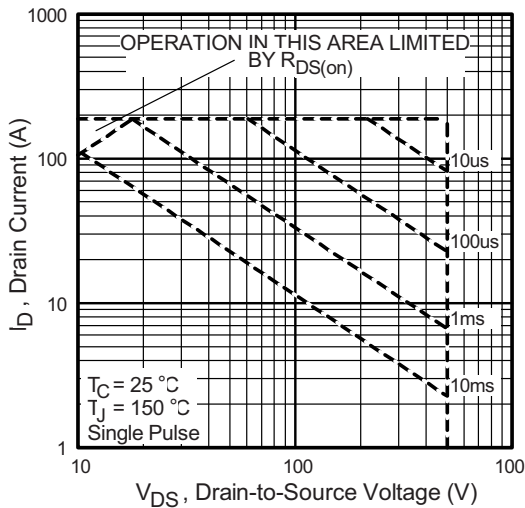
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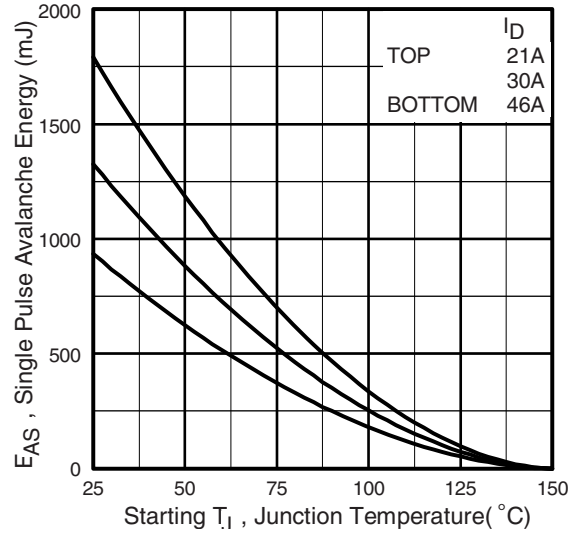
**Fig. 12a - Unclamped Inductive Test Circuit**



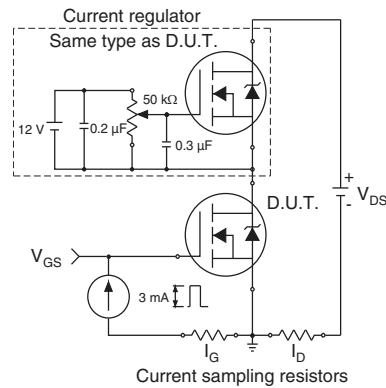
**Fig. 12b - Unclamped Inductive Waveforms**



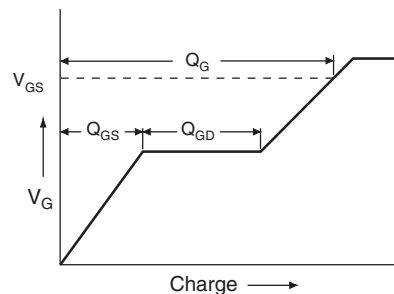
**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**



**Fig. 12d - Maximum Safe Operating Area**



**Fig. 13a - Gate Charge Test Circuit**



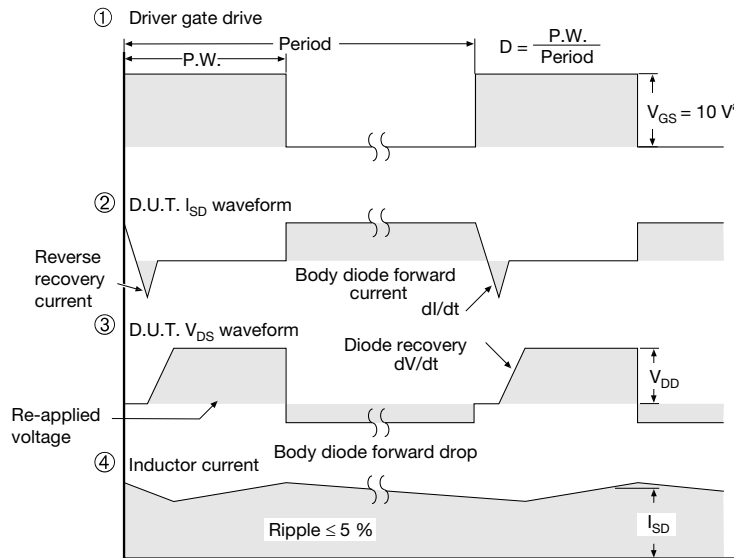
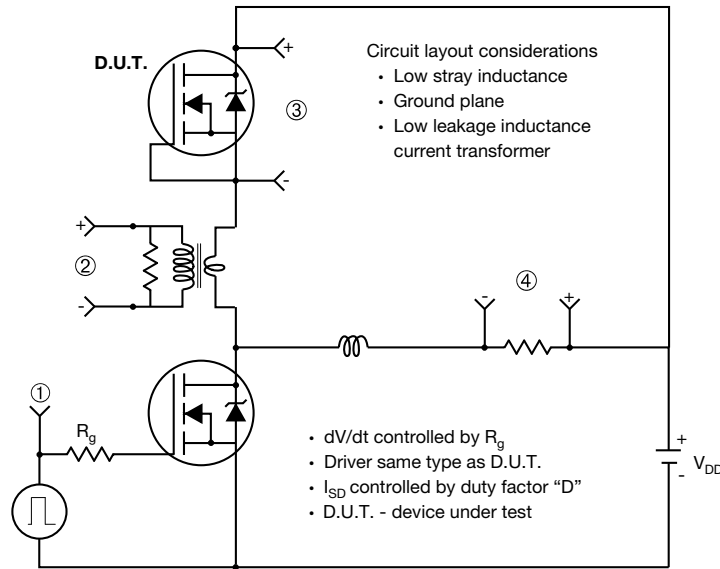
**Fig. 13b - Basic Gate Charge Waveform**



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**Peak Diode Recovery dV/dt Test Circuit**



**Note**  
 a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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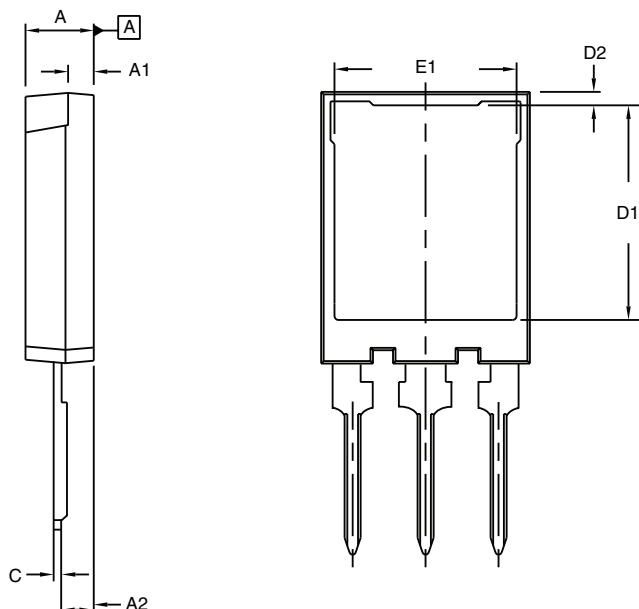
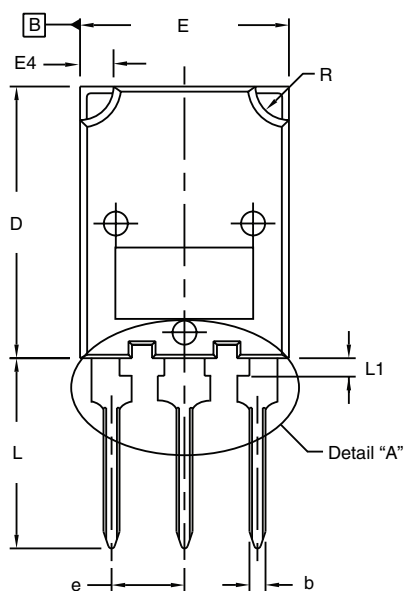




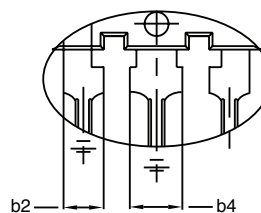
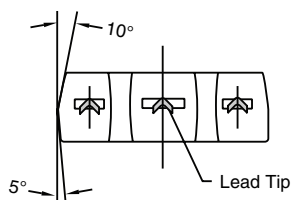
# Package Information

Vishay Siliconix

## TO-274AA (HIGH VOLTAGE)



⊕ 0.10 (0.25) ⊕ BA ⊕



Detail "A"  
Scale: 2:1

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c	0.80	1.20	0.031	0.047
D	19.80	20.80	0.780	0.819

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

ECN: S-82247-Rev. A, 06-Oct-08  
DWG: 5975

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body.
3. Outline conforms to JEDEC outline to TO-274AA.



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