



FDMC0310AS

N-Channel PowerTrench[®] SyncFET[™]

30 V, 21 A, 4.4 mΩ

Features

- Max $r_{DS(on)}$ = 4.4 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 19\text{ A}$
- Max $r_{DS(on)}$ = 5.2 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 17.5\text{ A}$
- Advanced package and silicon combination for low $r_{DS(on)}$ and high efficiency
- SyncFET[™] Schottky Body Diode
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

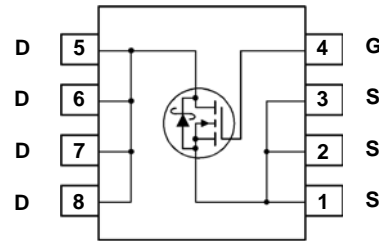
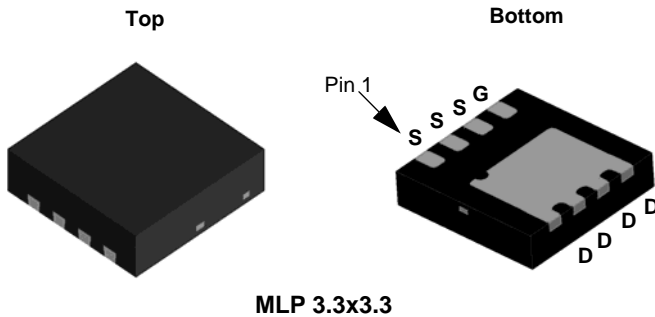


General Description

The FDMC0310AS has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic schottky body diode.

Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU low side switch
- Networking Point of Load low side switch
- Telecom secondary side rectification



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
$V_{DS(t)}$	Drain to Source Transient Voltage ($t_{\text{Transient}} < 100\text{ ns}$)	33	V
V_{GS}	Gate to Source Voltage (Note 4)	± 20	V
I_D	Drain Current -Continuous $T_C = 25^\circ\text{C}$	21	A
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	19	
	-Pulsed	100	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	66	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	36	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC0310AS	FDMC0310AS	MLP 3.3X3.3	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$		26		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$	1.2	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 19\text{ A}$		3.8	4.4	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 17.5\text{ A}$		4.5	5.2	
		$V_{GS} = 10\text{ V}, I_D = 19\text{ A}, T_J = 125\text{ }^\circ\text{C}$		4.5	5.8	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 19\text{ A}$		106		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2380	3165	pF
C_{oss}	Output Capacitance			885	1175	pF
C_{rss}	Reverse Transfer Capacitance			100	150	pF
R_g	Gate Resistance		0.1	0.7	2.5	Ω

Switching Characteristics

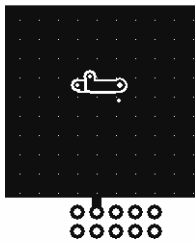
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 19\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		11	20	ns	
t_r	Rise Time			5	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			30	48	ns	
t_f	Fall Time			4	10	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		37	52	nC
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to }4.5\text{ V}$		18	25	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 15\text{ V}, I_D = 19\text{ A}$		6		nC	
Q_{gd}	Gate to Drain "Miller" Charge			6		nC	

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.6	0.8	V
		$V_{GS} = 0\text{ V}, I_S = 19\text{ A}$ (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 19\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		29	47	ns
Q_{rr}	Reverse Recovery Charge			33	53	nC

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $53\text{ }^\circ\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper.



b. $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- E_{AS} of 66 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 21\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 3\text{ mH}$, $I_{AS} = 10.2\text{ A}$.
- As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

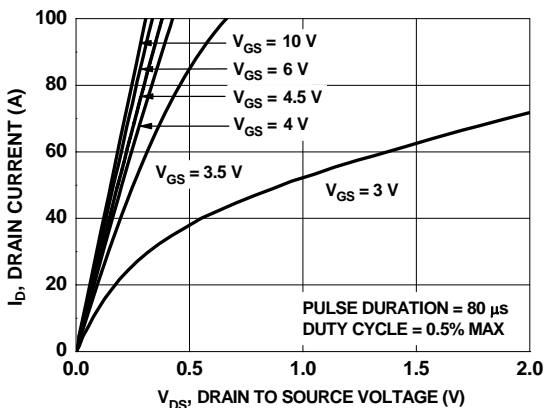


Figure 1. On Region Characteristics

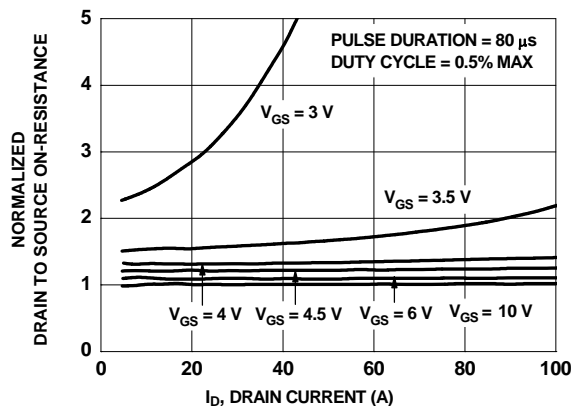


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

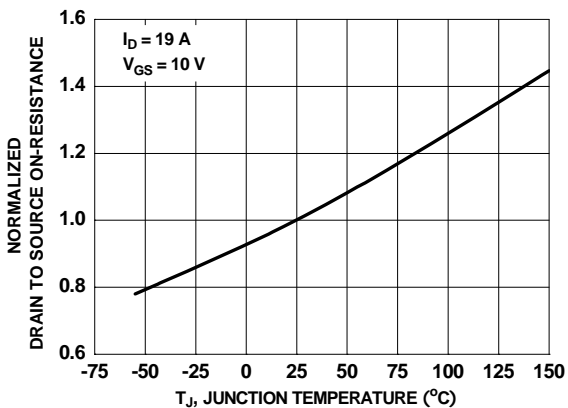


Figure 3. Normalized On Resistance vs. Junction Temperature

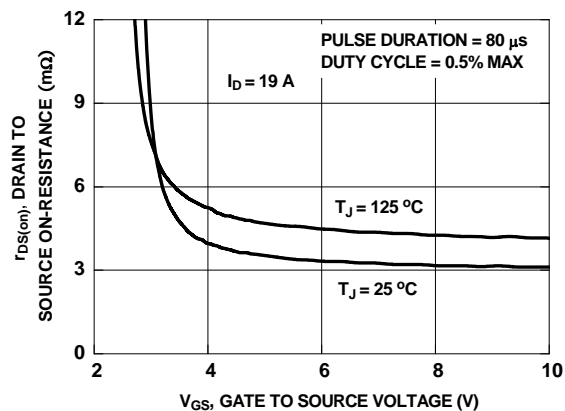


Figure 4. On-Resistance vs. Gate to Source Voltage

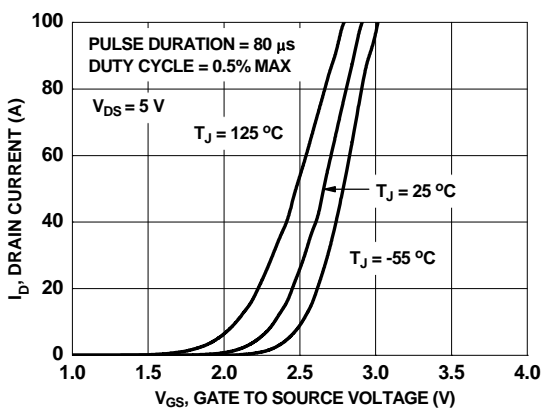


Figure 5. Transfer Characteristics

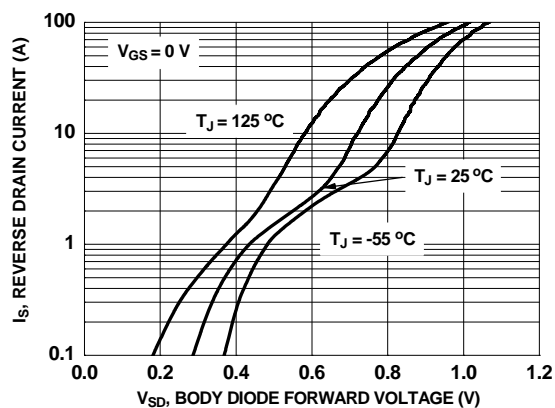


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

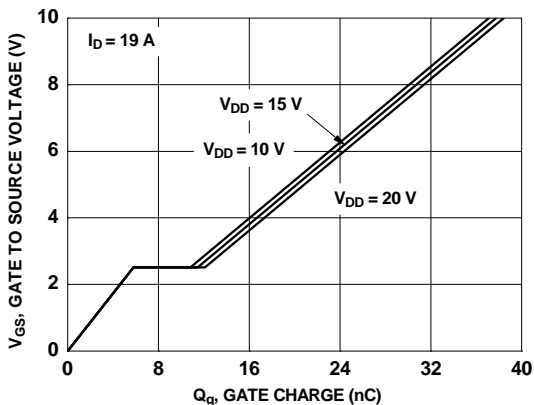


Figure 7. Gate Charge Characteristics

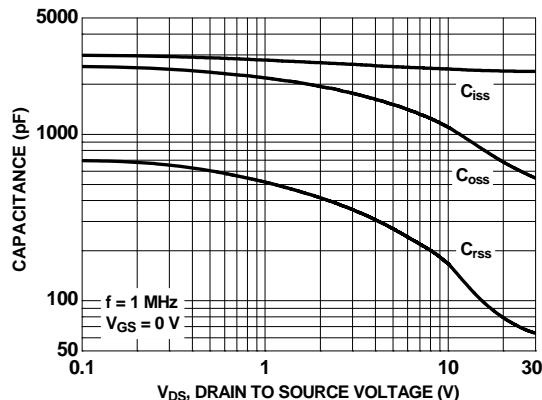


Figure 8. Capacitance vs. Drain to Source Voltage

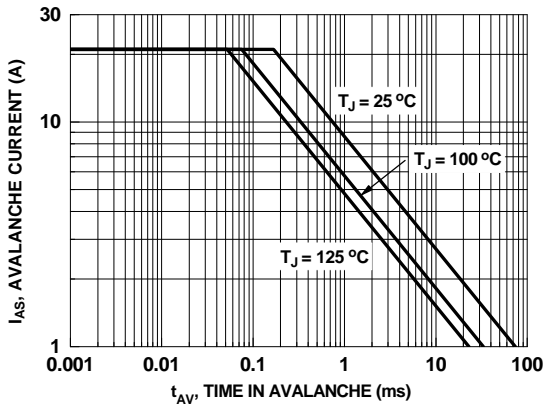


Figure 9. Unclamped Inductive Switching Capability

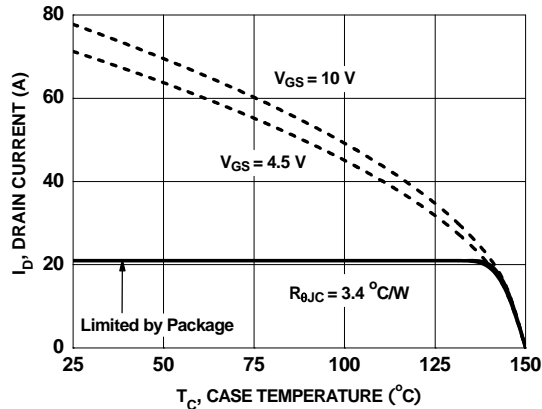


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

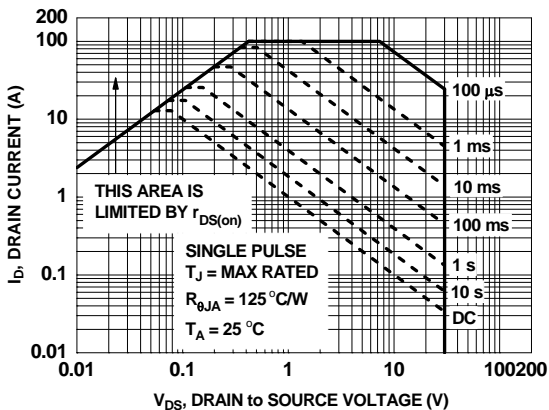


Figure 11. Forward Bias Safe Operating Area

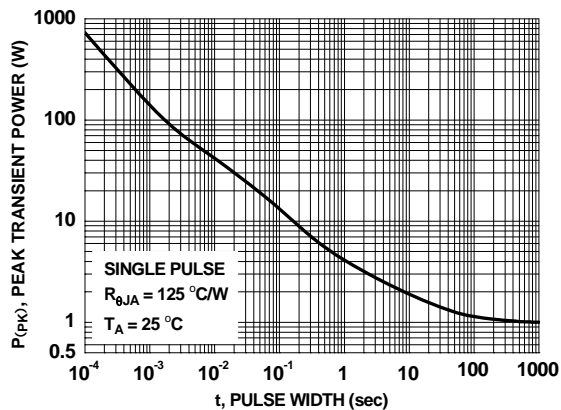


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

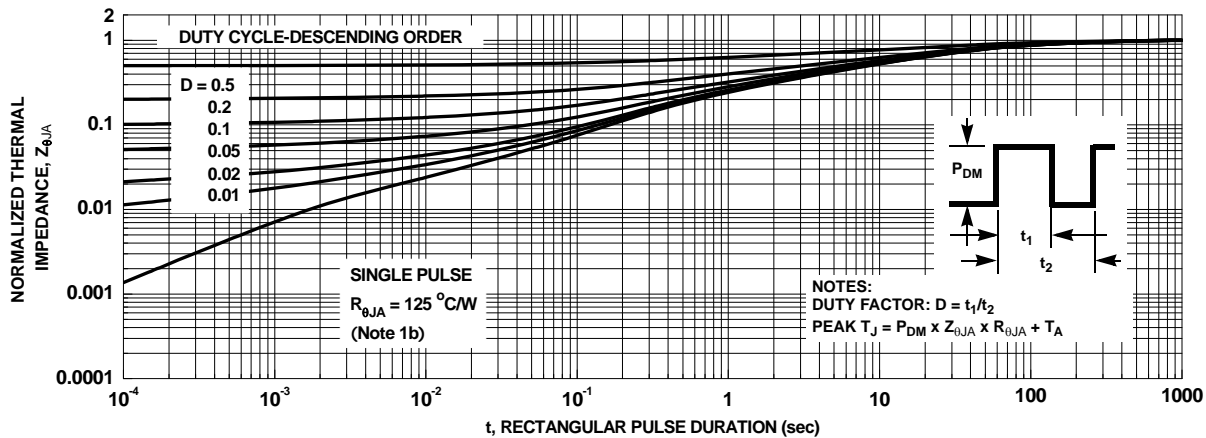


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET[™] Schottky body diode Characteristics

Fairchild's SyncFET[™] process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMC0310AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

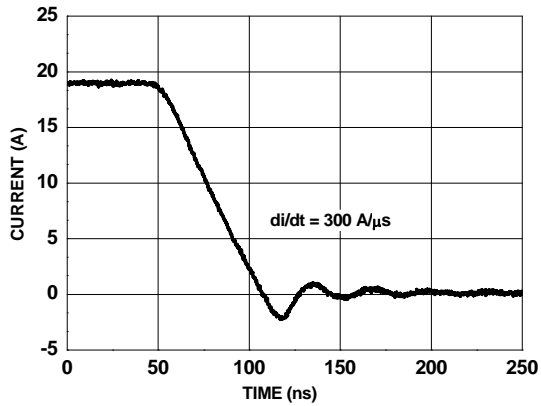


Figure 14. SyncFET[™] Body Diode Reverse Recovery Characteristic

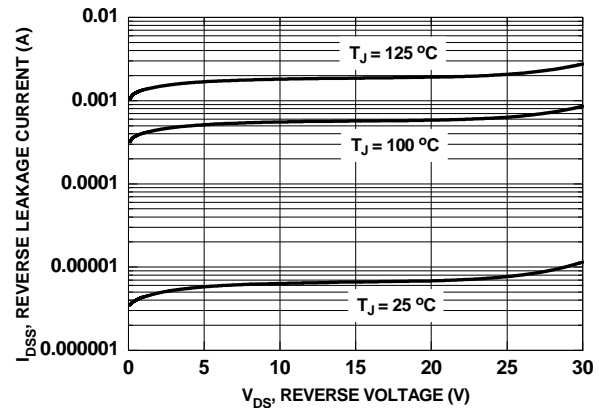
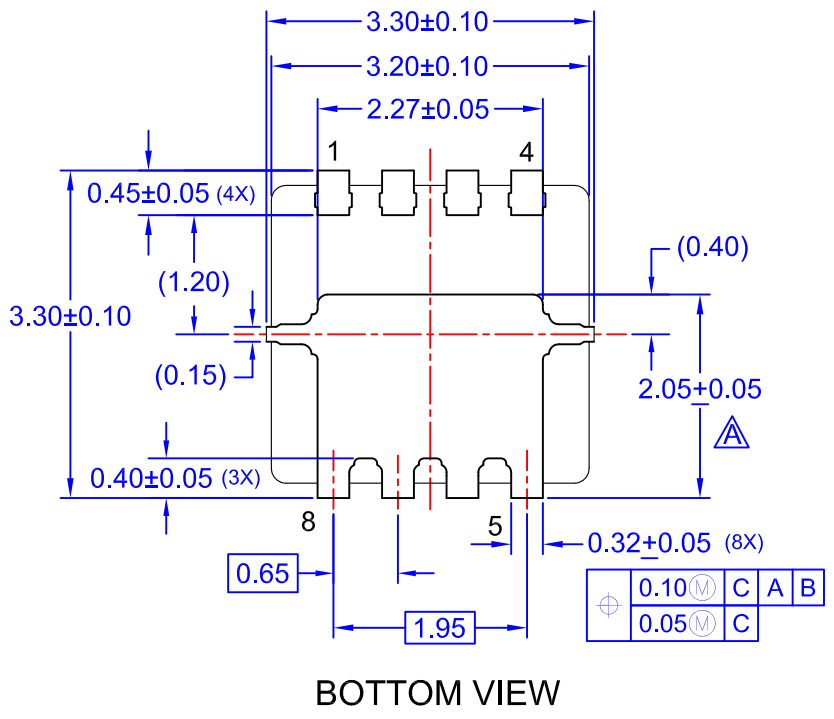
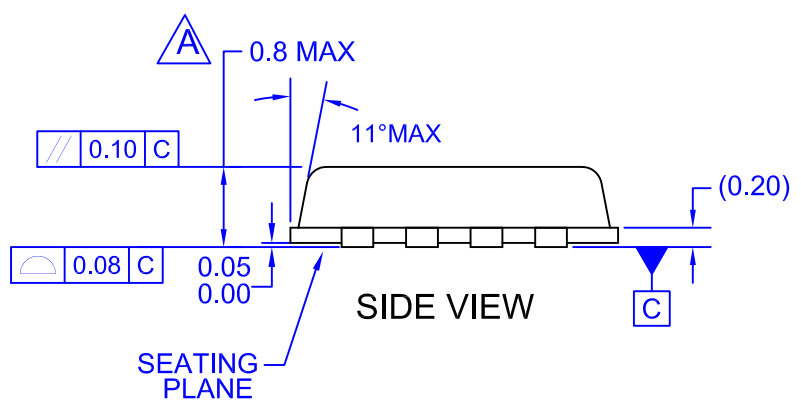
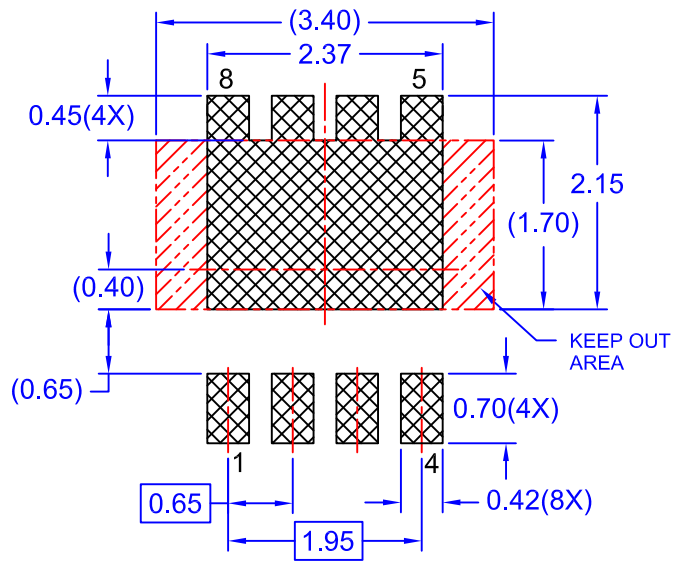
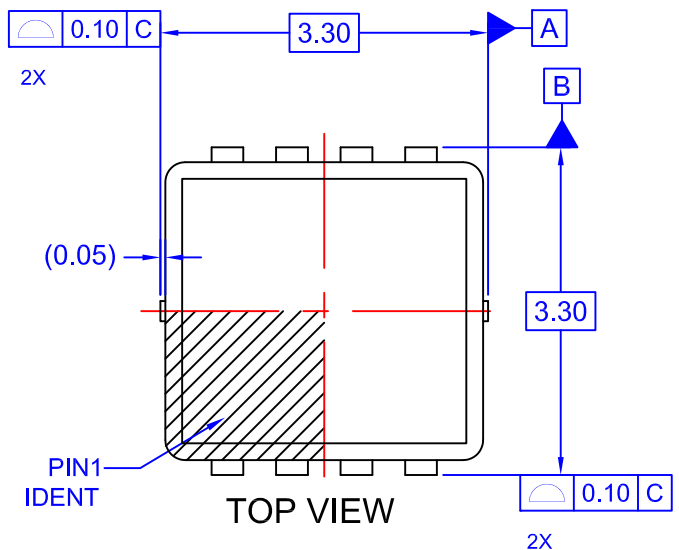
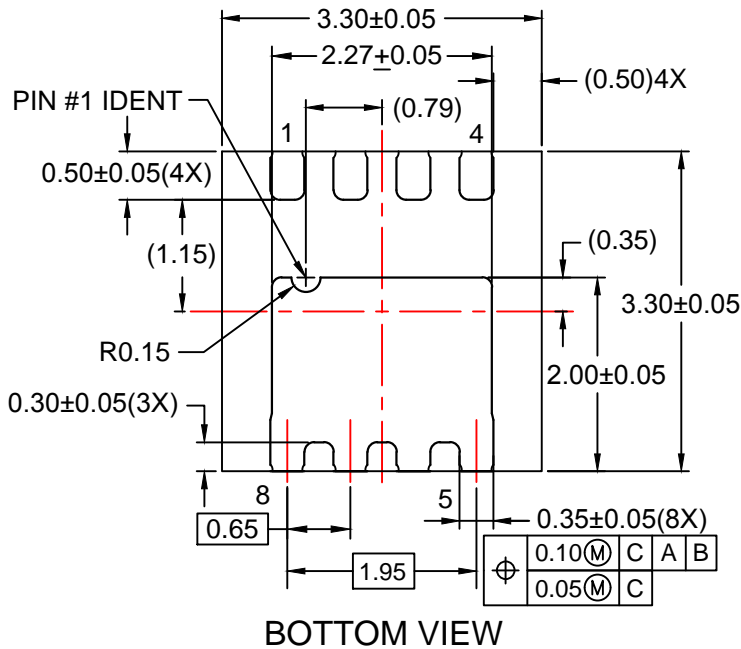
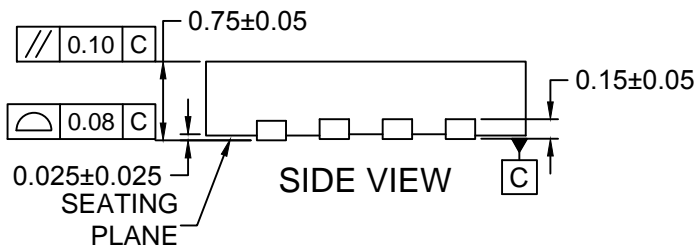
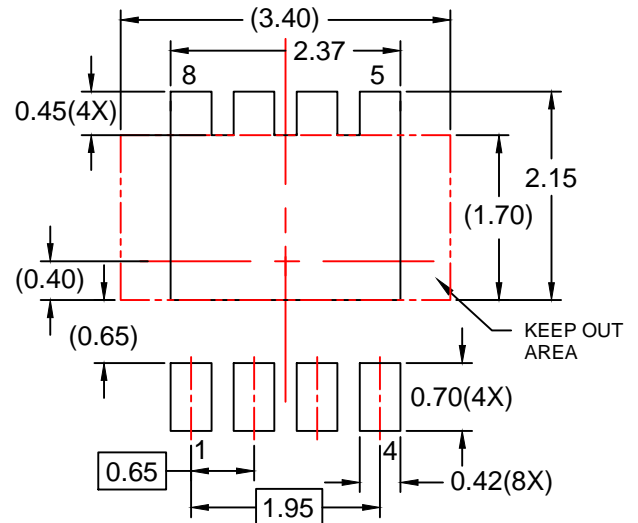
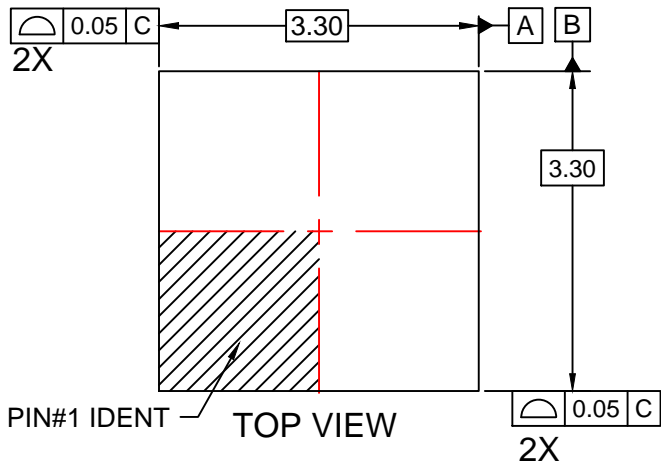


Figure 15. SyncFET[™] Body Diode Reverse Leakage vs. Drain-Source Voltage



- NOTES:**
- A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
 - D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
 - E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.
 - F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
 - G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.
 - H. DRAWING FILENAME: MKT-MLP08Trev4.
 - I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.





NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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