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Vishay/Siliconix SUM90N04-3M3P-E3

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Datasheet of SUM90N04-3M3P-E3 - MOSFET N-CH 40V 90A D2PAK

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SUM90N04-3m3P

Vishay Siliconix

N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) ^d	Q _g (TYP.)			
40	0.0033 at V _{GS} = 10 V	90	87			
	0.0041 at V _{GS} = 4.5 V	90	01			



FEATURES

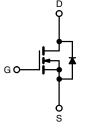
- TrenchFET® Power MOSFET
- 100 % R_g and UIS tested

• Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

COMPLIANT

APPLICATIONS

- Power supply
 - Secondary synchronous rectification
- DC/DC converter
- Power tools



N-Channel MOSFET

Ordering Information:

SUM90N04-3m3P-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS	(T _C = 25 °C, unless of	otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V _{DS}	40	V		
Gate-Source Voltage		V _{GS}	V _{GS} ± 20		
0 1	T _C = 25 °C		90 d		
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	l _D	90 d	٨	
Pulsed Drain Current (t = 300 μs)		I _{DM}	160	А	
Avalanche Current		las	60		
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	180	mJ	
Maximum Power Dissipation 8	T _C = 25 °C	В	125 ^b	W	
Maximum Power Dissipation ^a	T _A = 25 °C °C	- P _D	3.1] vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W		
Junction-to-Case (Drain)	R _{thJC}	1	- 'C/VV		

- a. Duty cycle $\leq 1 \%$.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Package limited.

S13-2462-Rev. B, 02-Dec-13 Document Number: 63397

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V_{GS} = 0 V, I_D = 250 μA	40	-	- V		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1	-	2.5	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 250	nA	
		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μА	
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125 °C	-	-	50		
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 150 °C	-	-	250		
On-State Drain Current a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	50	-	-	Α	
Duelle Octobe Decisteres 8	Б	V _{GS} = 10 V, I _D = 22 A	-	0.0027	0.0033	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 20 A	-	0.0034	0.0041		
Forward Transconductance a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A	-	169	-	S	
Dynamic ^b							
Input Capacitance	C _{iss}		-	5286	-	pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 20 \text{ V}, f = 1 \text{ MHz}$	-	705	-		
Reverse Transfer Capacitance	C _{rss}		-	283	-		
Total Gate Charge c	Qg		-	87	131	nC	
Gate-Source Charge c	Q _{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	15.3	-		
Gate-Drain Charge ^c	Q _{gd}		-	12.2	-		
Gate Resistance	R_g	f = 1 MHz	0.5	2.7	5.4	Ω	
Turn-On Delay Time ^c	t _{d(on)}		-	11	20		
Rise Time ^c	t _r	$V_{DD} = 20 \text{ V}, R_1 = 2 \Omega$	-	7	14		
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	45	68	ns -	
Fall Time ^c	t _f		-	7	14		
Drain-Source Body Diode Ratings a	nd Characteris	stics (T _C = 25 °C) b					
Continuous Current	I _S		-	-	90	А	
Pulsed Current	I _{SM}		-	-	160		
Forward Voltage ^a	V _{SD}	I _F = 10 A, V _{GS} = 0 V	-	0.72	1.2	V	
Reverse Recovery Time	t _{rr}		-	42	63	ns	
Peak Reverse Recovery Current	I _{RM(REC)}	$I_F = 10 \text{ A}, dI/dt = 100 \text{ A/}\mu\text{s}$	-	2.5	3.8	Α	
Reverse Recovery Charge	Q _{rr}		-	52	78	nC	

Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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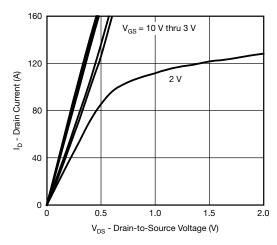
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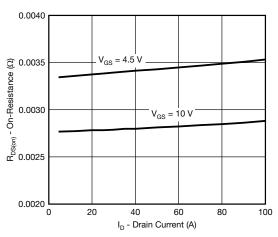
SUM90N04-3m3P



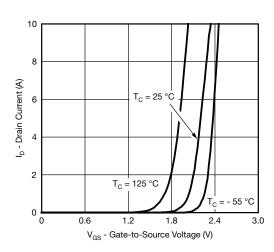
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

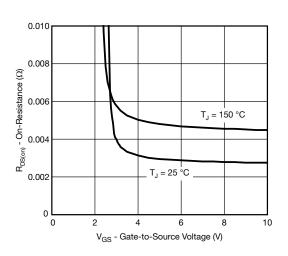




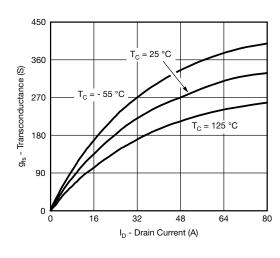
Output Characteristics



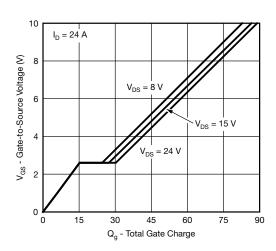
On-Resistance vs. Drain Current



Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage



Transconductance

Gate Charge

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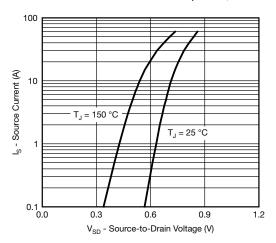


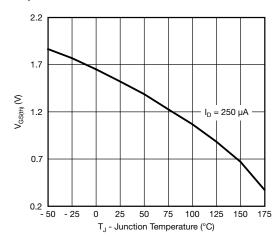


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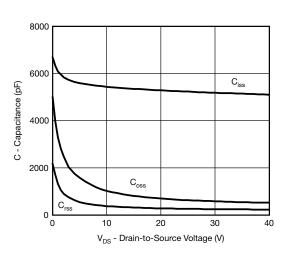
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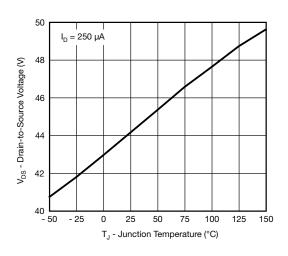




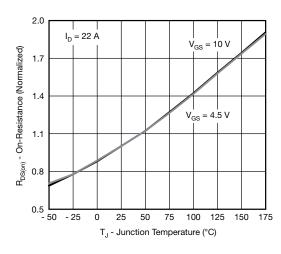
Source-Drain Diode Forward Voltage



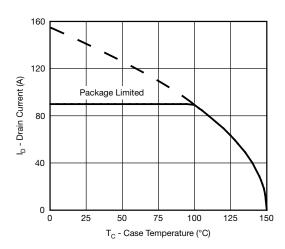
Threshold Voltage



Capacitance



Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Junction Temperature

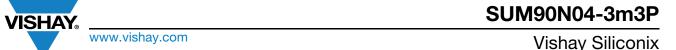
Current Derating

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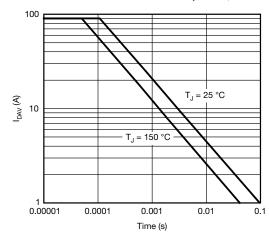
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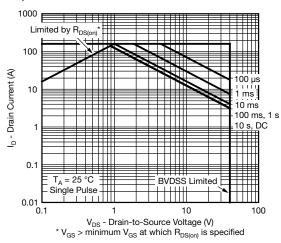
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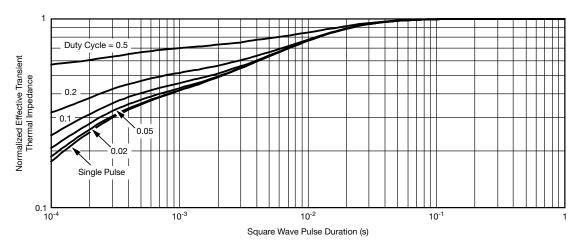
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Single Pulse Avalanche Current Capability vs. Time

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63397.

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MILLIMETERS

MAX.

MIN.

1.016

1.270

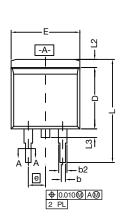
1.397

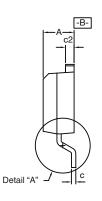
1.778

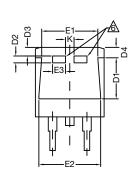
0.050

0.254 BSC

TO-263 (D²PAK): 3-LEAD

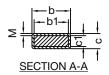








DETAIL A (ROTATED 90°)



Α		0.160	0.190	4.064	4.826	
b		0.020	0.039	0.508	0.990	
b1		0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
D1		0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
E3		E3 0.072		1.829	1.981	
е		0.100	BSC	2.54 BSC		
K		0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605 15.8		
L1		0.090	0.110	2.286	2.794	

INCHES

MAX.

MIN.

ECN: T13-0707-Rev. K, 30-Sep-13

0.040

0.050

0.055

0.070

0.002

0.010 BSC

DWG: 5843

12

L3

L4

Μ

DIM.

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.

6. This feature is for thick lead.

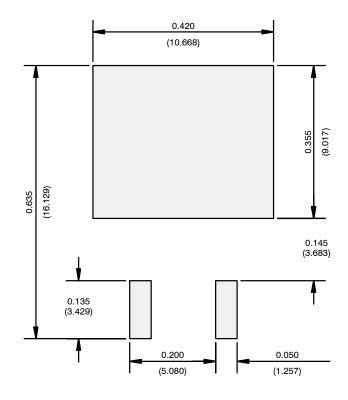
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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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